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TSMC 28nm overview

- From discussions at PIXEL2022: TSMC is trying to push designs away from 65nm and people start questioning the long-medium term availability of this technology.

The TSMC 28nm technology is the most performant planar mainstream solution that evolved through the years due to constant enhancements in the manufacturing process.
It supports a wide range of applications, including CPUs, GPUs, high-speed networking chips, smart phones, APs, tablets, home entertainment, consumer electronics, automotive and IoT.

It mainly uses High-k Metal Gate (HKMG) gate-last technology. Compared to the gate-first technology, the gate-last offering provides more advantages, including lower leakage current and better chip performance.

28nm CMOS HPC Logic, RF	
Technology characteristics	Shrink technology: YES Core voltage: 0.9V I/O voltage: 1.8V Shallow Trench Isolation (STI) Wells: Retrograde twin well for low well sheet resistance and better latch-up behavior. Triple well, Deep N-Well in option Dual Gate Oxide Vt options: ulvt, lvt, svt, hvt, uhvt, ehvt 5V HVMOS HighRes resistors Temperature range: -40C to 125C # of metals: 5 to 10 Cu + ALRDL Interconnect dielectric: ELK Top metal: 8.5KA, 11.5KA, 35KA CMP on STI, contact, via and passivation MoM capacitor Passivation: dual layers

Options that need special attention	SRAM Cell Vt's: maximum of 4 VT types in one design.
Wafer size	12 inch
Deliverables	100 dies, no wafer
Design tools	PDK: TSMC iPDK
Simulation tools	HSPICE, Eldo, Spectre
Verification tools DRC	Cadence, Siemens EDA, Synopsys
Verification tools LVS	Cadence, Siemens EDA, Synopsys
Parasitic extraction tools	Cadence, Siemens EDA, Synopsys
P&R tools	Cadence, Siemens EDA, Synopsys
Foundry IP	12-track / 9-track / 7-track core cell libraries, multi-vt's 0.9V/1.8V hybrid staggered (fail-safe digital and regular analog) I/O library SRAM compilers by TSMC , ARM, Synopsys
MPW block size	6mm² (on silicon)
Mini@sic characteristics	Supported Min area: 1mm² (post-shrink) mini@sic Technology options

Other technical details

- Lower metal layers: 0.45Ω/□
  (UMC110: M1=0.17 Ω/□;M2= 0.13Ω/□)
- fT above 300 GHz

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Recommended 28 nm mini@sic options

Metal Scheme	9M_5X1Y1Z1U UT-ALRDL
Flip-Chip/bumping	Not supported in the common flow. Please contact eptsmc@imec.be.
Allowed devices	(1) ultra low Vt = {VTUL_N OR VTUL_P} (2) low Vt = {VTL_N OR VTL_P} (3) high Vt {VTH_N OR VTH_P) (4) ultra high Vt = {UHVT_N OR UHVT_P} Standard devices are by default allowed Contact eptsmc@imec.be if other Vt's are needed.
SRAM/ ULL SRAM	Not supported in the common flow. Please contact eptsmc@imec.be.
AP thickness	28kA
Backlapping thickness	11 mils

Important note:
Always use the T-N28-CR-SP-029 (mmWave ULL) PDK with flavor RF HPC+ 0.9/1.8V.
Sub-dicing of multiple sub-chips is not possible.

Restrictive Design Rules

- Starting from the 28 nm technological node, the **design rules are becoming much more complex** in terms of device usage, density requirements and physical design limits.
- Poly and metal density must be kept very uniform across the die in order to fabricate the minimum channel length devices in a reliable way.
- Beside limits on the minimum and maximum poly density, there are also rules for the maximum poly area per device finger: large area devices must be fragmented
- Gate orientation of all the devices must be uniform across the whole wafer, circuits rotation is strictly prohibited.
- Maximum transistor gate area,maximum transistor width W and length L:in 28 nm the maximum W and L for a single device finger are 3µm and 1µm, respectively.

Radiation Hardness

- Enclosed-layout devices not possible
- Circuital approaches more challenging (and not always enough)
- Ultra-scaled technologies, and especially the 28 nm, results to be more radiation resistant than the others
  - radiation damage is proportional to gate oxide volume
  - gate dielectric has been replaced with high-k materials

Accessibility through EP

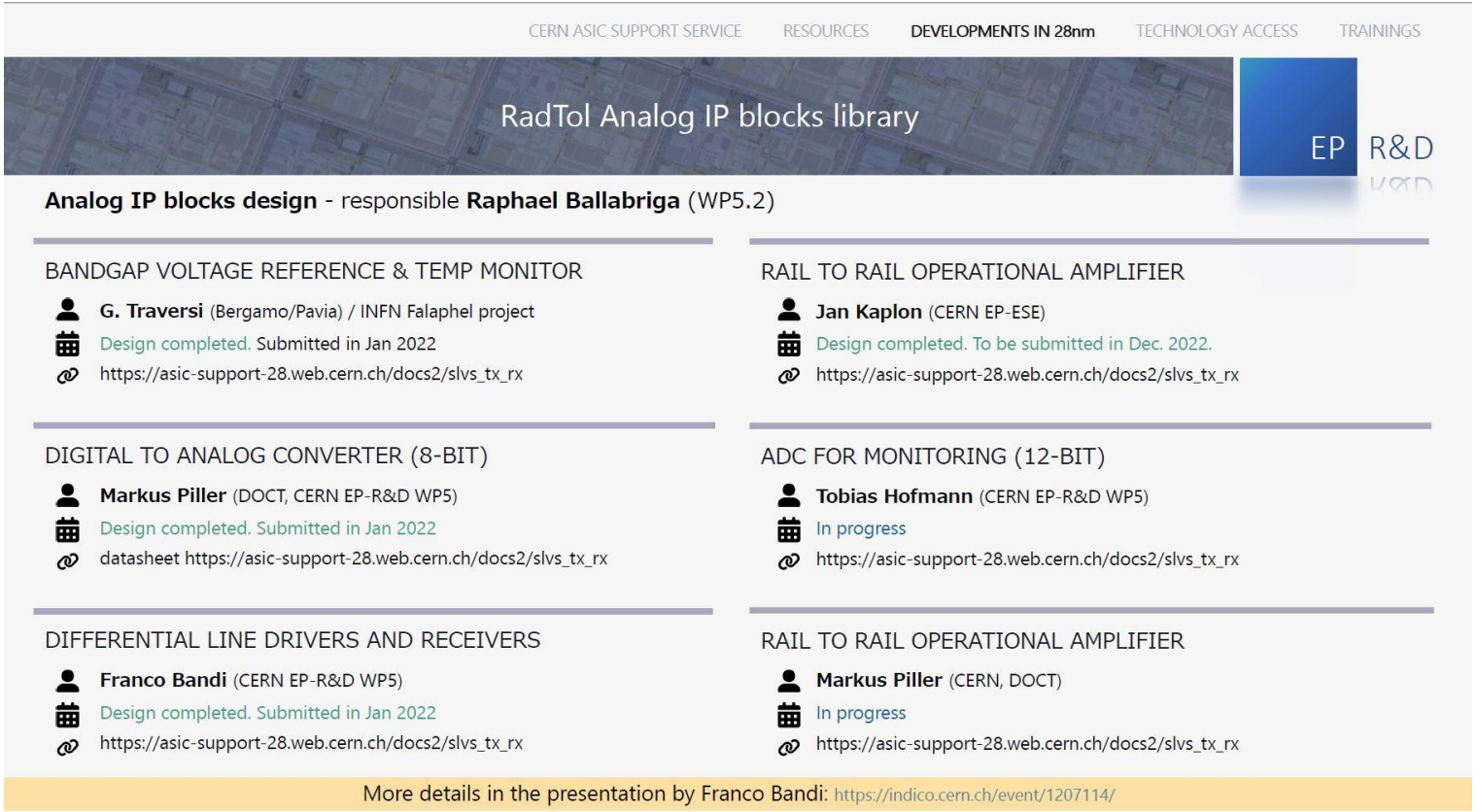
mini@sic:

- HPC: 1 run/year
- HPC+: 3 runs/year

MPW:

- HPC/HPC+: 12 runs/year

CERN support



RadTol Analog IP blocks library

EP R&D

Analog IP blocks design - responsible **Raphael Ballabriga** (WP5.2)

ANALOG PLL

Tobias Hofmann (CERN EP-R&D WP5)

In progress

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

DIGITAL PLL

Markus Piller (DOCT, CERN EP-R&D WP5)

In progress

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

Powering solutions design - responsible **Stefano Michelis** (WP5.2b)

DCDC CONVERTER

Stefano Michelis and **Giacomo. Ripamonti** (CERN EP-ESE)

In progress

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

LDO

Stefano Michelis and **Giacomo Ripamonti** (CERN EP-ESE)

In progress

https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

More details in the presentation by Franco Bandi: https://indico.cern.ch/event/1207114/

RadTol Analog IP blocks library

Fundamental IP blocks - responsible **ASIC Support Service**

RADIATION TOLERANT ESD PROTECTIONS

- **Outsourced to SOFICS** by the CERN ASIC Support
- Design completed. Submitted in Jan 2022 for radiation characterization.
- https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

RADIATION TOLERANT CMOS IO PAD

- **outsourced to SOFICS** by the CERN ASIC Support
- In progress. Radiation characterization will follow.
- https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

SRAM MEMORIES

- **Compilers purchased from the Foundry** by the CERN ASIC Support
- We can distribute precompiled memory upon request
- Submitted in Jan 2022. Radiation characterization completed.
- https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

EFUSES

- **IP block purchased from the Foundry** by the CERN ASIC Support
- Radiation characterization will follow.
- https://asic-support-28.web.cern.ch/docs2/slvs_tx_rx

More details in the presentation by Franco Bandi: https://indico.cern.ch/event/1207114/

Cost

- K. Kloukinas:

«A full maskset with all technology options and maximum metal stack (9 metals) is **1.2 million USD**».

As a reference:

110nm UMC: 150,000 USD

65nm TSMC: 500,000 USD

MPW are on the contrary rather cheap, I don’t have a number but I think ~40,000 for the minimum size. MiniAsics are possible.

Status

- We should receive the NDA to sign vwery soon (today?)
- It should go much quicker than with 65nm: