PAUL SCHERRER INSTITUT

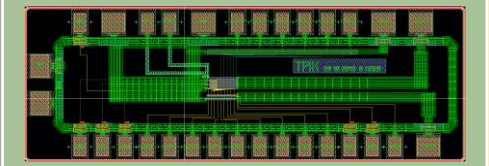
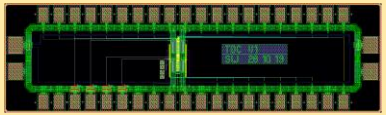
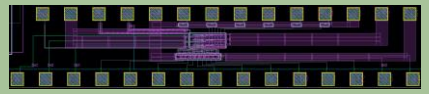
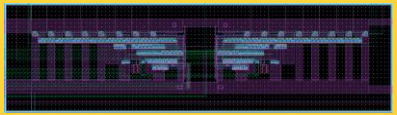
PSI

Beat Meier :: Paul Scherrer Institut

TDC Development at PSI and UZH

Chip Design Meeting 20. Juni 2022

TDC (Time to Digital Converter) Fall 2019

		TPIX **Analog Ring Readout** *Layout: Beat Meier* *Test: Matías Senger, Beat Meier*	TDC **Digital Ring Readout** *Layout: Stephan Wiederkehr* *Test: Matías Senger*	ATDC **no Ring Readout** *Layout: Wolfram Erdmann* *Test: A. Ebrahimi, W. Erdmann*
TECHNOLOGY	UMC110			
	LF110			

Time Resolution Requirements

CMS TEPX timing layer **30 ps**

- Low Gain Avalanche Detectors LGAD preferred
- Project with UZH

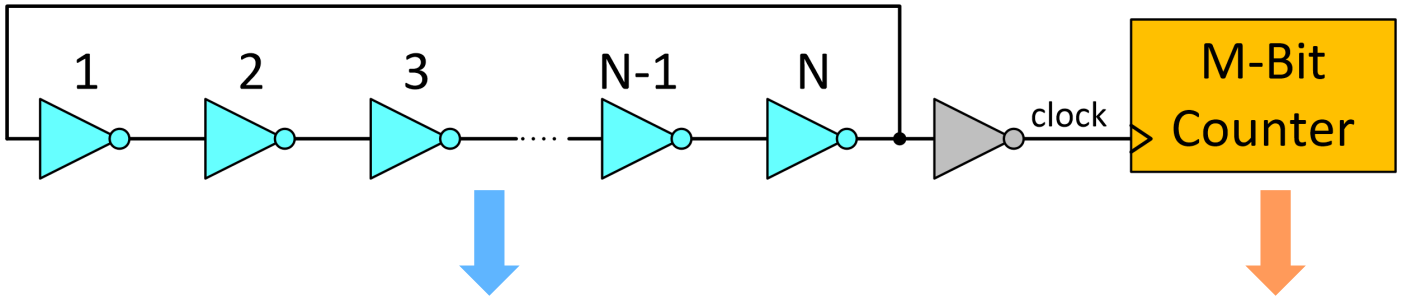
Other Projects: **100 ps**

TDC Based on Ring Oscillator and Counter

Ring oscillator controlled by

START (pixel hit)

STOP (reference clock)



Ring Readout (snapshot)

Fine resolution > t_{PD}

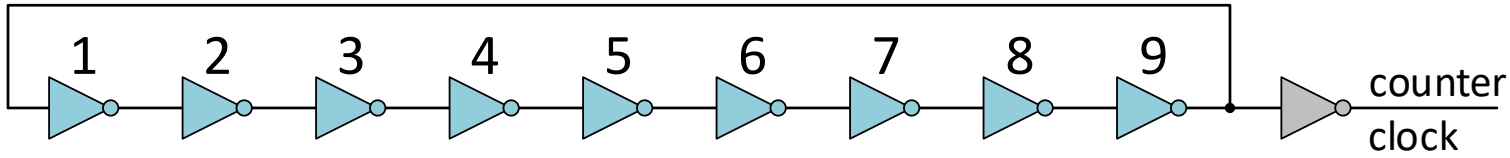
Cycle Counter Readout

Coarse resolution >1 ns

Example:

- Propagation delay: 60 ps
- N = 9: T = 1 ns; f = 1 GHz

Ring Oscillator Gate Propagation Delay t_{PD}



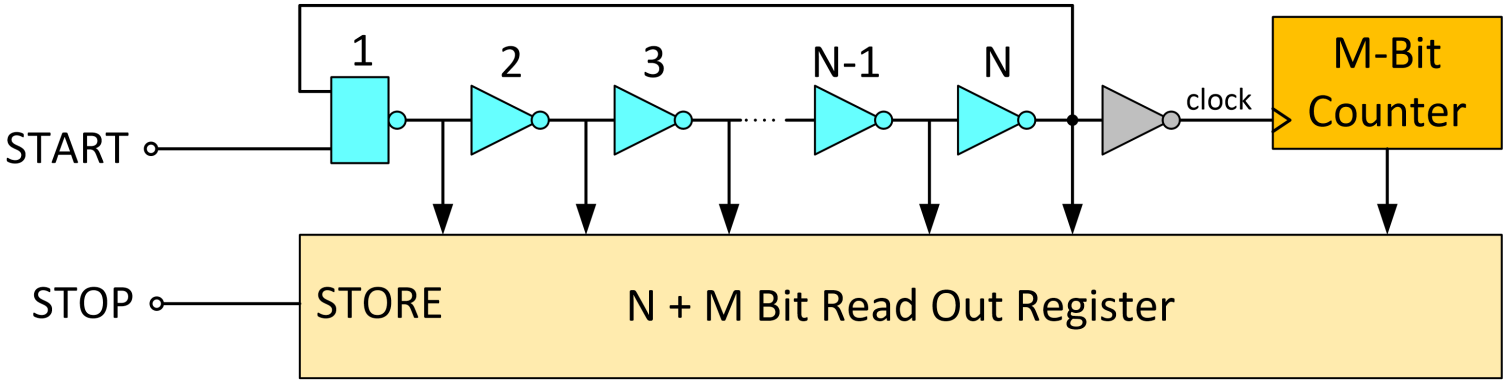
LF	⎍	124	114	111	111	110	108	108	113	141	ps
	⎎	68	64	48	45	48	45	47	51	100	ps
UMC	⎍	114	88	110	109	92	99	98	111	133	ps
	⎎	51	37	36	36	35	42	32	29	96	ps

TPIX; enclosed transistors nand gates; VDD = 1.2 V

LF110 T = 1550 ps (645 MHz) t_{PD} = 86 ps

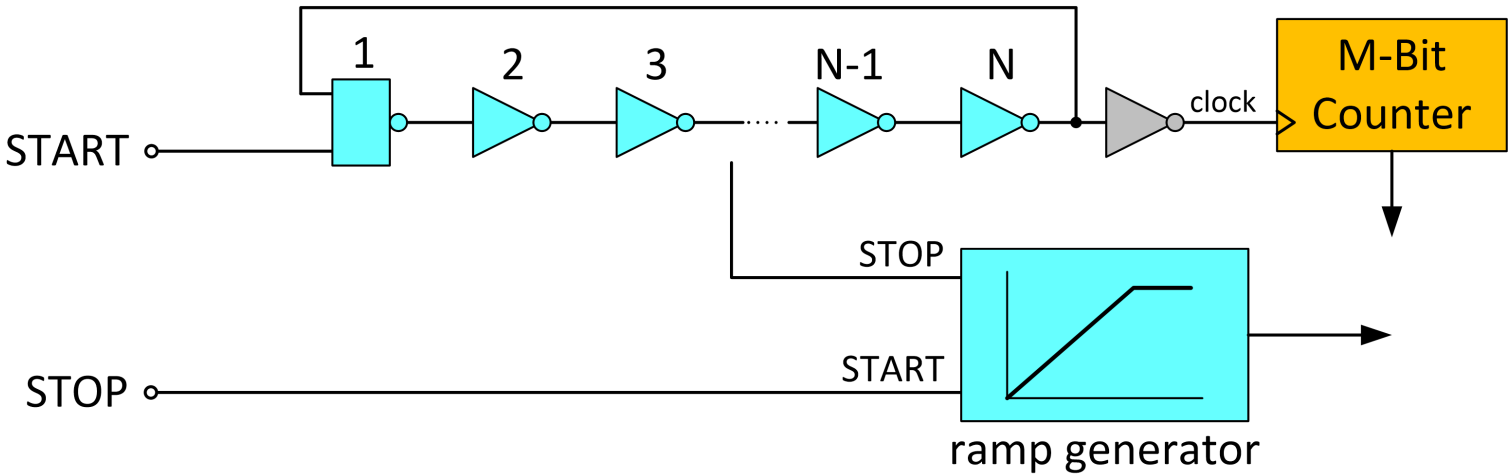
UMC110 T = 1350 ps (740 MHz) t_{PD} = 75 ps

TDC Fully Digital Readout



- Easy to read out; fully digital; No ADC needed
- Huge size; only for big pixel or in periphery
- High capacitive load of ring oscillator → high $t_{PD} \approx 100\ ps$
- t_{PD} resolution limit (can be reduced only with another technology)
- common TDC designs

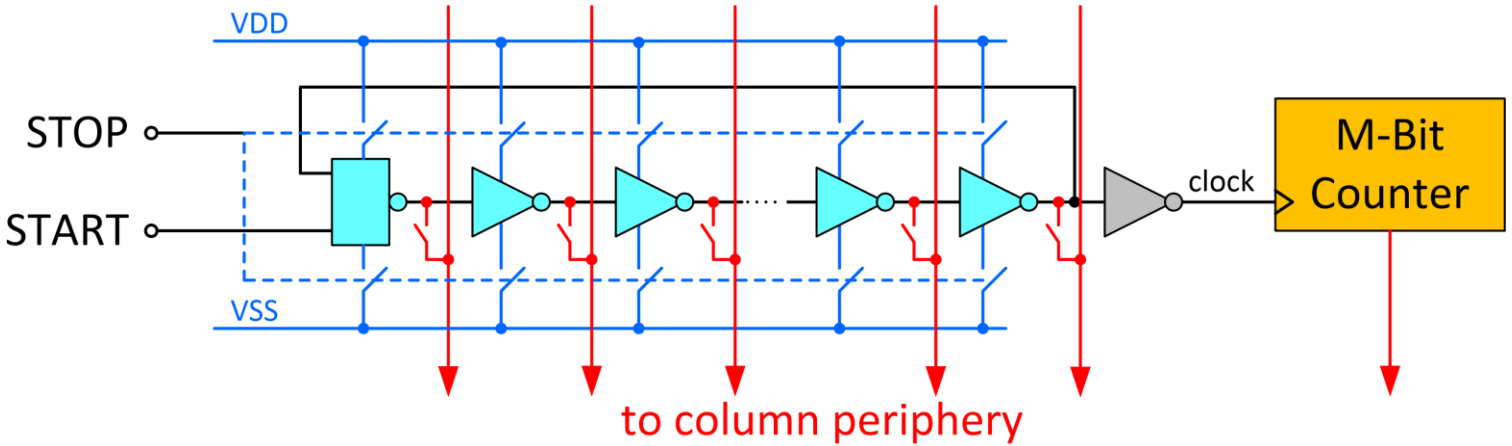
ATDC



- no ring oscillator readout
- After stop, ring runs to the end
- I-C Ramp generator for sub ns resolution

- no T_{PD} resolution limit
- time resolution limited by nonlinearity, noise of ramp generator, calibration
- higher resolution ADC for analog read out (6 bit or more)

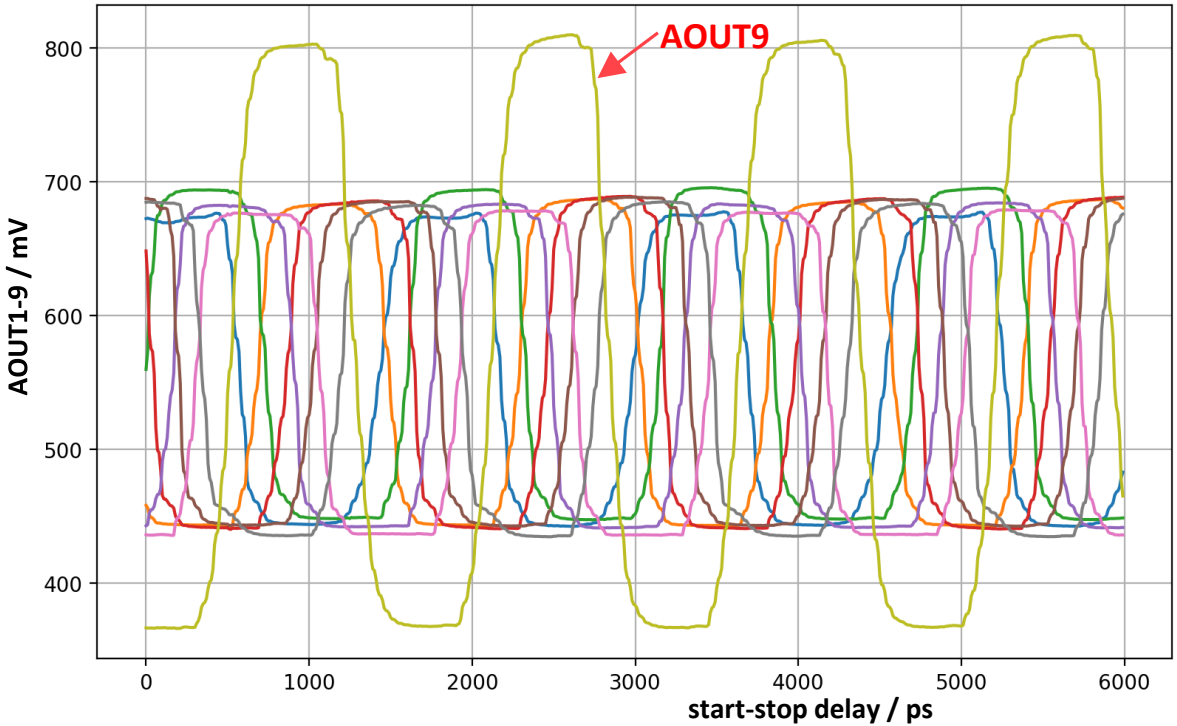
TPIX: Analog Ring Readout

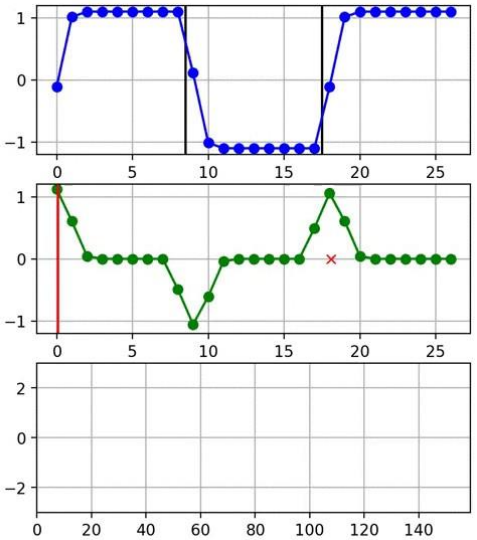


- Charge storage in ring oscillator
- Charge readout of a full column like a analog storage cell
- Minimal circuitry for read out
- minimal size; 50 um x 25 um

- digital readout: t_{PD} resolution limit
- analog readout: sub T_{PD} resolution
- only 2 bit ADC needed
- High effort for analog interpolation in periphery (not yet solved)
- Non uniformity of the ring oscillator

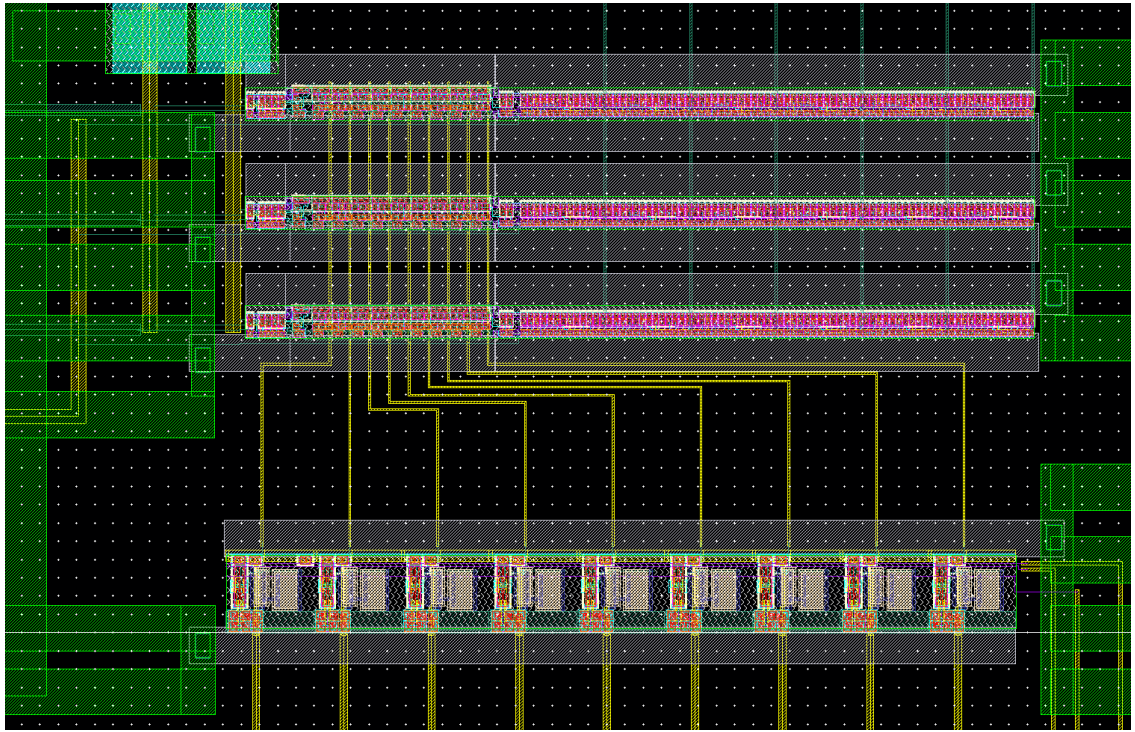
TPIX: Analog Read Out





running ring oscillator measured with 1 ps time resolution

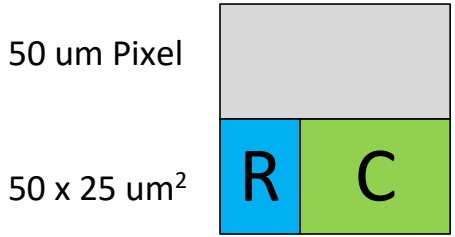
TPIX required Space in Pixel (UMC)



ring stage 4.86 x 9.1 = **44.2 um²**
ring 9 x 44.2 um² = 398 um²
ring interface 5.5 x 9.1 = 50 um²
ring area: **450 um²** **36%**

counter stage 21.1 x 6 = **126.6 um²**
counter (6 stages) 760 um²
counter interface 8.3 x 6 = 50 um²
counter area: **810 um²** **64%**

Total area: **1260 um²** **100%**



Integration

So far:

- Isolated test structures
- Ideal START/STOP signals from a test system

MOTIC Chip (*Stephan Burkhalter)*:

- MAPS demonstrator, IFoundry
- Full pixel array
- ATDC (with analog readout) per pixel group
- Order of some 100 ps resolution ok. MAPS rather slow

LGAD sensor readout (Matías Senger UZH):

- Readout amplifier under test stagnates due to lack of components for the tester
- Test with LGAD + preamp/comp + TDC in Preparation

Next Steps

Integration in a readout chip: PROC600 with TDC?

- Which readout architecture?
- TDC per Pixel? Per Column? Per Chip?
- TDC architecture is highly dependent on the application
- It is not useful to spend a lot of time in a “fantasy” architecture

Applications needed

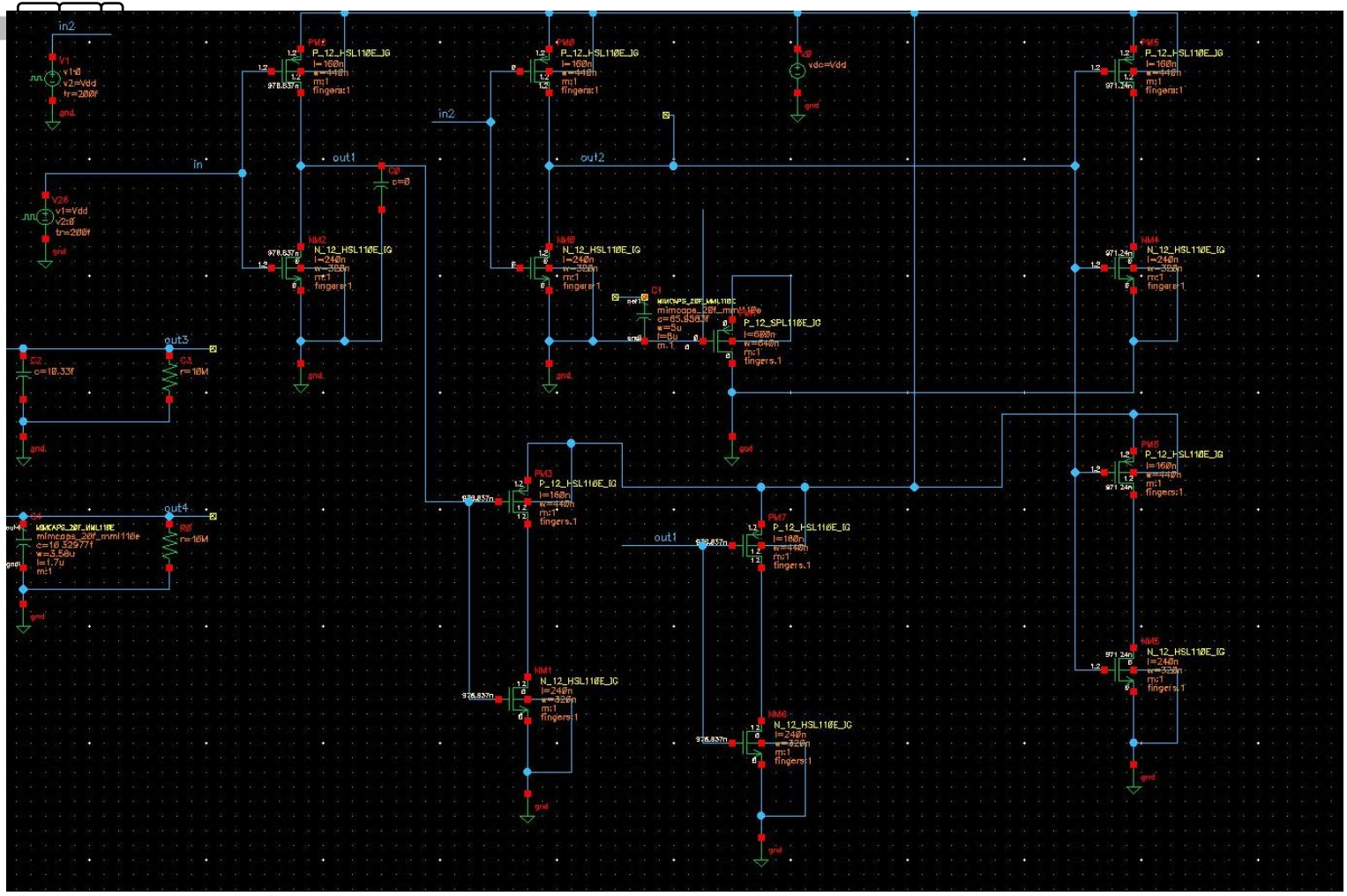
Change to 65 nm technology

- for lower t_{PD}
- to reach 30 ps resolution with digital TDC
- no analog readout (ADC) needed with TPIX
- PSI already signed NDAs for TSMC 65nm and UMC 65nm (*Roberto*)
- CERN NDA for TSMC 65nm where I have access

New Technology

NOTES BY ROBERTO

~2h work!!!! Just some very rough, brainstorming-type, ideas/calculations!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v1=0
v2=Vdd
tr=200f
gnd
PM4
P_12_HSL110E_IG
l=160n
w=440n
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fingers:1
978.837n
PM0
vdc=Vdd
PM5
971.24n
in
out1
C0
c=0
V26
v1=Vdd
v2=0
tr=200f
NM2
N_12_HSL110E_IG
l=240n
w=320n
NM0
out2
NM4
C1
mimcaps_28f_mml110e
c=65.9361f
w=5u
l=5u
m:1
P_12_SPL110E_IG
l=680n
w=440n
fingers:1
out3
C2
c=10.33f
C3
r=10M
out4
C4
mimcaps_28f_mml110e
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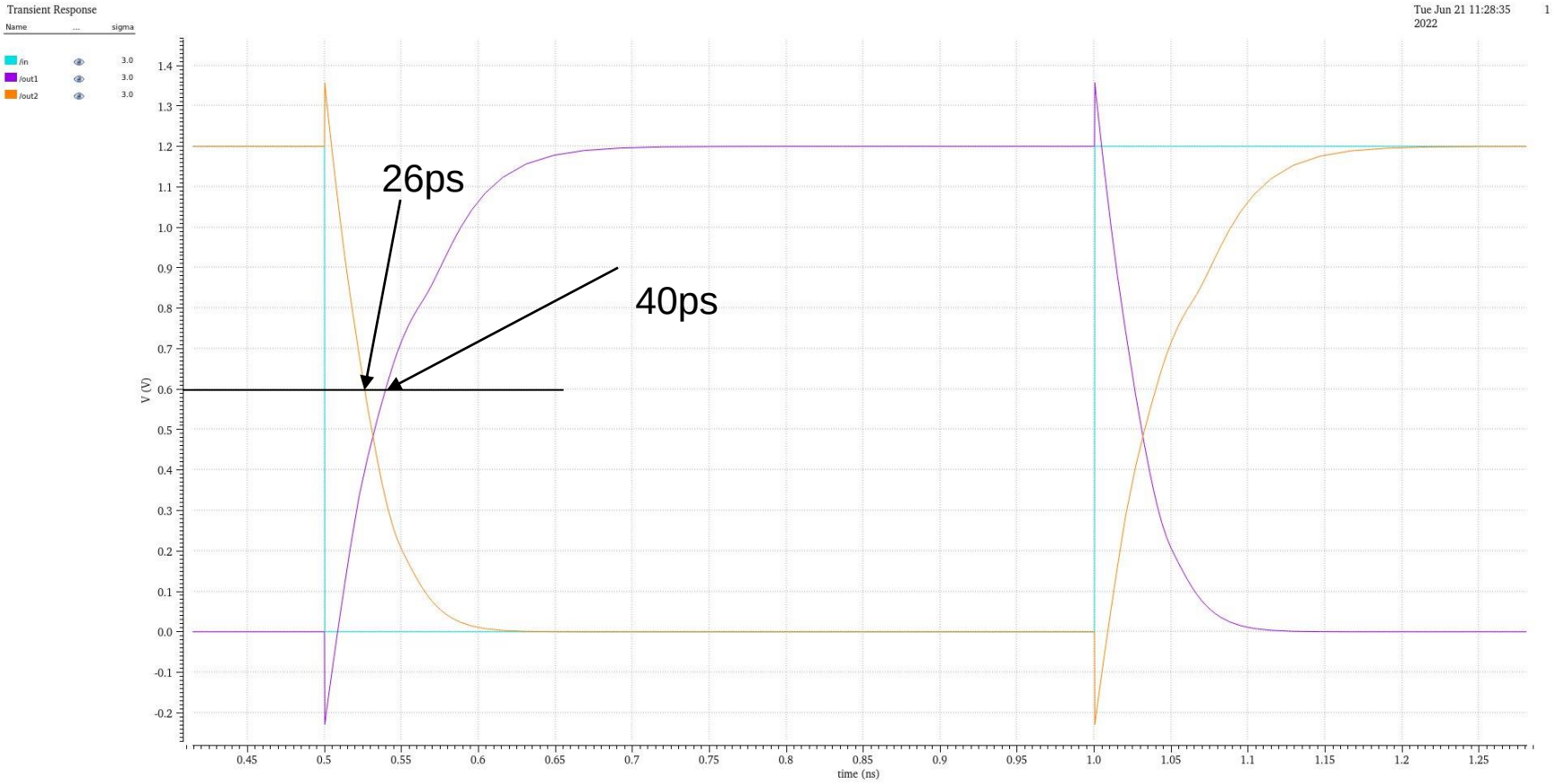
C5
PM3
PM7
PM8
NM1
NM6
NM5


Transient Response
Tue Jun 21 11:28:35 2022
1
Name
...
sigma
/in
3.0
/out1
3.0
/out2
3.0
26ps
40ps
V (V)
time (ns)

Area calculation

- Size: 2 inverters (not min. size,p=2x n): ~1.8x1.8um2 ~ 1.62um2/inv.;
- My counter (minimal size transistors, includes storage): 4bits=28x4.6u2=32.2um2/bit

(You probably do not need the storage in the counter, but you need output buffers)

- 8 gates ring osc. (3bit) + 7 bit counters=1.62x8 + 32.2um2/bit*7=238.36; sqrt(238)=15.4
- I think every cell will need 2 inverters=1.62x16+32.2*7=**251um2**; sqrt(251)=15.9 (10 bit equivalent)
- Estimated size for tpix**: 1250um2 (~9bit equivalent)**

SUMMARY

- With linear transistors (not minimum size) you can do >2x better in terms of timing and >5x better in terms of area
- Based on “0 level approximation”, i.e. all timing resolution comes from tpd, the rest can be “calibrated away” (strongly doubt about that)

- Rad tol.
  - Counter with minimum size transistors dies after 0.7-1Grad (but recovers after annealing)
  - Digital leakage?
  - More tests ongoing
  - Rad. tests planned with Matterhorn 0.1