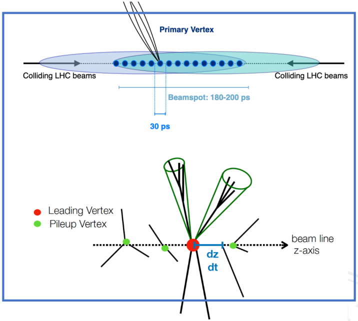
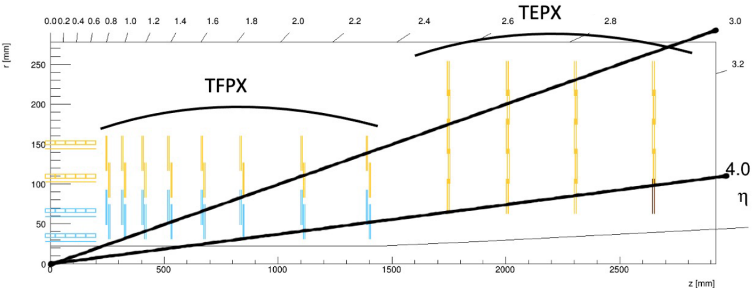
Timing in CMS



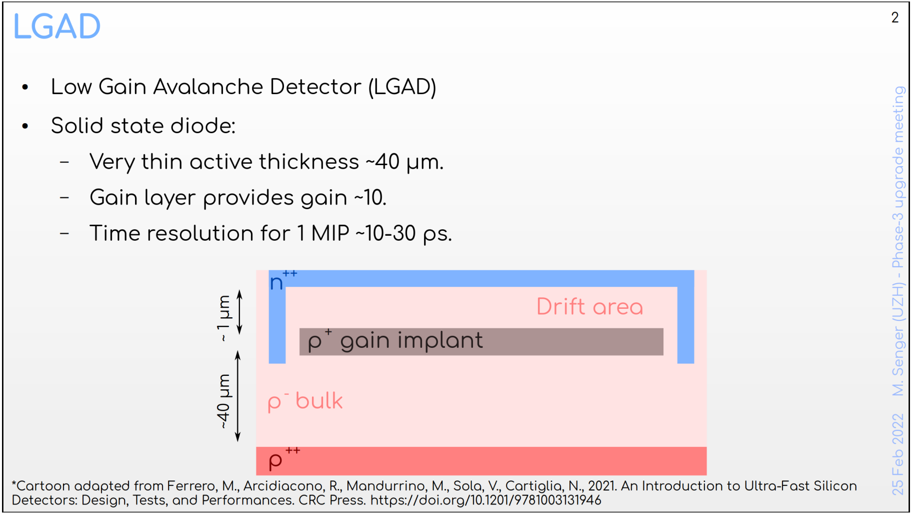
- HL-LHC : 140 – 200 simultaneous collisions
- collision region 4 cm
  2 and more collisions per mm
- difficult to do disentangle, especially for forward tracks

- CMS plans to exploit the fact that collisions are spread in time, too
- barrel + endcap timing detectors in 'Phase 2' (2030)
- resolution 30 ps–50 ps

CMS inner tracker



- CMS 'Phase 2' timing covers region up to $\eta = 3$ (BTL: LYSO + SiPM, ETL LGAD pads)
- possible extension to $\eta = 4$ in 'Phase 3': replacing 1 or 2 TEPX pixel disks with LGAD pixels

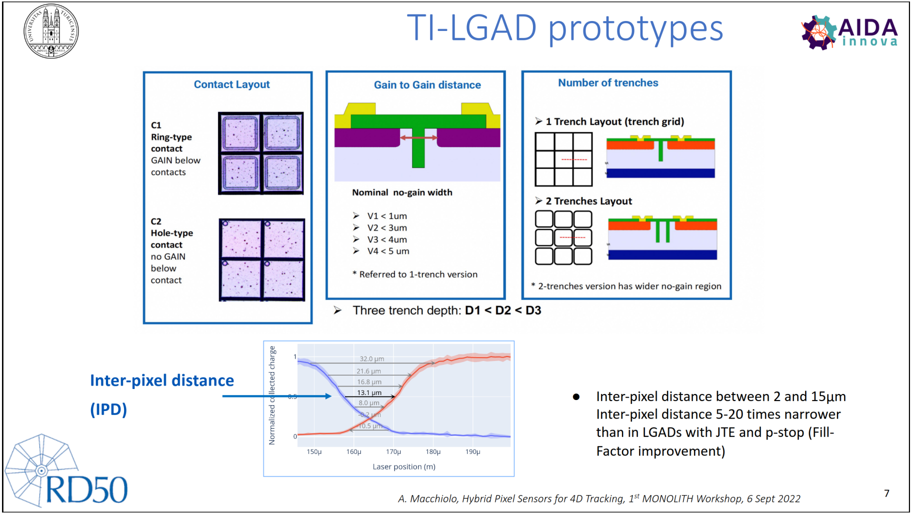


LGAD

- Low Gain Avalanche Detector (LGAD)
- Solid state diode:
  - Very thin active thickness ~40 µm.
  - Gain layer provides gain ~10.
  - Time resolution for 1 MIP ~10-30 ps.

*Cartoon adapted from Ferrero, M., Arcidiacono, R., Mandurrino, M., Sola, V., Cartiglia, N., 2021. An Introduction to Ultra-Fast Silicon Detectors: Design, Tests, and Performances. CRC Press. https://doi.org/10.1201/9781003131946

caveats : radiation hardness, dead region between pixels



TI-LGAD prototypes

Contact Layout

C1
Ring-type contact
GAIN below contacts

C2
Hole-type contact
no GAIN below contact

Gain to Gain distance

Nominal no-gain width

- V1 < 1um
- V2 < 3um
- V3 < 4um
- V4 < 5 um

* Referred to 1-trench version

Number of trenches

- **1 Trench Layout (trench grid)**
- **2 Trenches Layout**

* 2-trenches version has wider no-gain region

- Three trench depth: **D1 < D2 < D3**

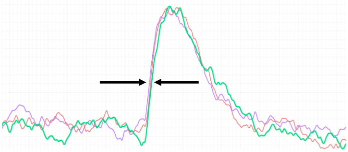
Inter-pixel distance

(IPD)

- Inter-pixel distance between 2 and 15µm
  Inter-pixel distance 5-20 times narrower than in LGADs with JTE and p-stop (Fill-Factor improvement)

A. Macchiolo, Hybrid Pixel Sensors for 4D Tracking, 1st MONOLITH Workshop, 6 Sept 2022

noise contributions : electronics noise



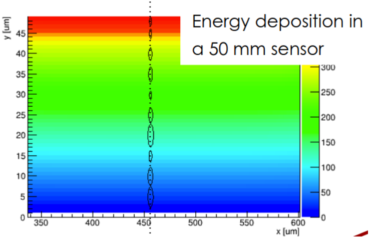
Fast integration

$$\sigma_t = \frac{\sigma_V}{dV/dt} \cong \frac{t_{rise}}{Signal/Noise} \cong \frac{ENC}{I_{Ind}}$$

- fast amplifier, rise-time $\sim$ charge collection time
- LGAD gain $\mathcal{O}(10)$ improves S/N
  unfortunately this gain drops after irradiation
- other electronic noise sources : clock jitter, TDC binning

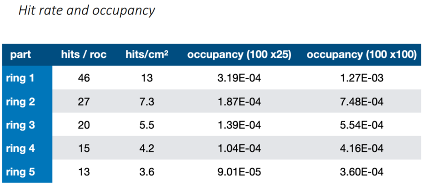
noise contributions : sensor noise

- uniform fields for position independent collection time (parallel plate geometry)
- remaining : arrival time distribution of electrons ('Landau noise')


Energy deposition in a 50 mm sensor

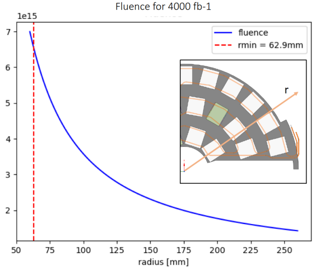
- e.g. 30 ps for 50 µm LGAD, 200 V
  electronics noise must not deteriorate this significantly
- leakage current shot noise probably small (small pixels, cold)

boundary conditions



Hit rate and occupancy

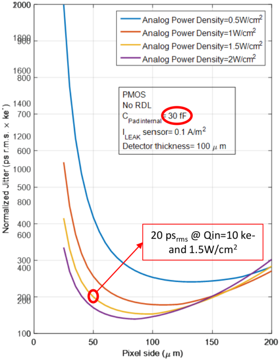
part	hits / roc	hits/cm²	occupancy (100 x25)	occupancy (100 x100)
ring 1	46	13	3.19E-04	1.27E-03
ring 2	27	7.3	1.87E-04	7.48E-04
ring 3	20	5.5	1.39E-04	5.54E-04
ring 4	15	4.2	1.04E-04	4.16E-04
ring 5	13	3.6	9.01E-05	3.60E-04



- TEPX pixel size 50 µm × 50 µm, maybe 100 µm × 100 µm
- fluence : $< 3 \times 10^{15} n_{\mathrm{eq}} \mathrm{cm}^{-2}$, 100 Mrad (innermost part)
- LHC 40 MHz beam structure
- pixel rates up to 500 MHz cm^{-2}
- triggered readout (up to 1 MHz trigger rate,µs latency)

power budget

- CROC : $\sim 1\,\mathrm{W\,cm^{-2}}$ (incl. Shunt LDO), 50% analog
  small increase may be acceptable, but not a large factor
- TimePix4 (65 nm) $0.4\,\mathrm{W\,cm^{-2}}$ analog, 56 ps rms at 10 ke signal
- LHCb/picopix (28 nm) goal 20 ps
  power estimate $\sim 1\,\mathrm{W\,cm^{-2}}$



R.Ballabriga, Fundamental limits to noise and time resolution in highly segmented hybrid pixel detectors: lessons learnt on the Timepix4 design [publication in preparation]

compatibility with TEPX

- large modules/chips preferred
  (TEPX 4 cm × 4 cm sensor , 4 chips)
  CERN/LHCb goes for much smaller chips
- power budget (cooling capacity may be limited, tbd)
- serial powering, up to 10 modules
- control 160 MHz LVDS
- readout 1.28 GHz LVDS
  configurable data-merging

65 nm

- + proven technology, easy access
- + re-use parts of the Phase 2 ASIC?
- - lack of interest, community moving to 28 nm
- - can we achive significantly better timing than Timepix4 with comparable power budget using the same technology?
- - CROC pixel already 100% full, larger pixel size

28 nm

- - no experience yet, cost?
- + possible to keep the pixel size
- + better chance to stay within the power budget
- + 'active' technology in HEP
- + synergies with CERN/LHCb

next steps

- get the design kit
- improve understanding of constraints and limitations
- readout chip for sensor tests (soon)
- sketch a system design for a full chip
- cross our fingers that this turns into an official project