Development of

nanosecond-timescale beam-based feedback systems for single-pass beamlines

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John Adams Institute

Oxford University

Outline

- **Intra-train beam feedback system concept**
- **Designs for ILC + CLIC interaction regions**
- **Prototype hardware development**

  (FONT systems)
- **Other applications**
- **Summary**

Feedback On Nanosecond Timescales

Philip Burrows
Glenn Christian
Javier Resta Lopez
Colin Perry

PhD students:
Douglas Bett
Alexander Gerbershagen
Michael Davis
Neven Blaskovic
Simon Jolly → RAL, UCL
Steve Molloy → SLAC, ESS
Christine Clarke → SLAC
Christina Swinson → BNL
Ben Constance → CERN
Robert Apsimon → CERN

Valencia, CERN, DESY, KEK, SLAC

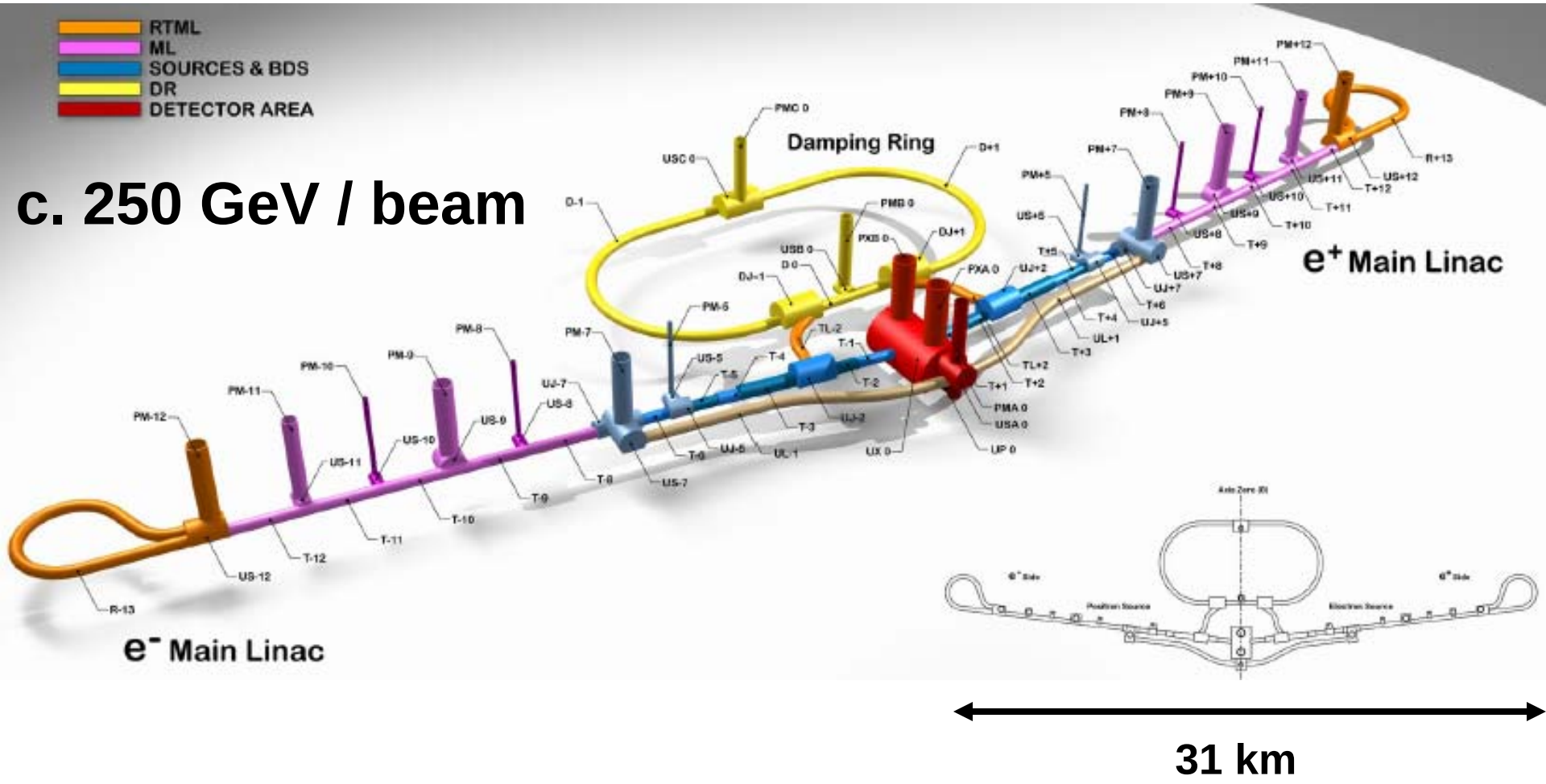
Next-generation e+e- collider

- **Exploitation machine for new physics revealed at LHC, eg. 'Higgs boson factory'**
- **International Linear Collider (ILC)**

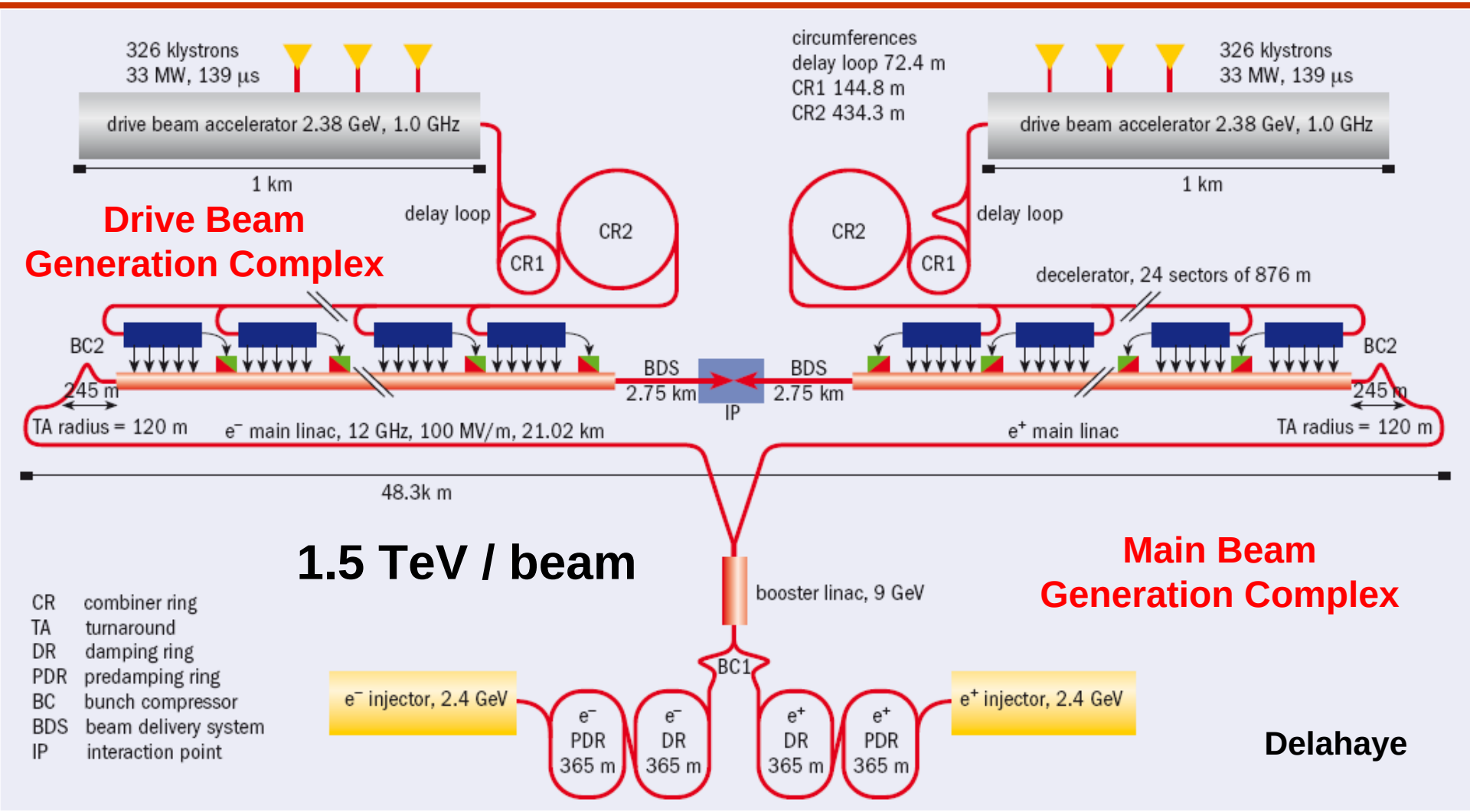
  500 – 1000 GeV
- **Compact Linear Collider (CLIC)**

  3000 GeV (500 → 5000 GeV?)
- **Laser and beam-driven concepts for TeV-scale colliders based on plasmas**

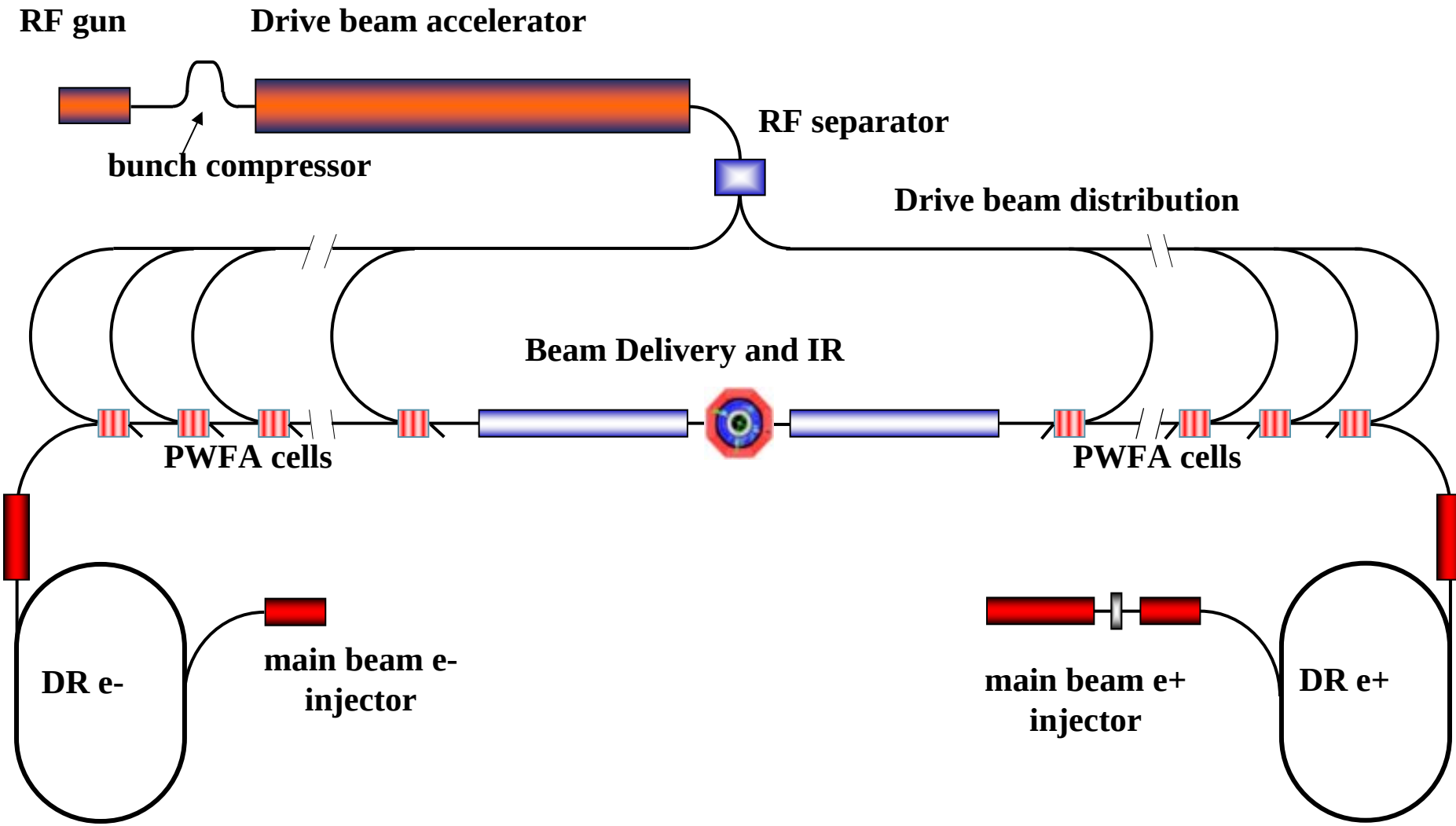
International Linear Collider



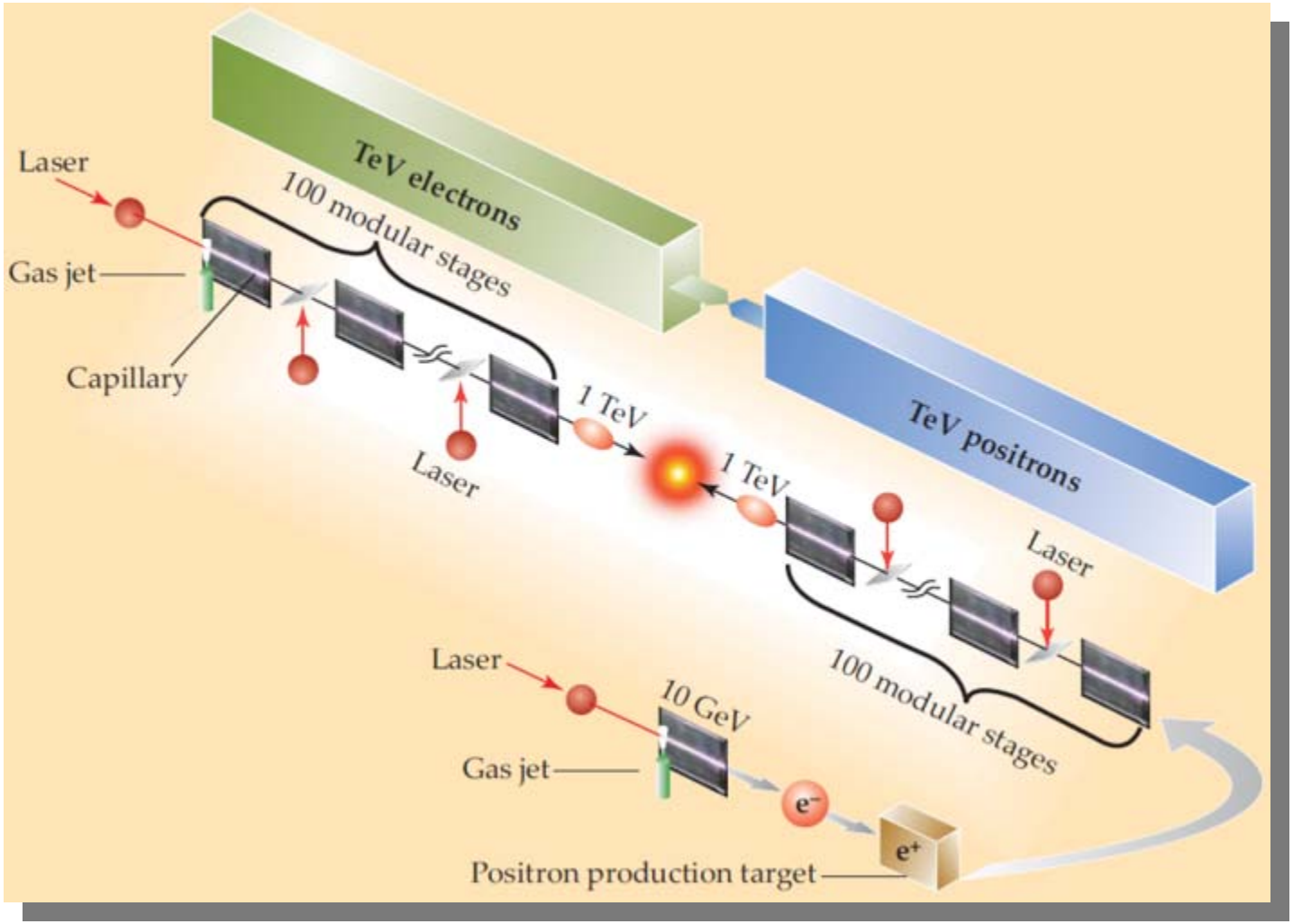
Compact Linear Collider (CLIC)



Concept for beam-driven Plasma Wake Field TeV Linear Collider



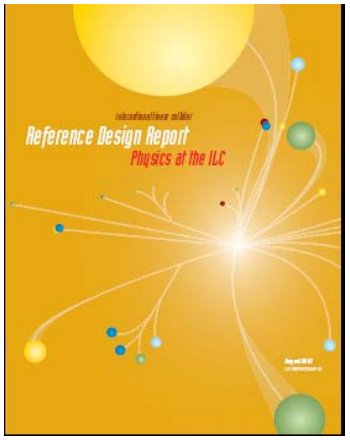
Concept of TeV e+e- collider based on laser-plasma acceleration



Wim Leemans and Eric Esarey, Physics Today, March 2009

ILC Reference Design Report (Feb 2007)

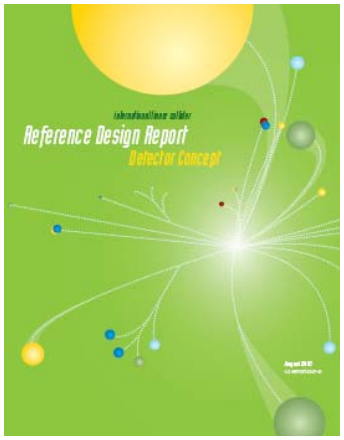
Executive Summary



Physics at the ILC

700 authors, 84 institutes

Accelerator



Detectors

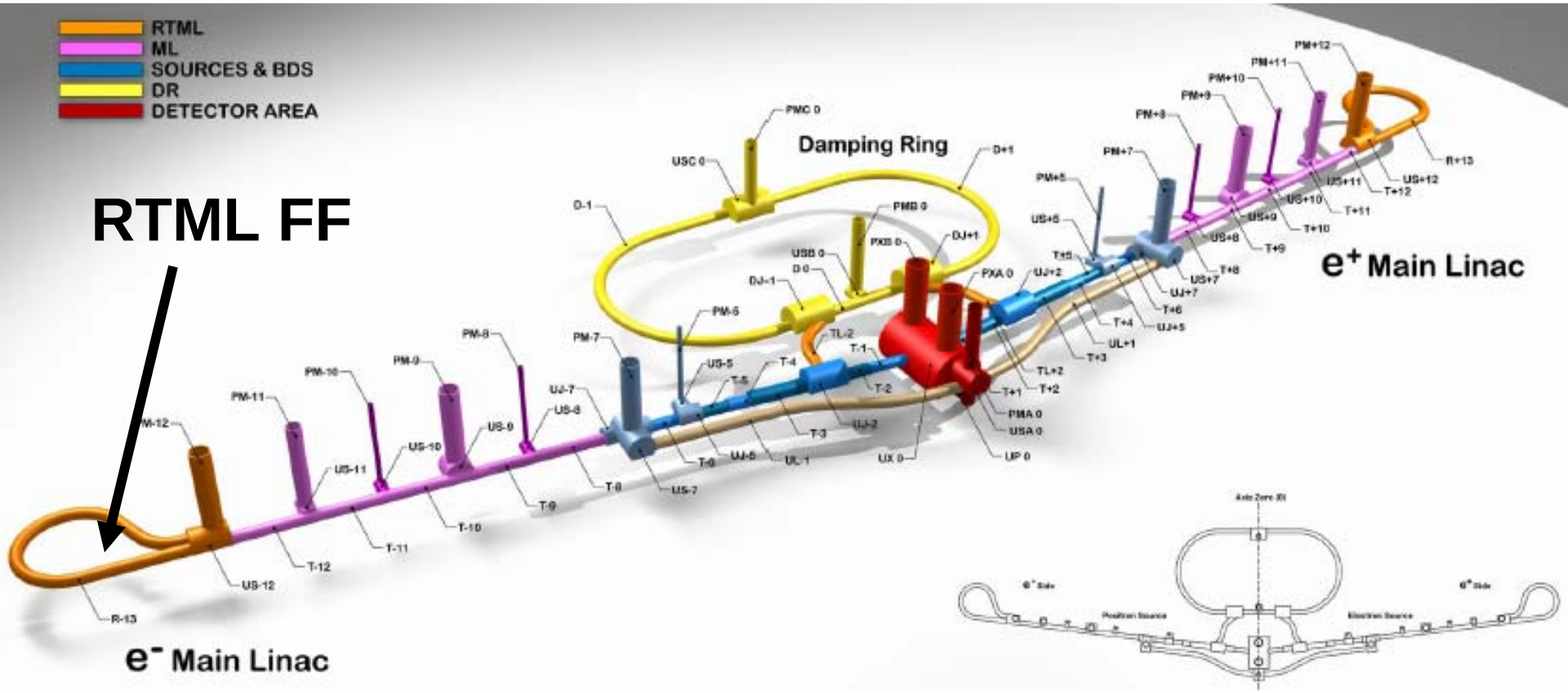
Feedback On Nanosecond Timescales

- **Intra-train feedback systems for ILC and CLIC**

Feedback On Nanosecond Timescales

- **Intra-train feedback systems for ILC and CLIC**
- **Ring-Linac feed-forward: correct for DR extraction**

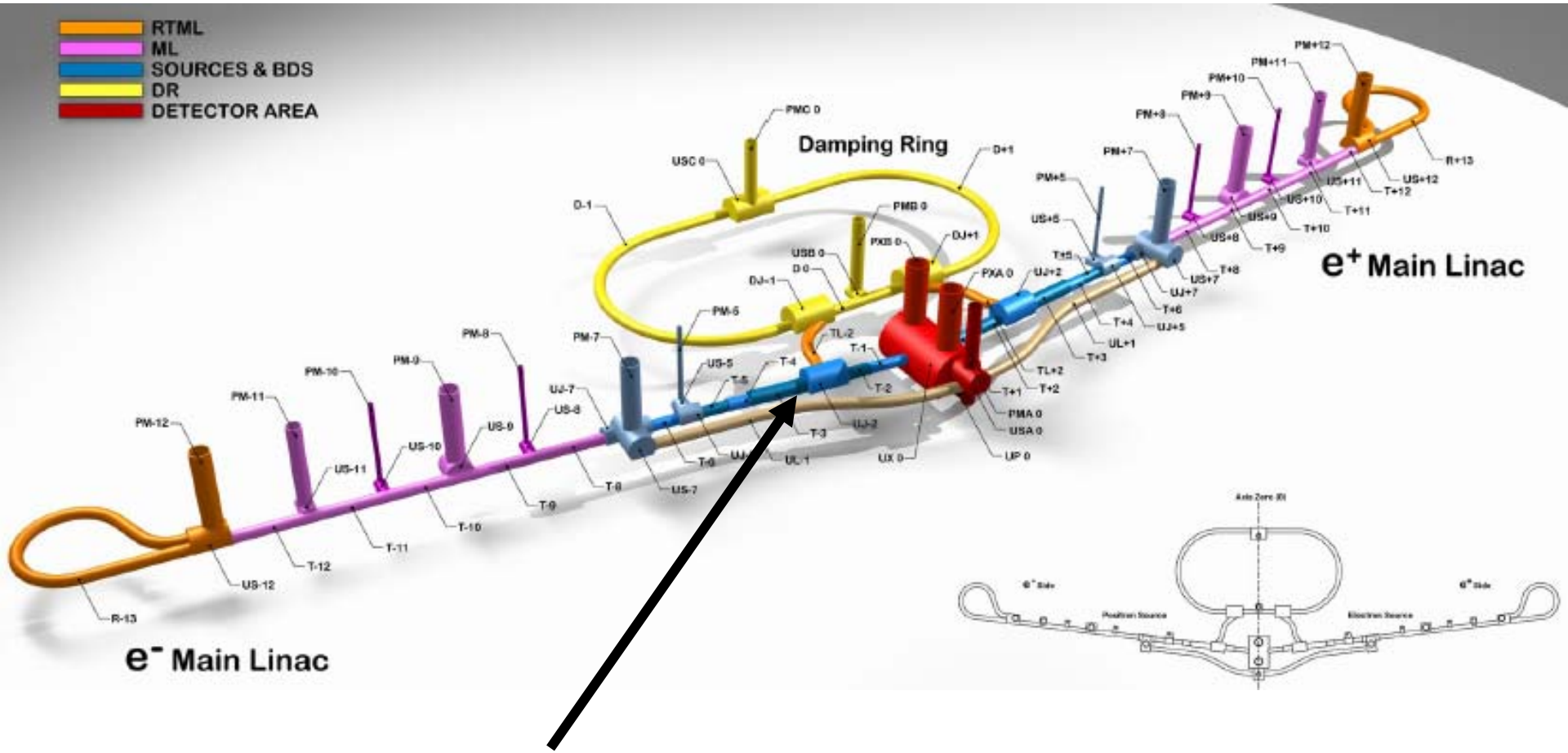
International Linear Collider



Feedback On Nanosecond Timescales

- **Intra-train feedback systems for ILC and CLIC**
- **Ring-Linac feed-forward: correct for DR extraction**
- **End of linac ‘train-straightener’**

International Linear Collider

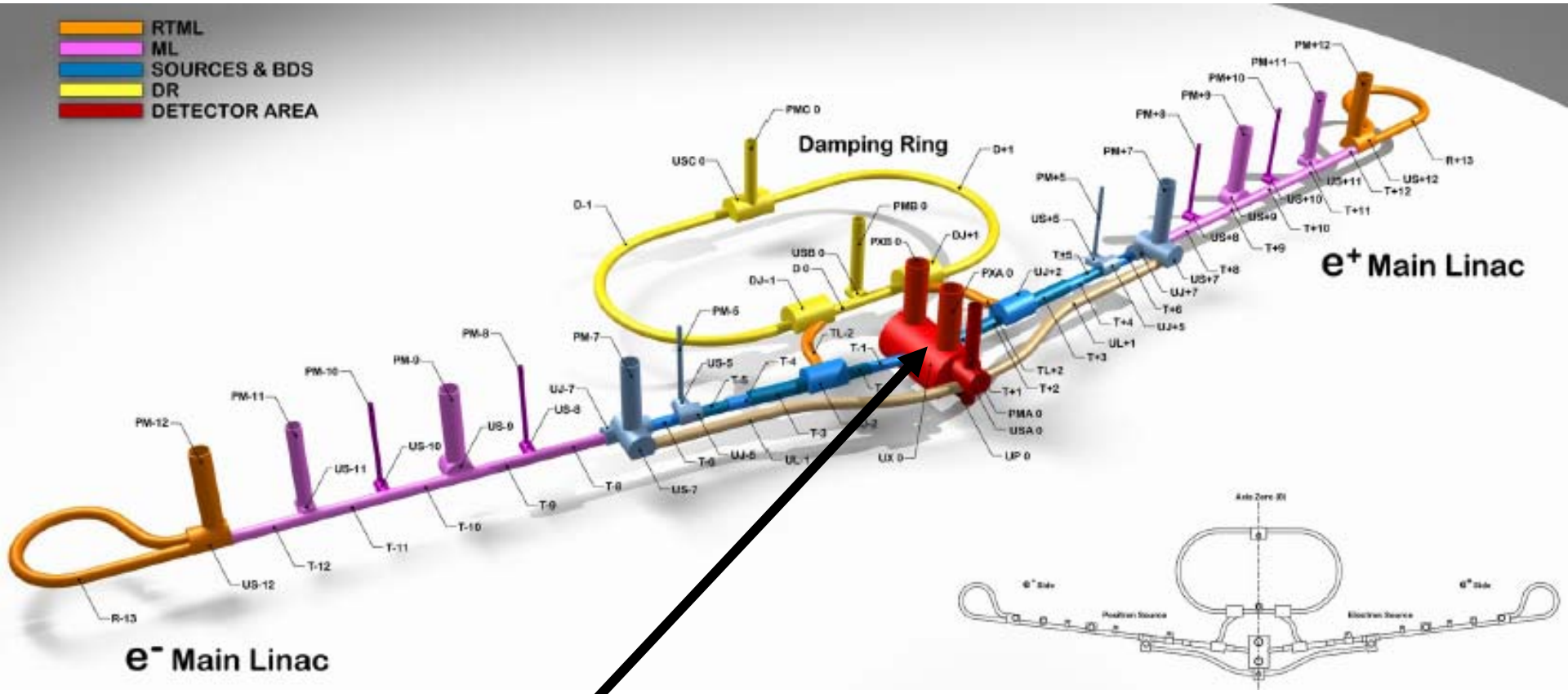


End of linac FB

Feedback On Nanosecond Timescales

- **Intra-train feedback systems for ILC and CLIC**
- **Ring-linac feed-forward: correct for DR extraction**
- **End of linac ‘train-straightener’**
- **Interaction point: collision feedback**

International Linear Collider

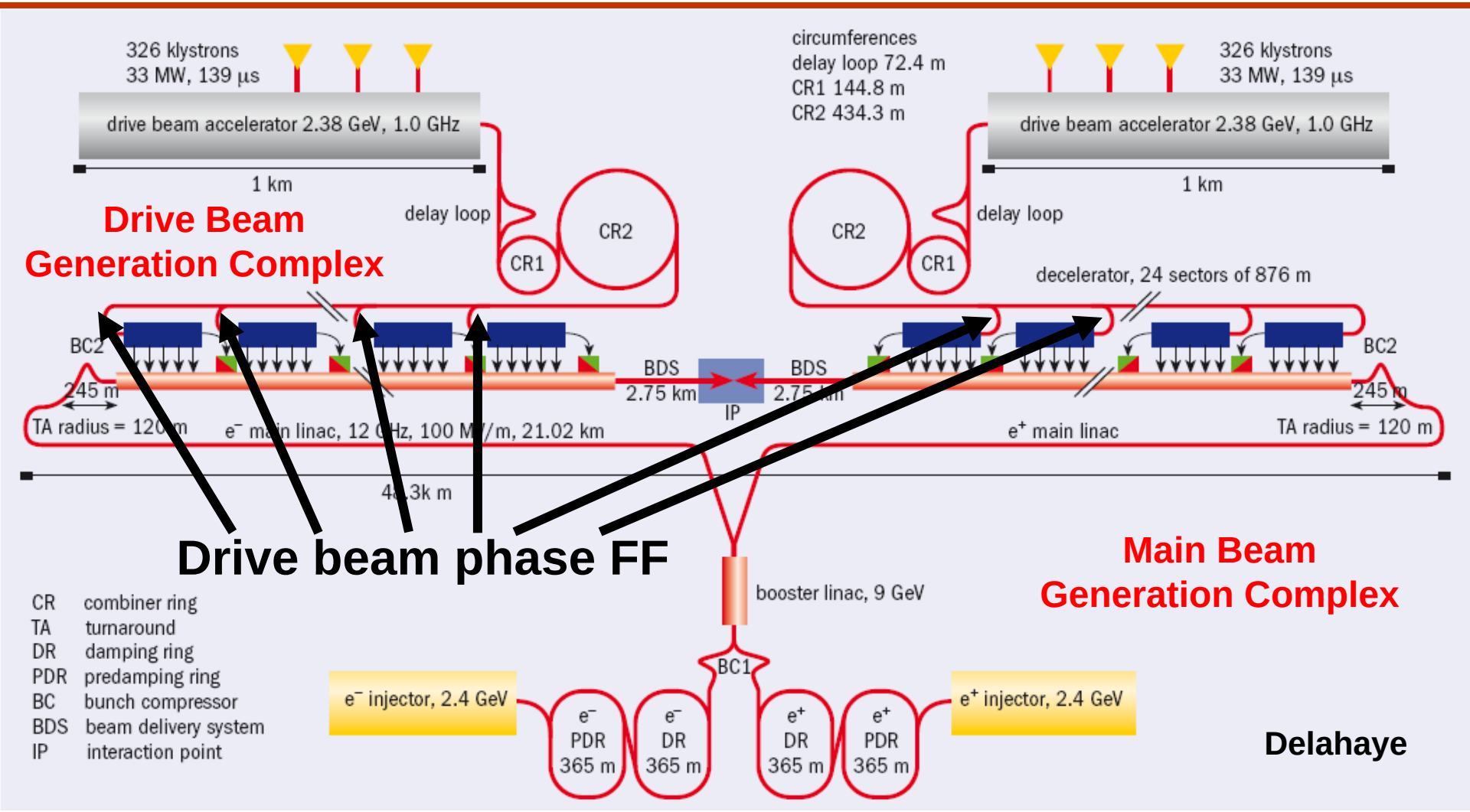


Collision FB

Feedback On Nanosecond Timescales

- **Intra-train feedback systems for ILC and CLIC**
- **Ring-linac feed-forward: correct for DR extraction**
- **End of linac ‘train-straightener’**
- **Interaction point: collision feedback**
- **CLIC drive beam phase feed-forward**

Compact Linear Collider (CLIC)



Beam parameters

	ILC (500)	CLIC (3 TeV)	
Electrons/bunch	0.75	0.37	10**10
Bunches/train	2820	312	
Train repetition rate	5	50	Hz
Bunch separation	308	0.5	ns
Train length	868	0.156	us
Horizontal IP beam size	655	45	nm
Vertical IP beam size	6	0.9	nm
Longitudinal IP beam size	300	45	um
Luminosity	2	6	10**34

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Feedback On Nanosecond Timescales

- **Intra-train feedback systems for ILC and CLIC**
- **Ring-linac feed-forward: correct for DR extraction**
- **End of linac ‘train-straightener’**
- **Interaction point: collision feedback**
- **CLIC drive beam phase feed-forward**

→ **Must operate with latency**

O(10ns) (CLIC) and O(100ns) ILC

Luminosity

$$L = f_{rep} n_b \frac{N^2}{\pi \sigma_x \sigma_y}$$

N	**number of particles in each bunch**
n_b	**number of bunches per beam**
f_rep	**repetition frequency of bunches**
sigma_x *	
sigma_y	**transverse area of bunches**

→ Number passing per unit time per unit area ('flux')

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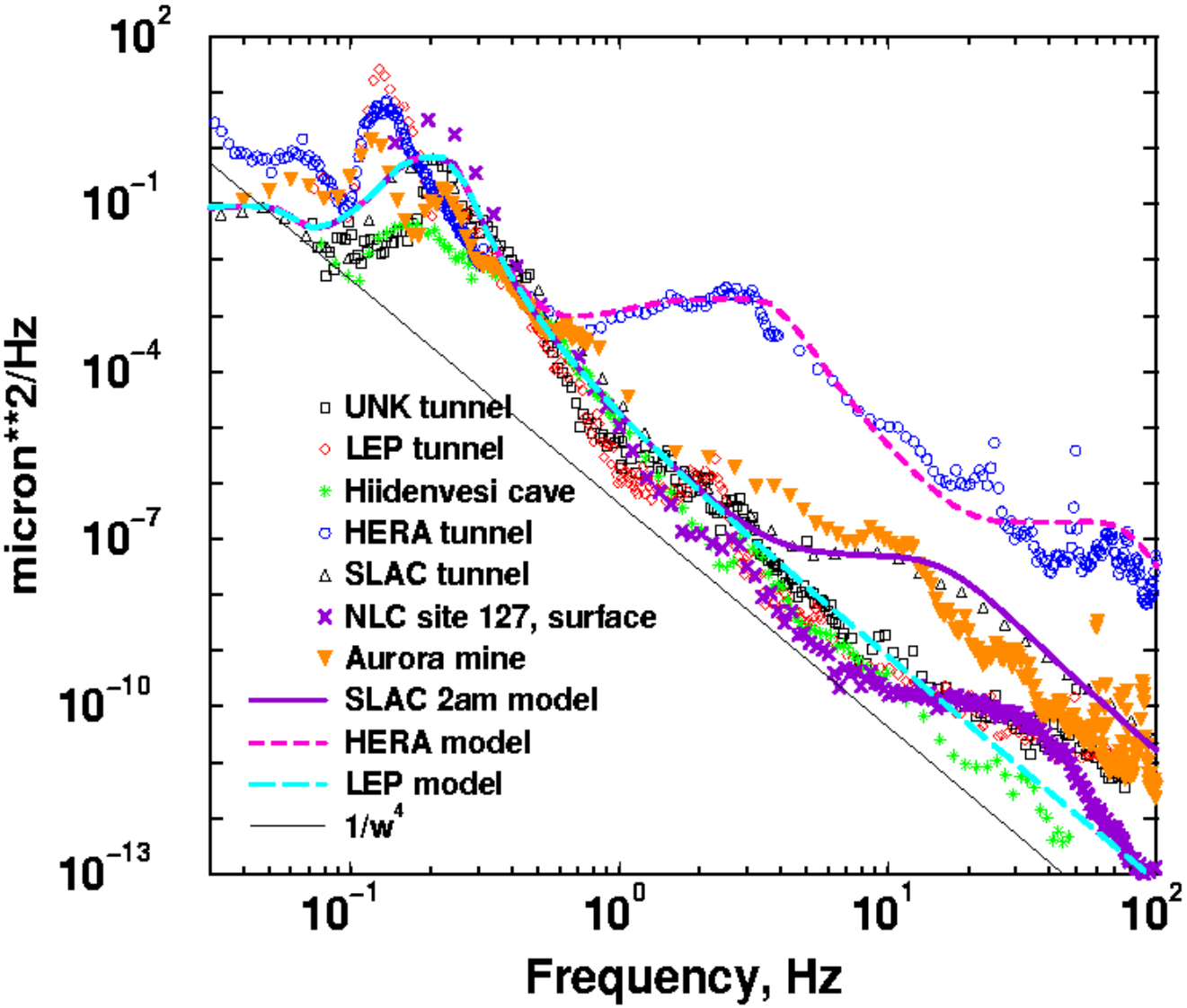
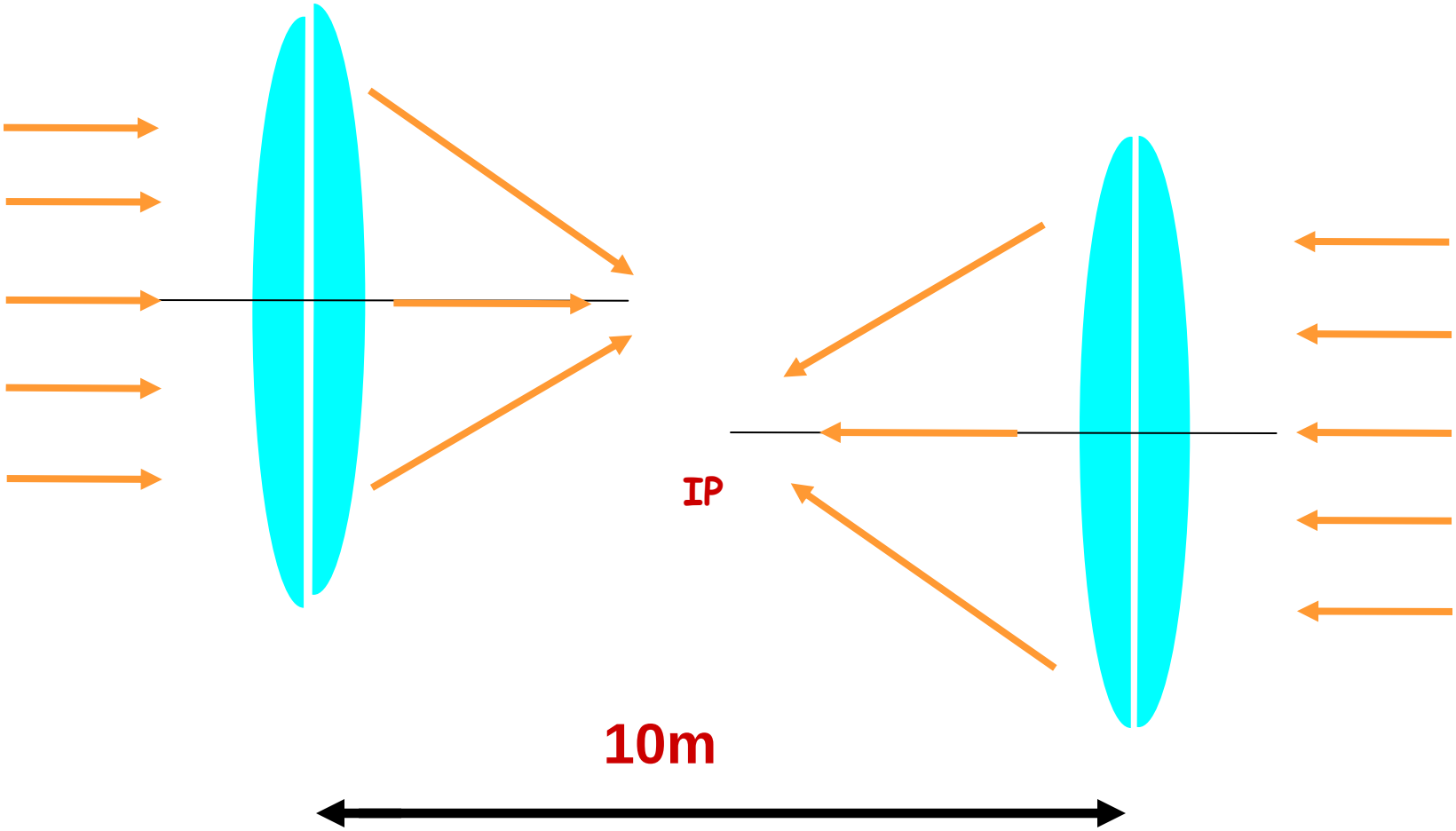
Ground motion measurements



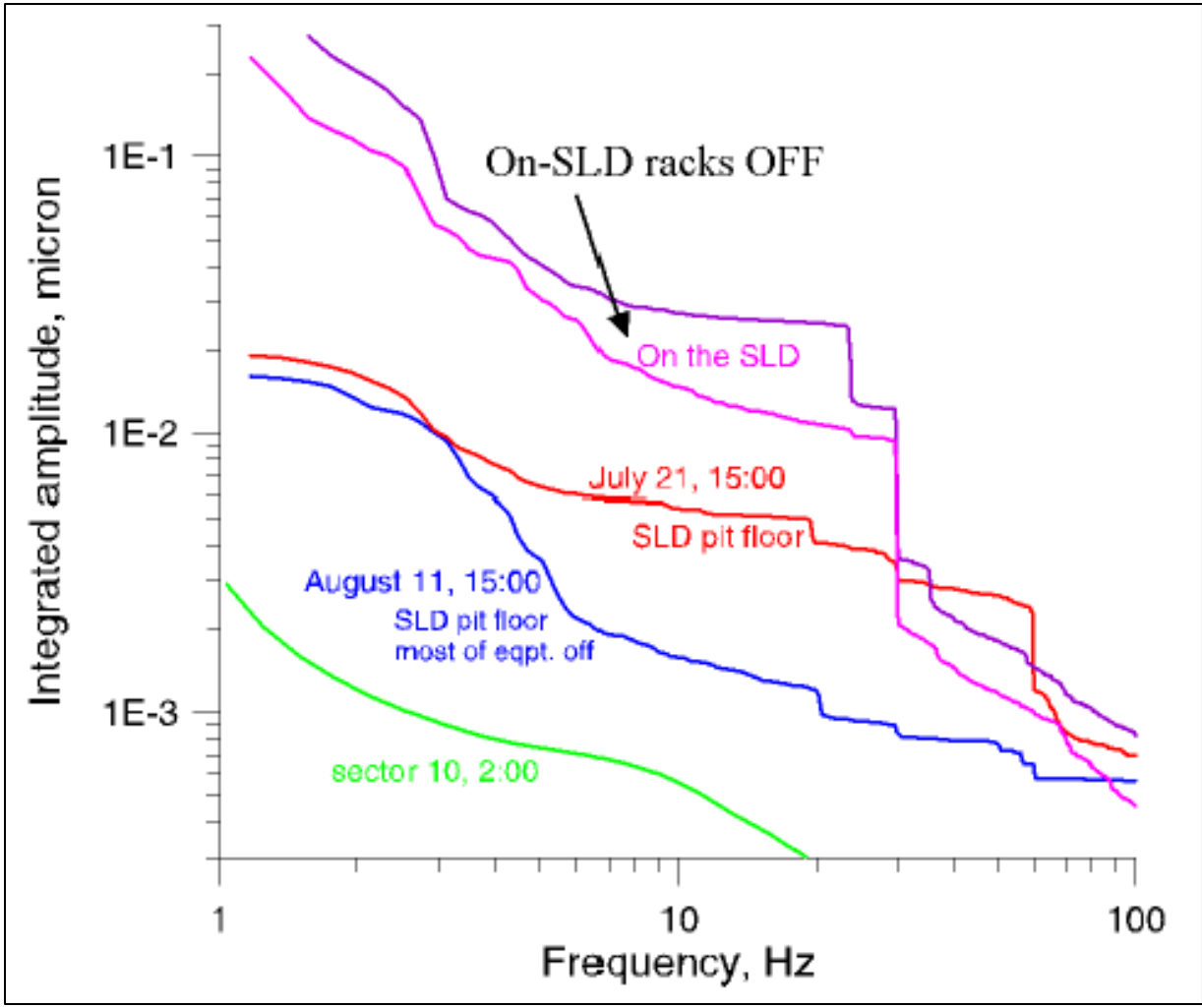
Vibrations of Final Focus



SLAC Linear Collider (SLC)

Data from SLAC

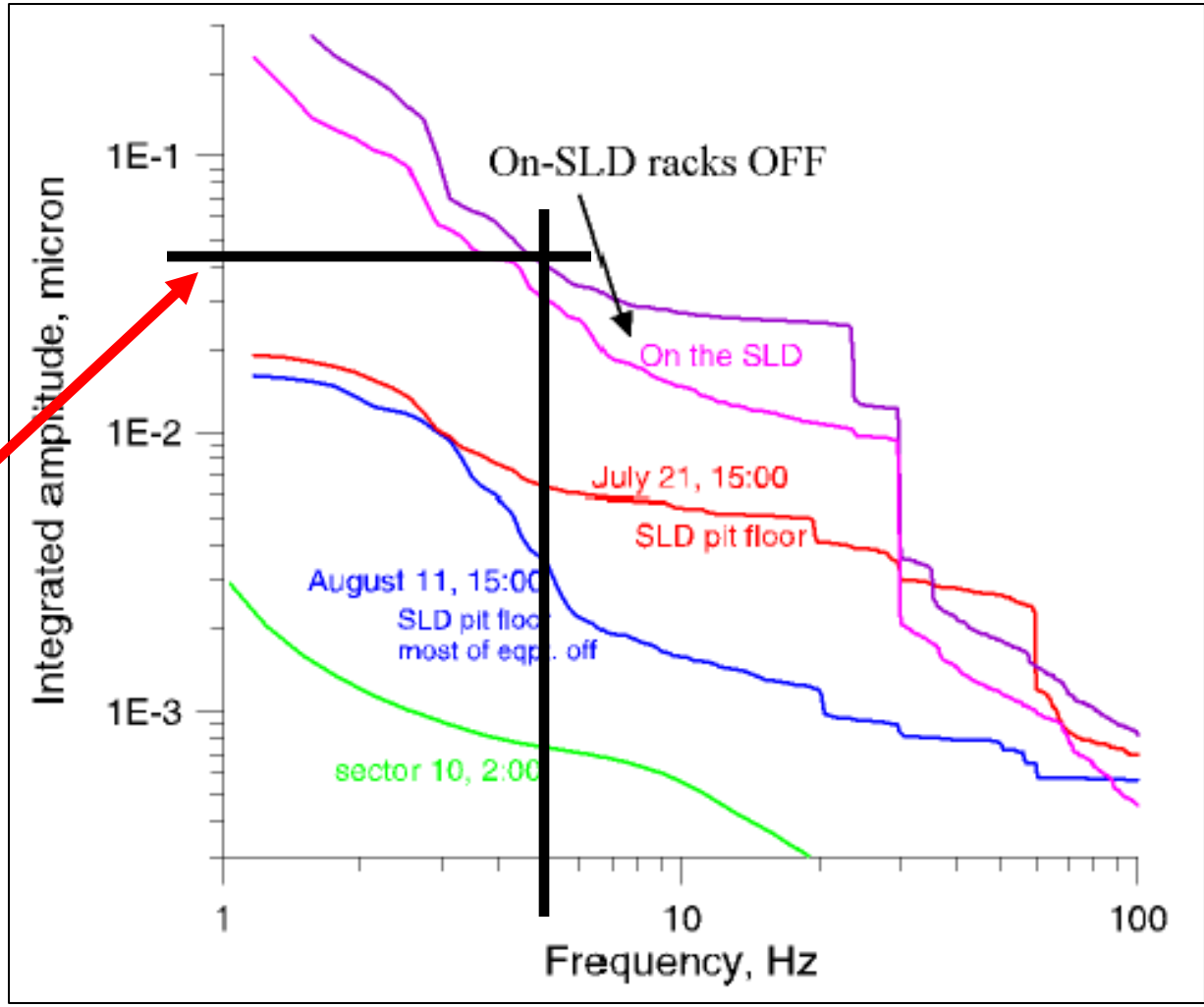
Integrated vertical r.m.s. motion between 2 points 10m apart, vs frequency



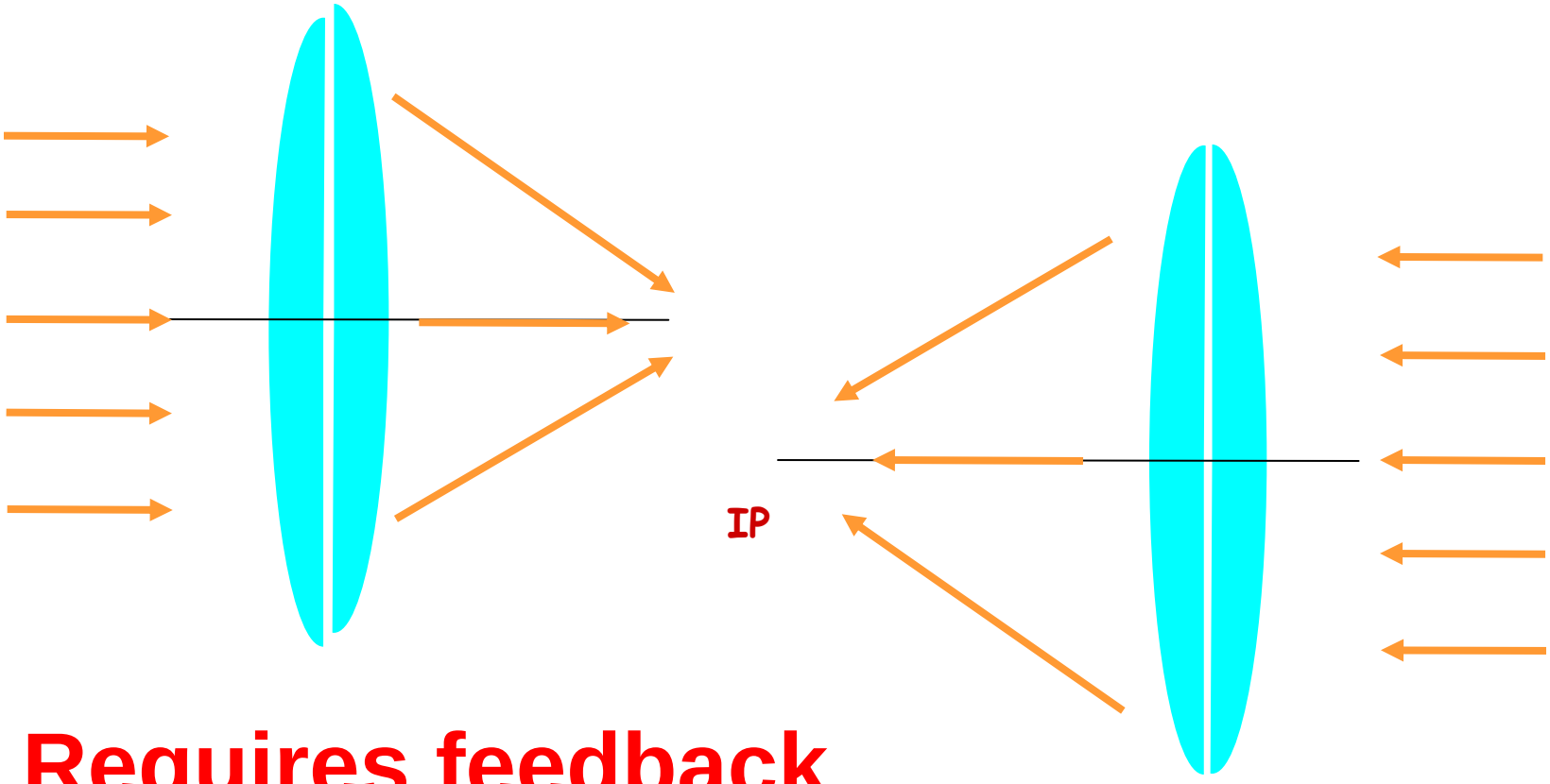
Data from SLAC

Integrated vertical r.m.s. motion between 2 points 10m apart, vs frequency

10 – 100 nanometres



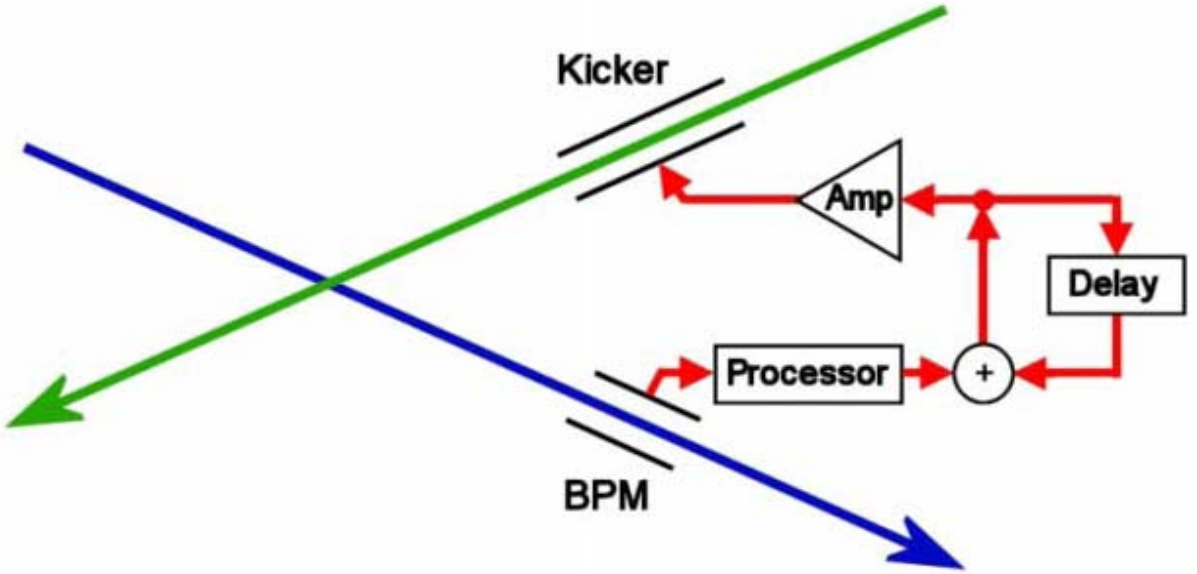
Vibrations of Final Focus



Requires feedback

LC intra-train feedback system - concept

- Last line of defence against relative beam misalignment
- Measure vertical position of outgoing beam and hence beam-beam kick angle
- Use fast amplifier and kicker to correct vertical position of beam incoming to IR



FONT – Feedback On Nanosecond Timescales

General considerations (1)

Collision optimisation – based on beam-beam deflection:

1. Interaction point position feedback:

- hardware located near IP
- kicker at 90 degrees w.r.t. IP

2. Interaction point angle feedback:

- hardware ideally located near IP
- kicker in phase w.r.t. IP

3. Additional (feed-forward) inputs:

- information from alignment systems (eg. QD0 etc.)
- information about beam from upstream in machine (eg. DR)

Luminosity optimisation – based on measured luminosity:

- fast luminosity signal (from BEAMCAL)

General considerations (2)

Time structure of bunch train:

ILC (500 GeV): c. 3000 bunches w. c. 300 ns separation

CLIC (3 TeV): c. 300 bunches w. c. 0.5 ns separation

Feedback latency:

ILC: O(100ns) latency budget allows digital approach

CLIC: O(10ns) latency requires analogue approach

Recall speed of light: c = 30 cm / ns:

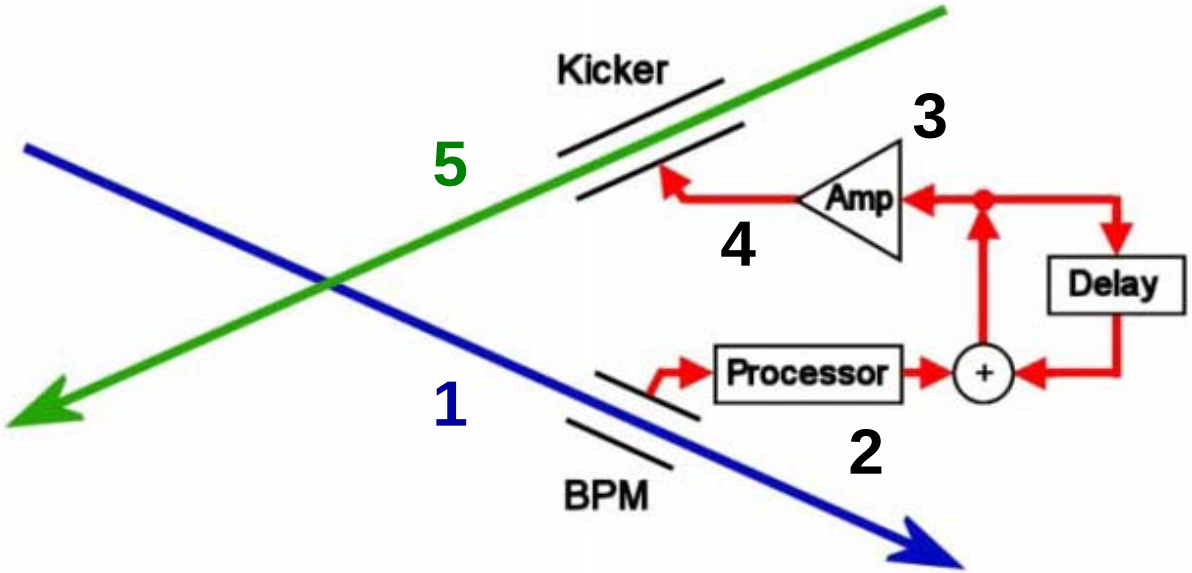
FB hardware should be close to IP (especially for CLIC!)

Two systems, one on each side of IP, allow for redundancy

IP position feedback latency

Latency:

1. Beam flight time IP → BPM
2. Signal processing, FB calculation
3. Amplifier + kicker response time
4. Cable delays
5. Beam flight time kicker → IP



IP FB Design Status: ILC

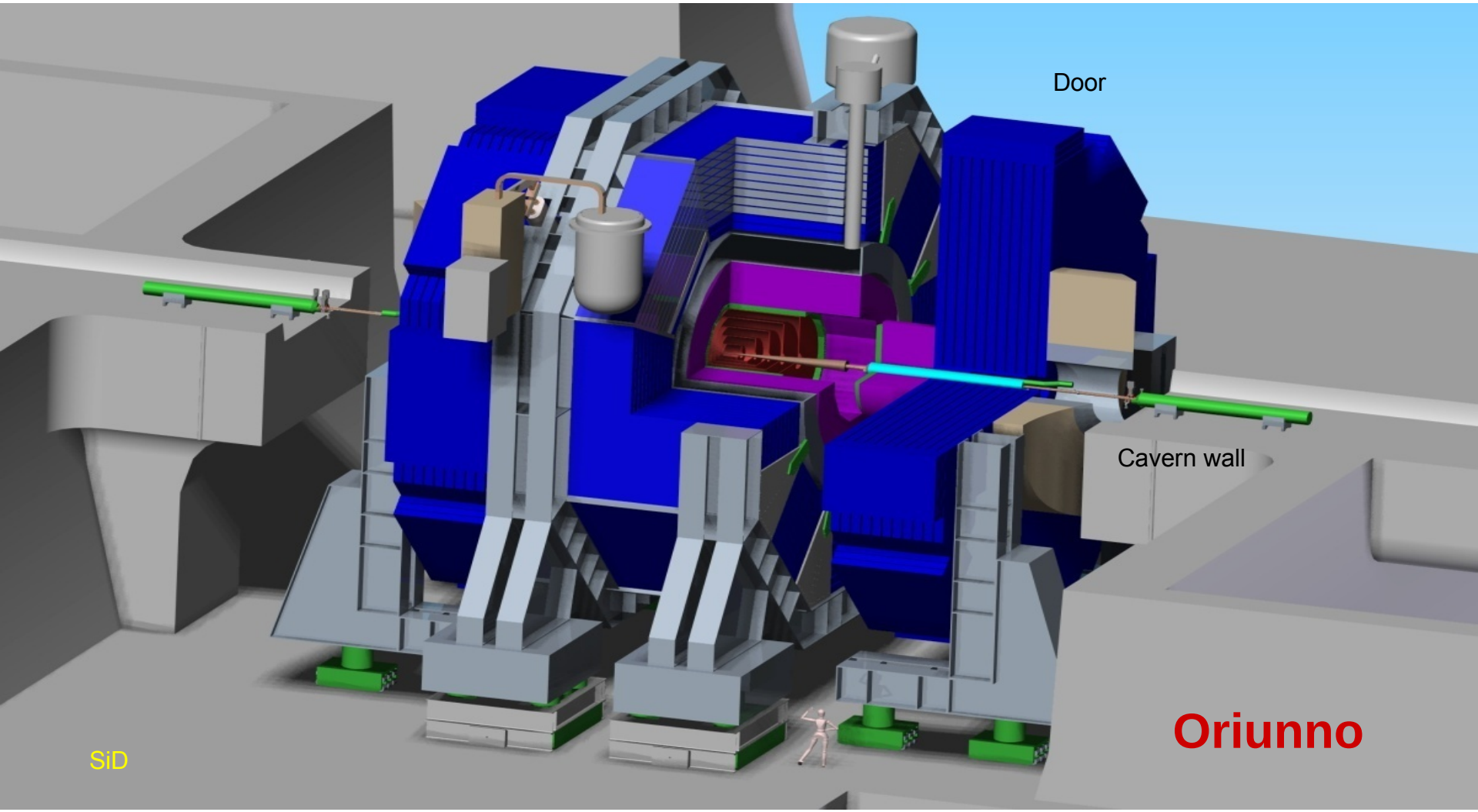
Conceptual design documented in ILC RDR (2007), fleshed out since:

1. IP position feedback:
provide IP beam position correction at +- 50 sigma_y level
i.e. +- 300 nm of vertical beam motion at IP
2. IP angle feedback: hardware located few 100 metres upstream
conceptually very similar to position FB, (arguably) less critical
3. Bunch-by-bunch luminosity signal (from BEAMCAL)

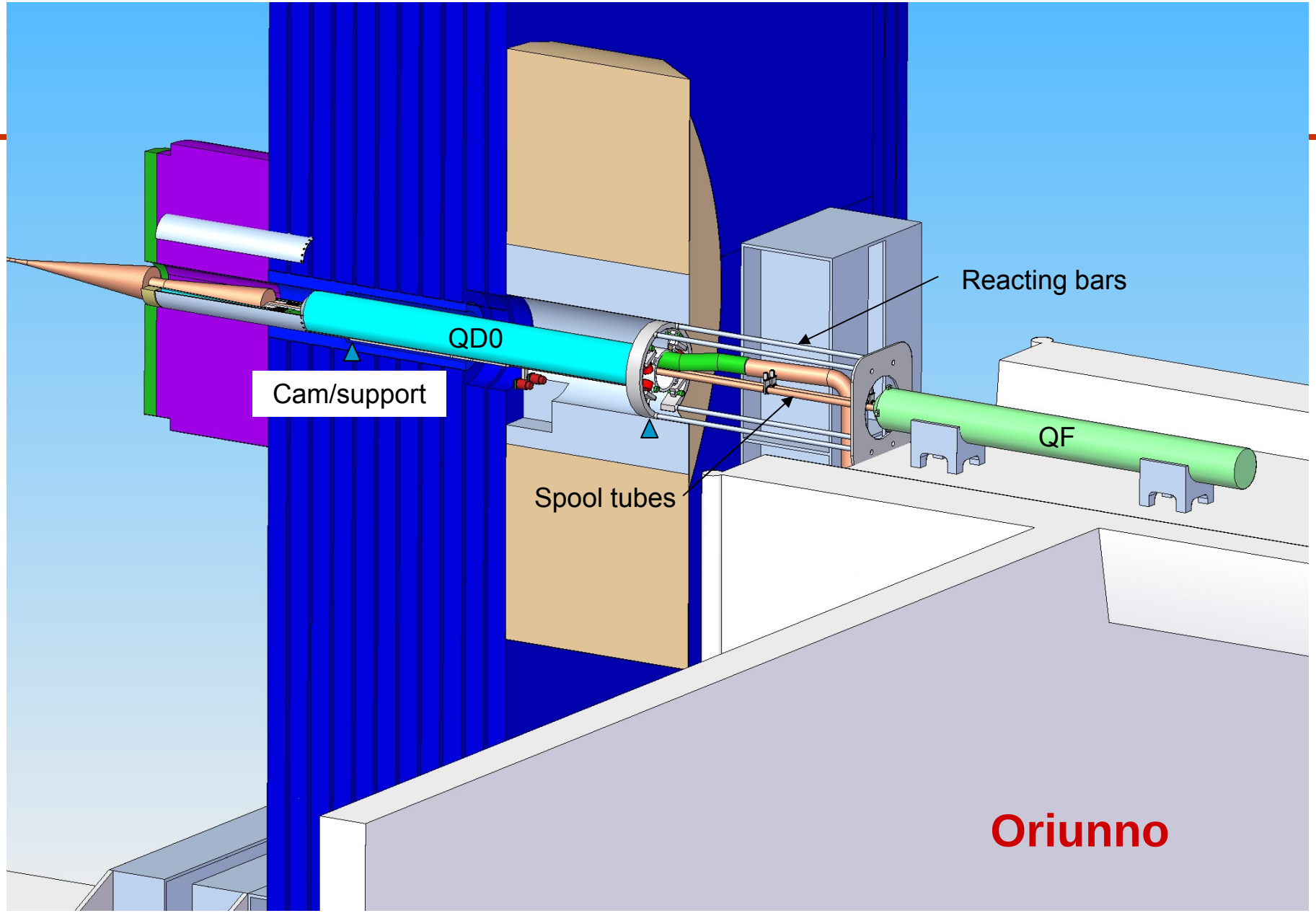
'special' systems requiring dedicated hardware + data links

More realistic engineering design now in progress for TDP document (2012)

ILC IR: SiD for illustration



Final Doublet Region (SiD for illustration)



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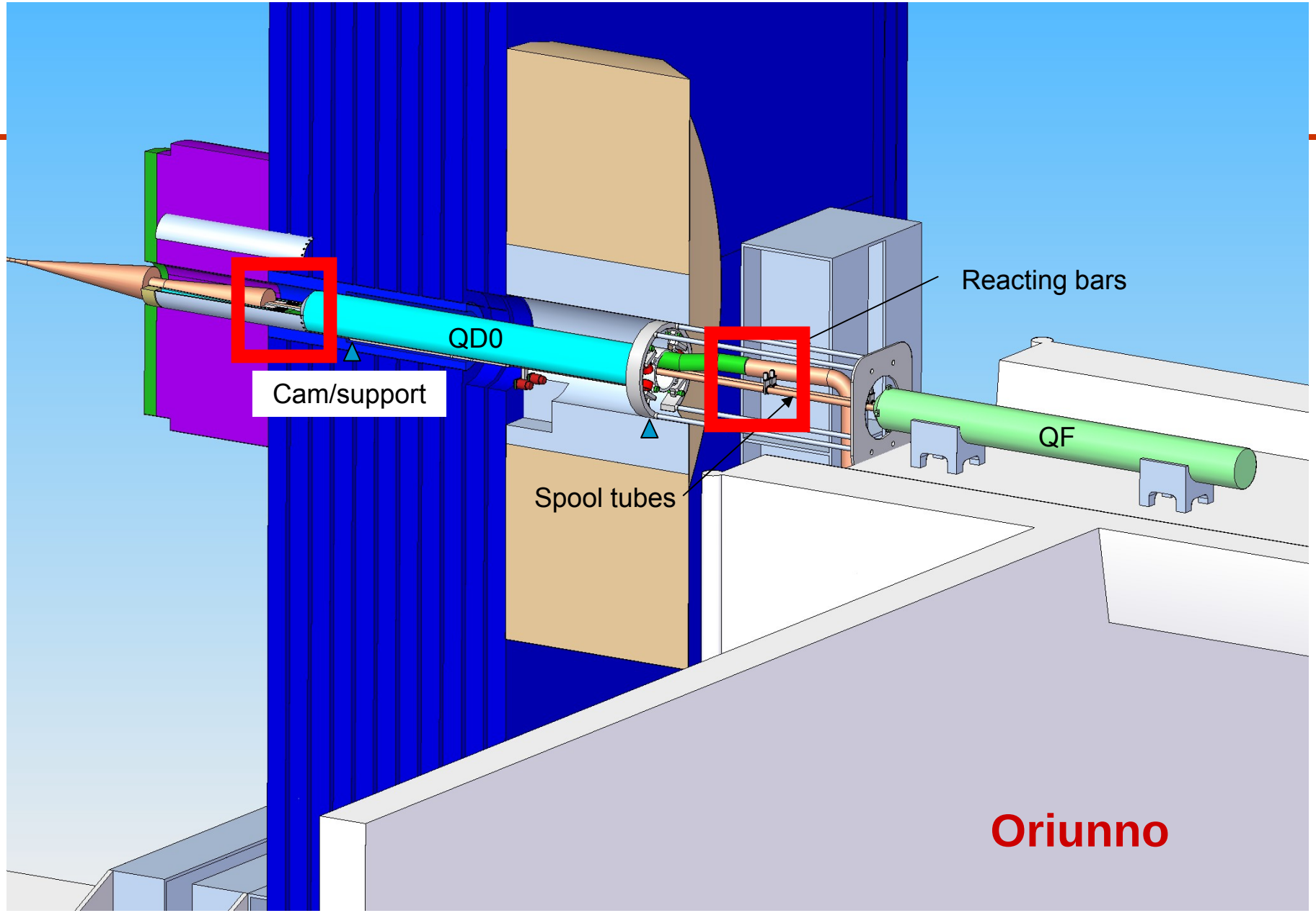
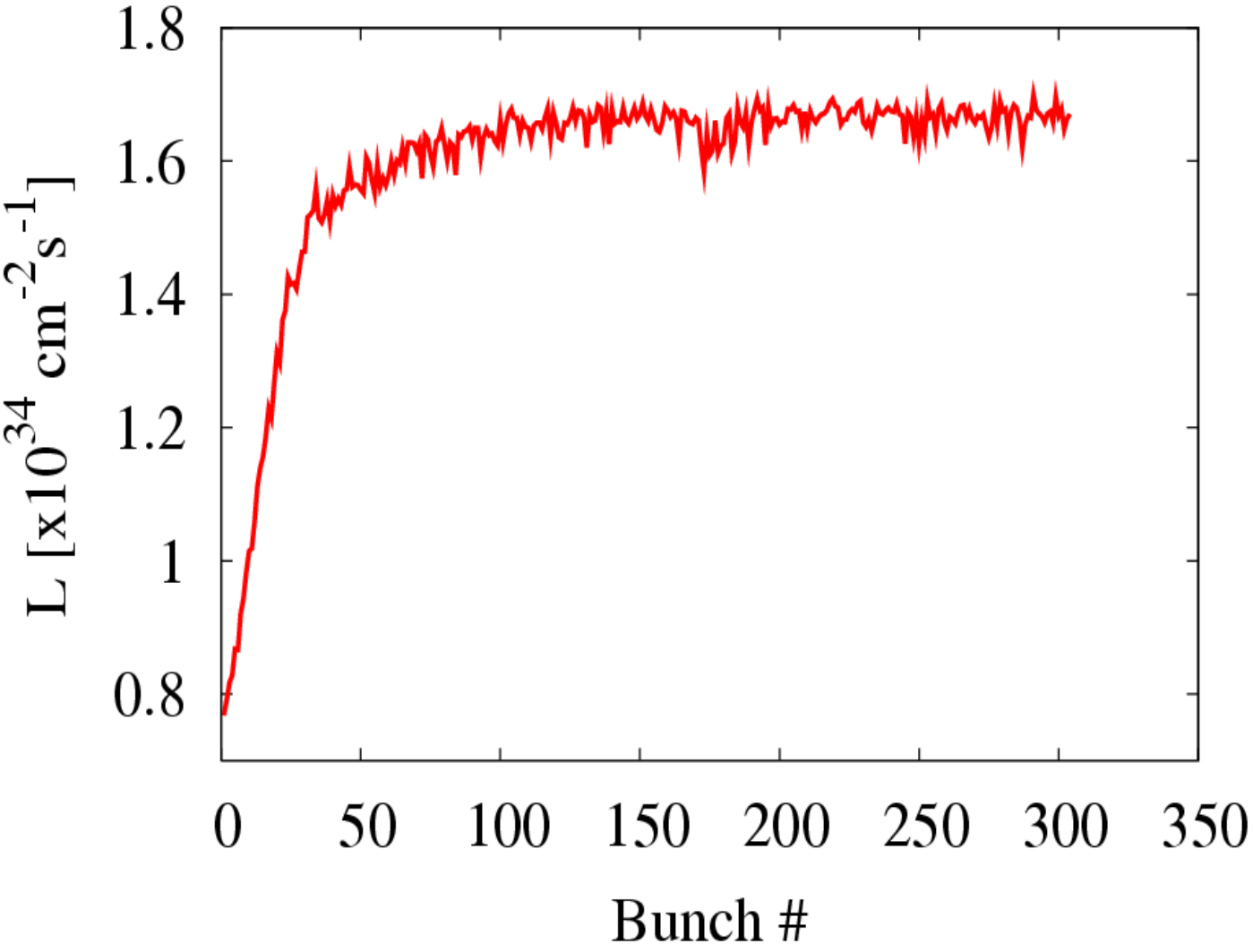
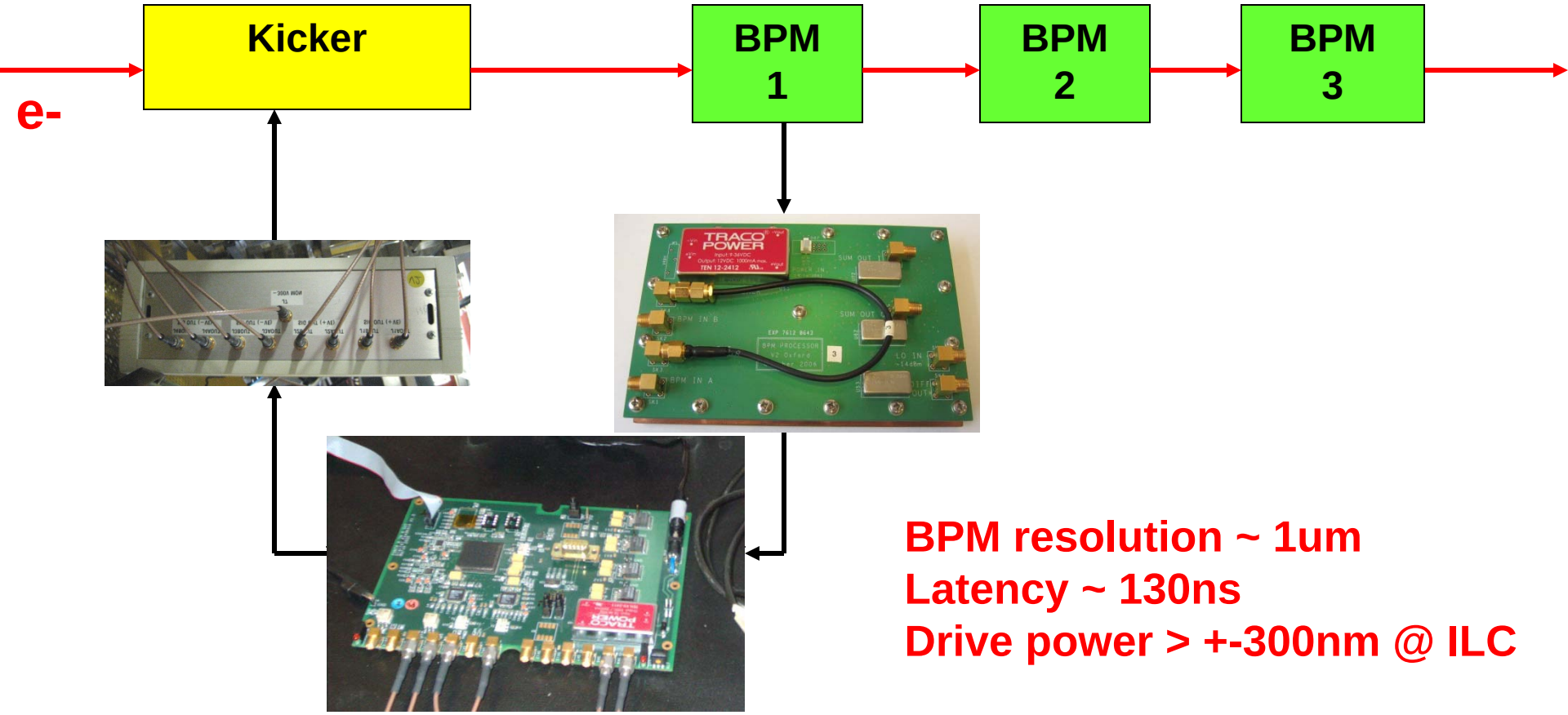


ILC IP intra-train FB performance



ILC prototype: FONT4 at KEK/ATF



BPM resolution ~ 1um
Latency ~ 130ns
Drive power > +-300nm @ ILC

IP FB Design Status: CLIC

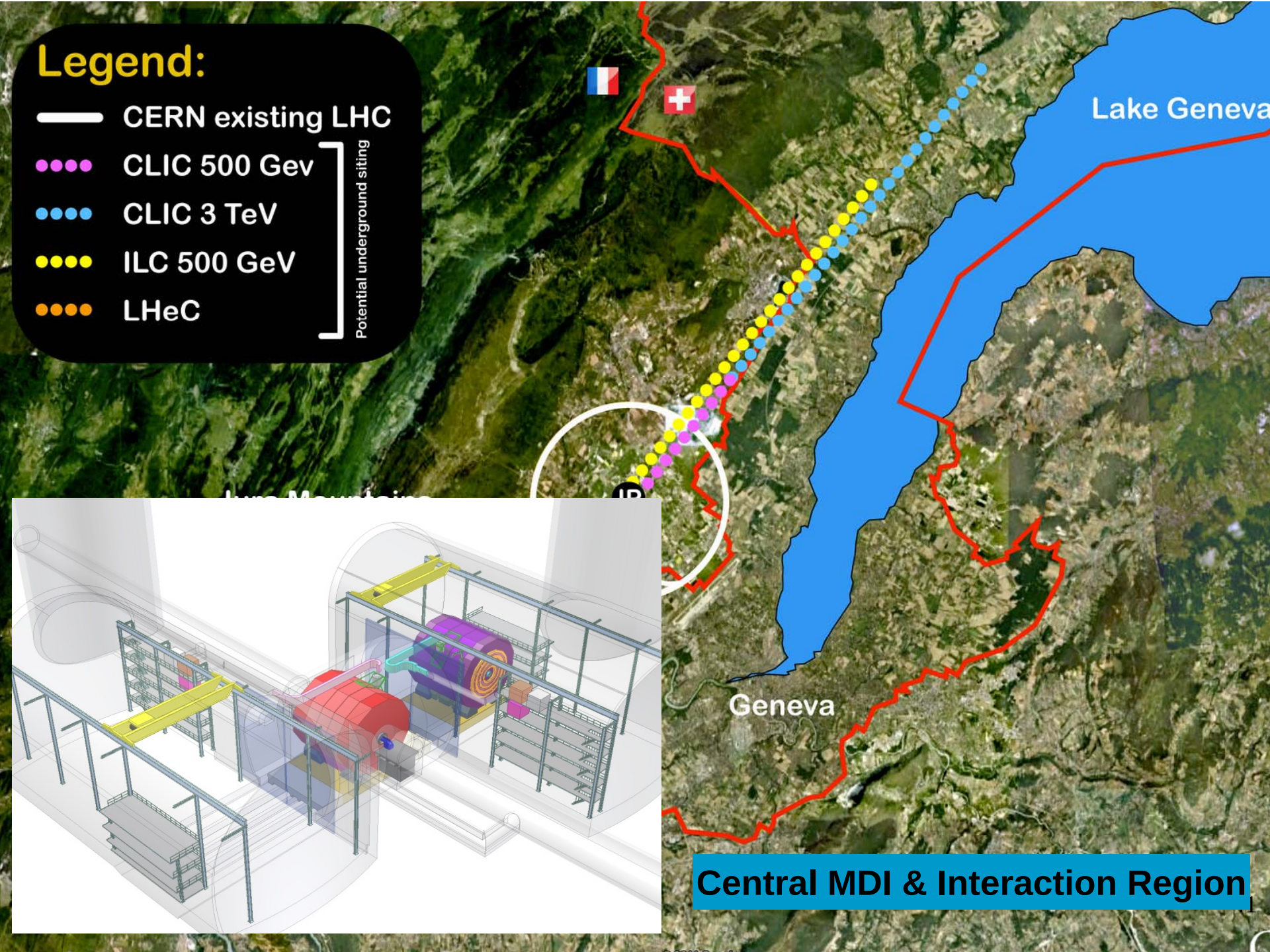
Conceptual design developed and documented in CLIC CDR (2011)

NB primary method for control of beam collision overlap is via vibration isolation of the FF magnets, and dynamic correction of residual component motions

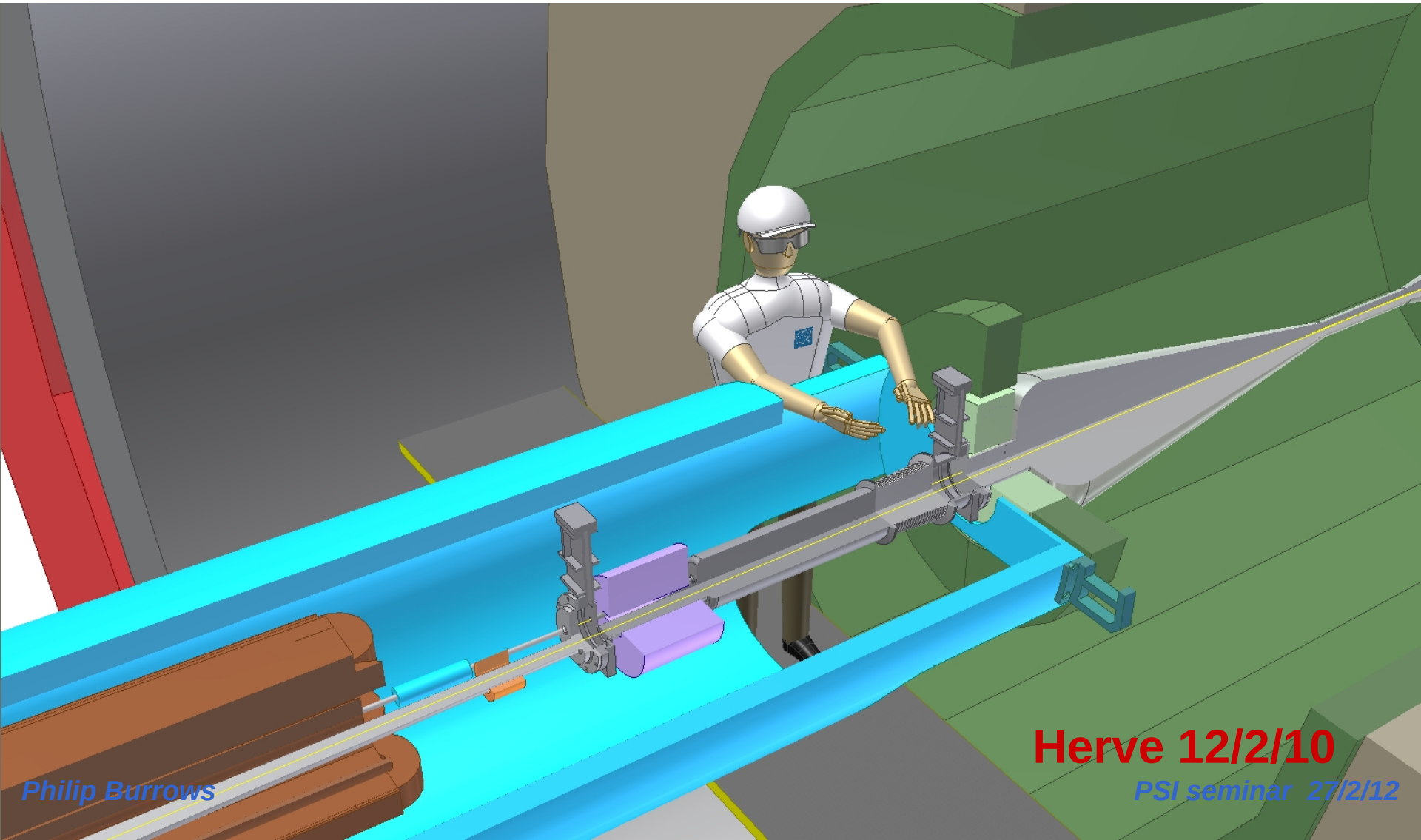
IP position feedback:

provide IP beam position correction of +- 50 nm of vertical beam motion

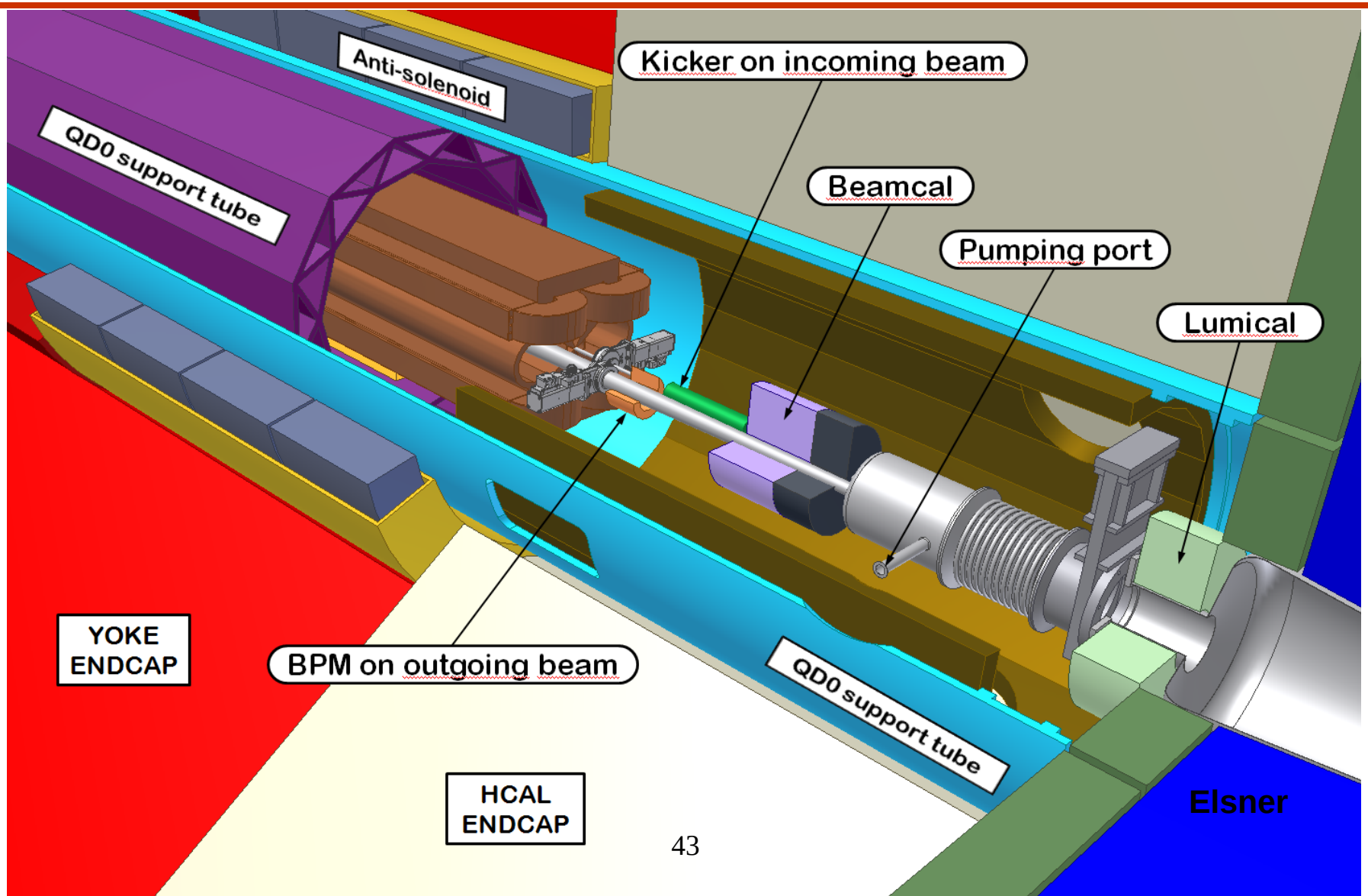
More realistic engineering design can be developed in next project phase


Legend:
CERN existing LHC
CLIC 500 Gev
CLIC 3 TeV
ILC 500 GeV
LHeC
Potential underground siting
Lake Geneva
Geneva
Central MDI & Interaction Region

CLIC: zoom-in to QD0



CLIC Final Doublet region



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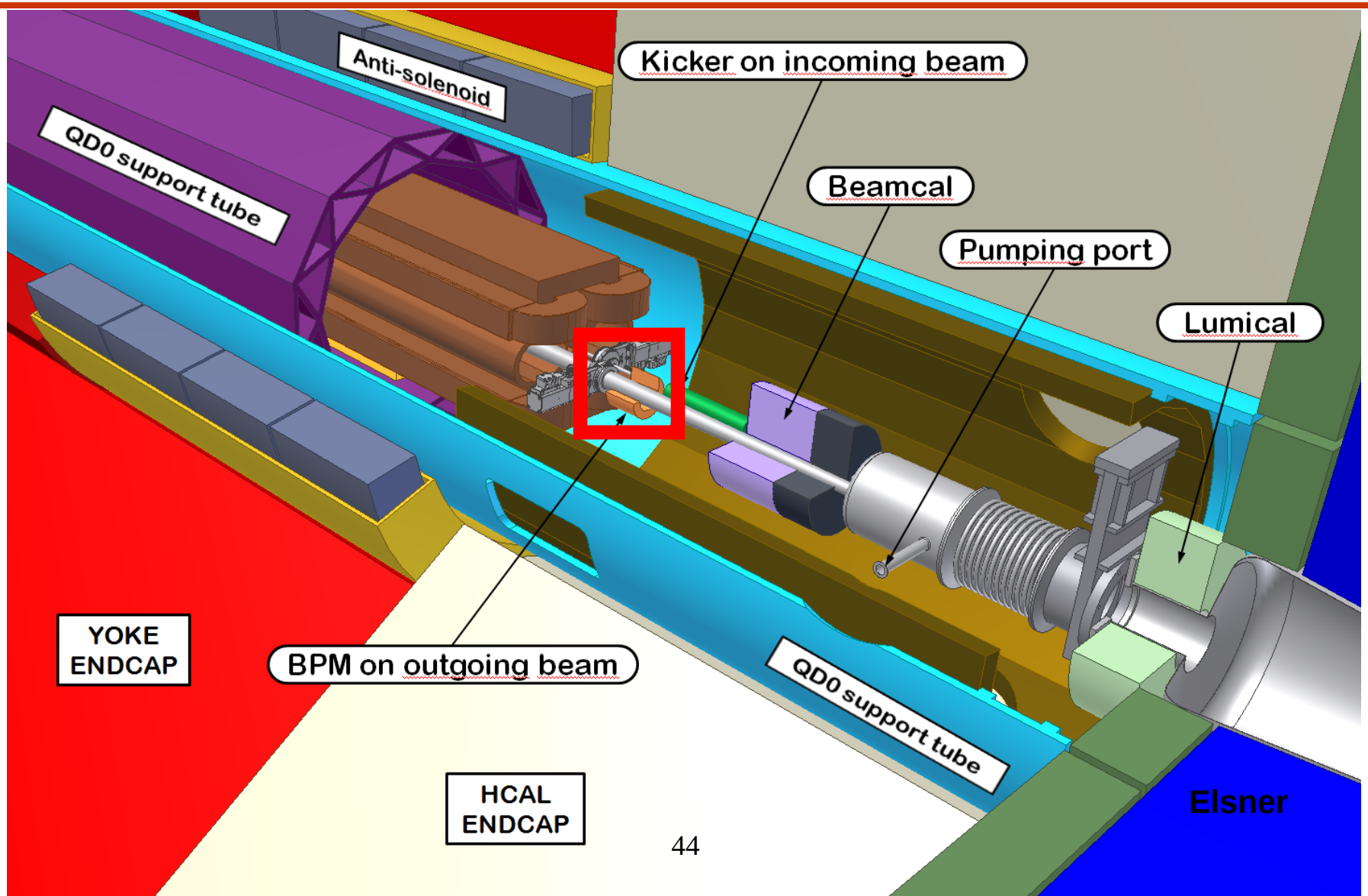

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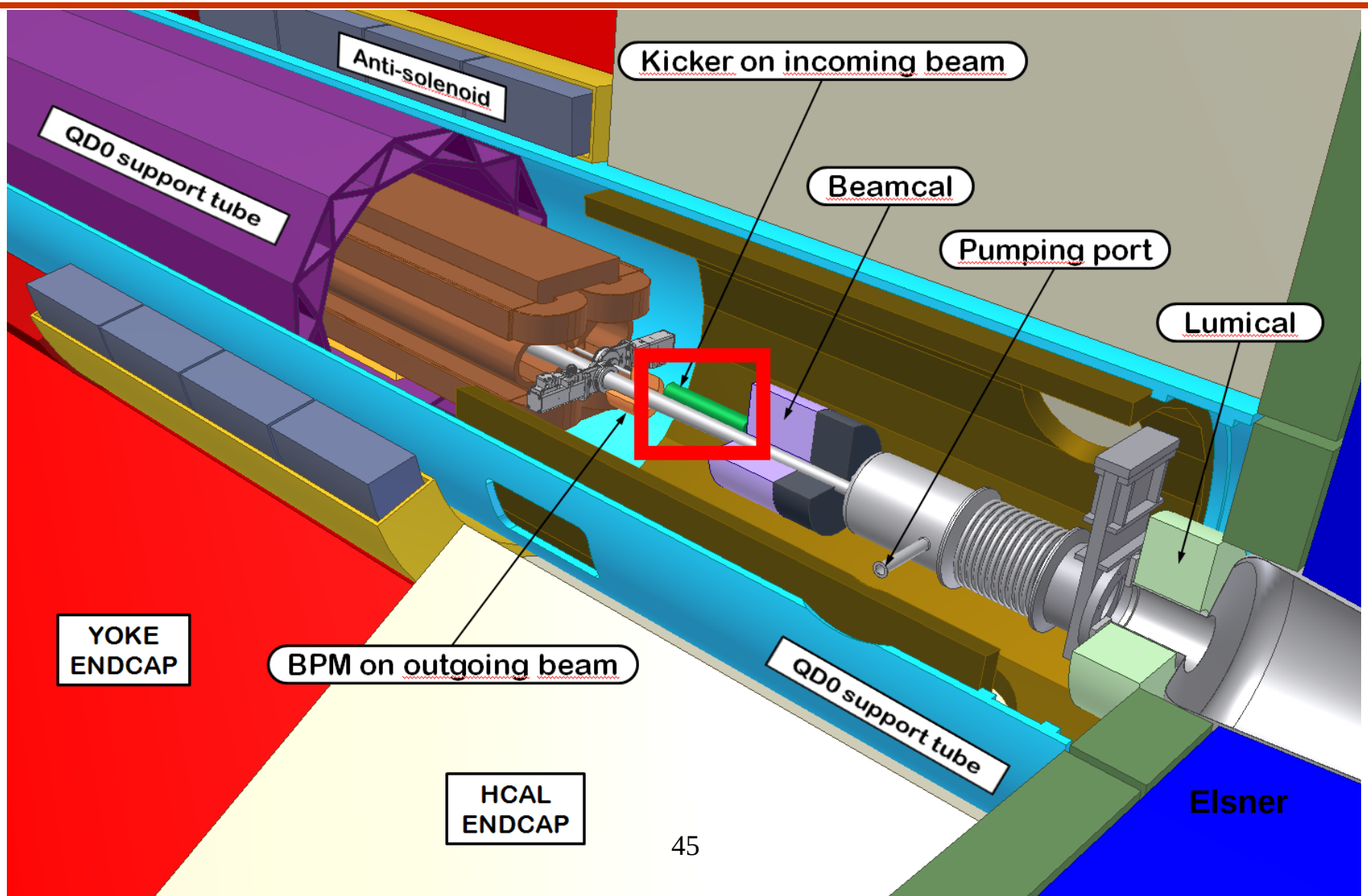
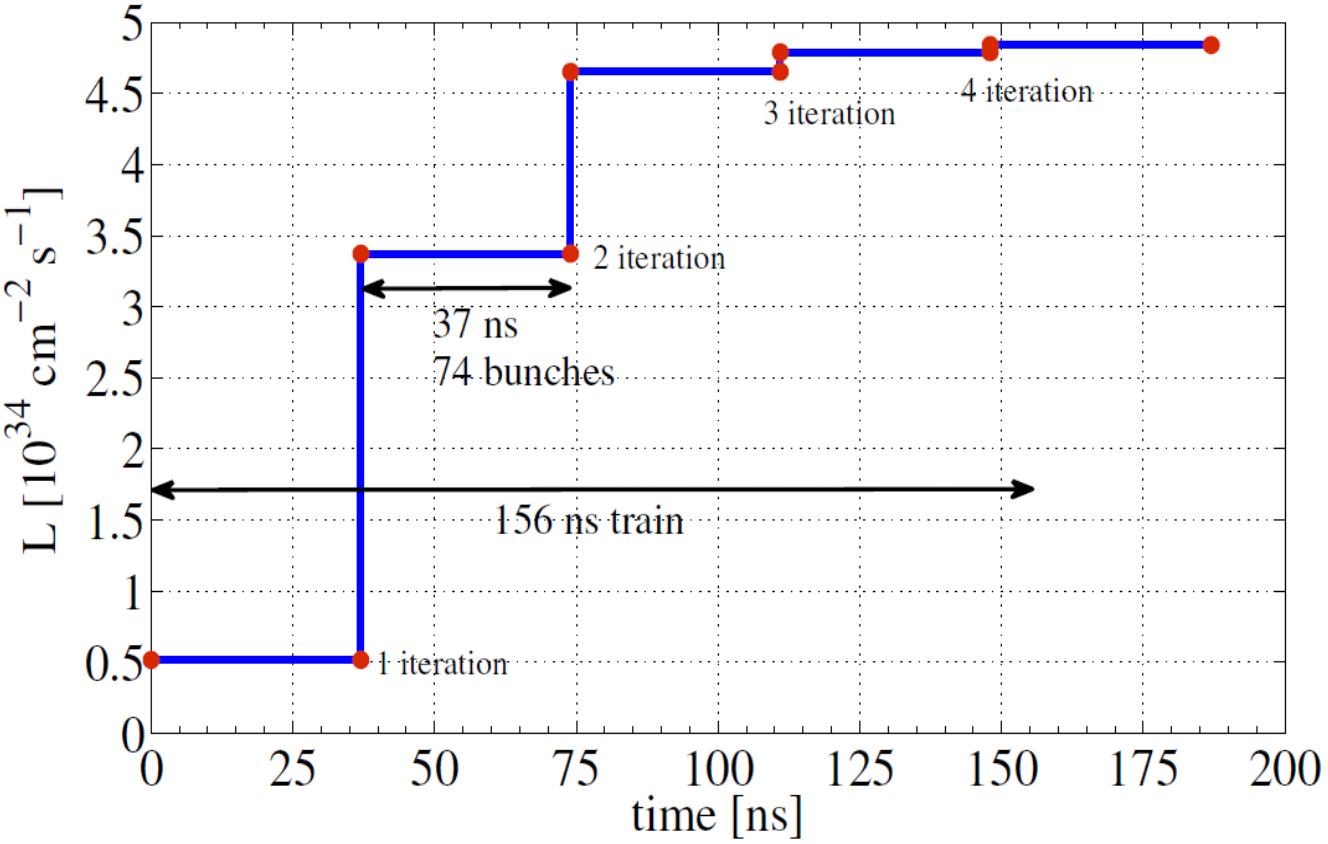


Luminosity performance with IP FB

Resta Lopez

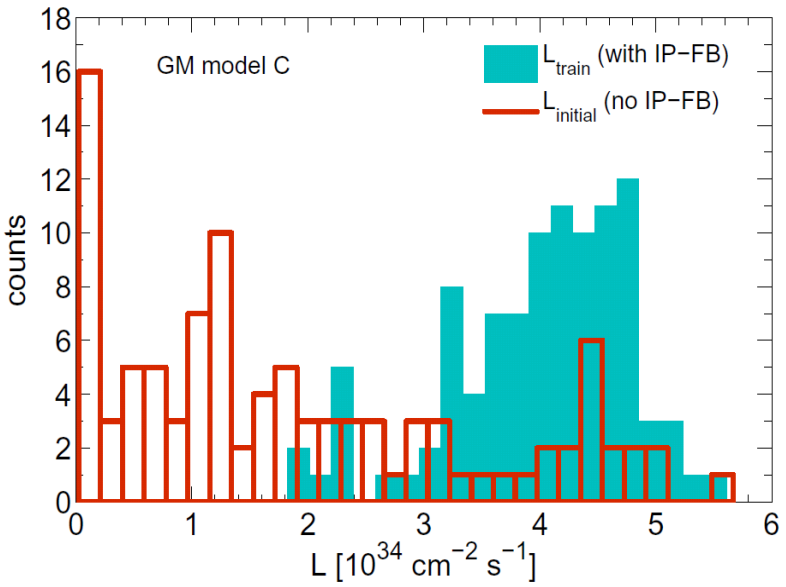
Simulation time structure:
Example applying a single random seed of GM C

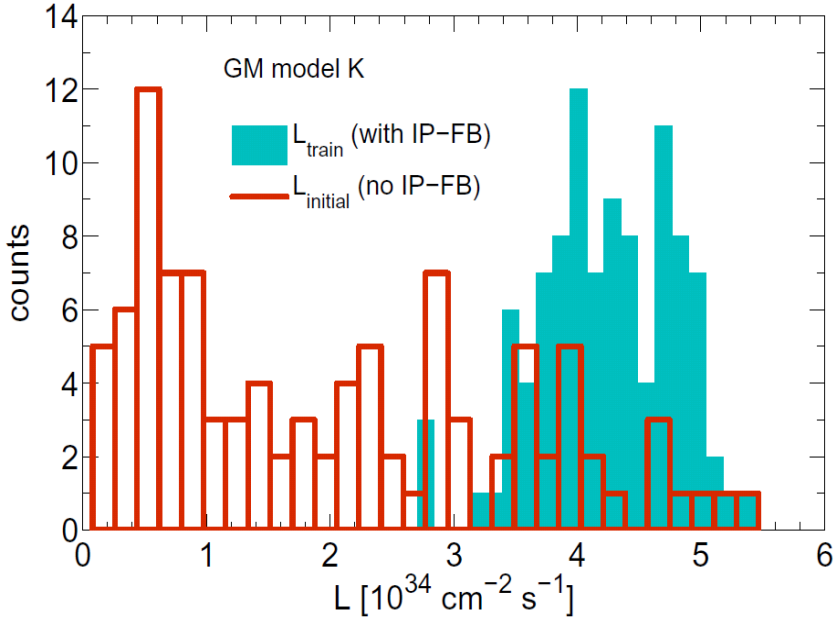


Luminosity performance with IP FB

Resta Lopez

For noisy sites:





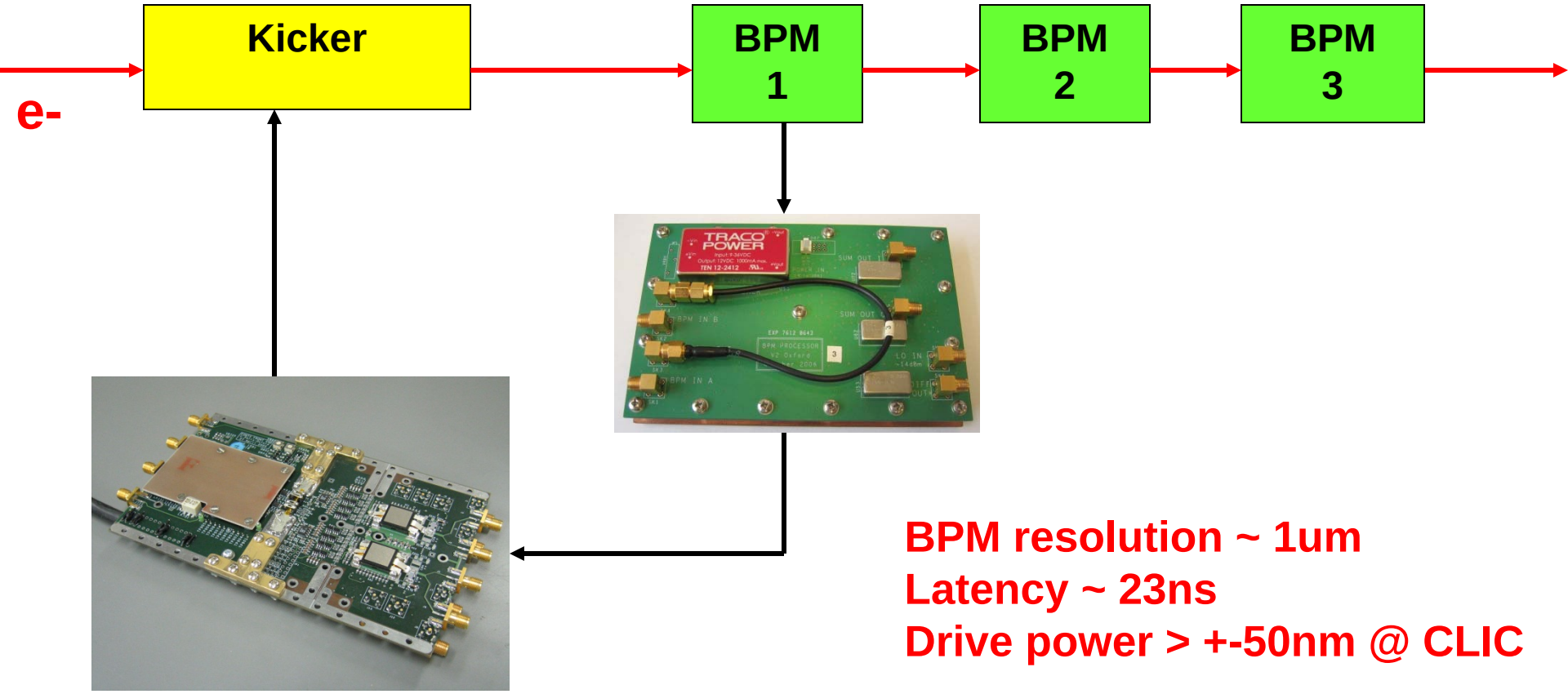
Model C:

- Without any correction: mean $\Delta L/L_0\rangle_{train}$=30.52% & High standard deviation!
- With IP-FB: mean $\Delta L/L_0\rangle_{train}$=64.15% std reduced by a factor 2

Model K:

- Without any correction: mean $\Delta L/L_0\rangle_{train}$=32.53% & High standard deviation!
- With IP-FB: mean $\Delta L/L_0\rangle_{train}$=67.82% std reduced by a factor 3

CLIC prototype: FONT3 at KEK/ATF



BPM resolution ~ 1um
Latency ~ 23ns
Drive power > +-50nm @ CLIC

Remaining technical issues

- **Engineering of real hardware optimised for tight spatial environment: BPM, kicker, cables …**
- **Large (and spatially-varying) B-field → operation of ferrite components in kicker amplifier?!**
- **Further studies of radiation environment for FB system:**

  was studied for ILC, so far preliminary for CLIC;

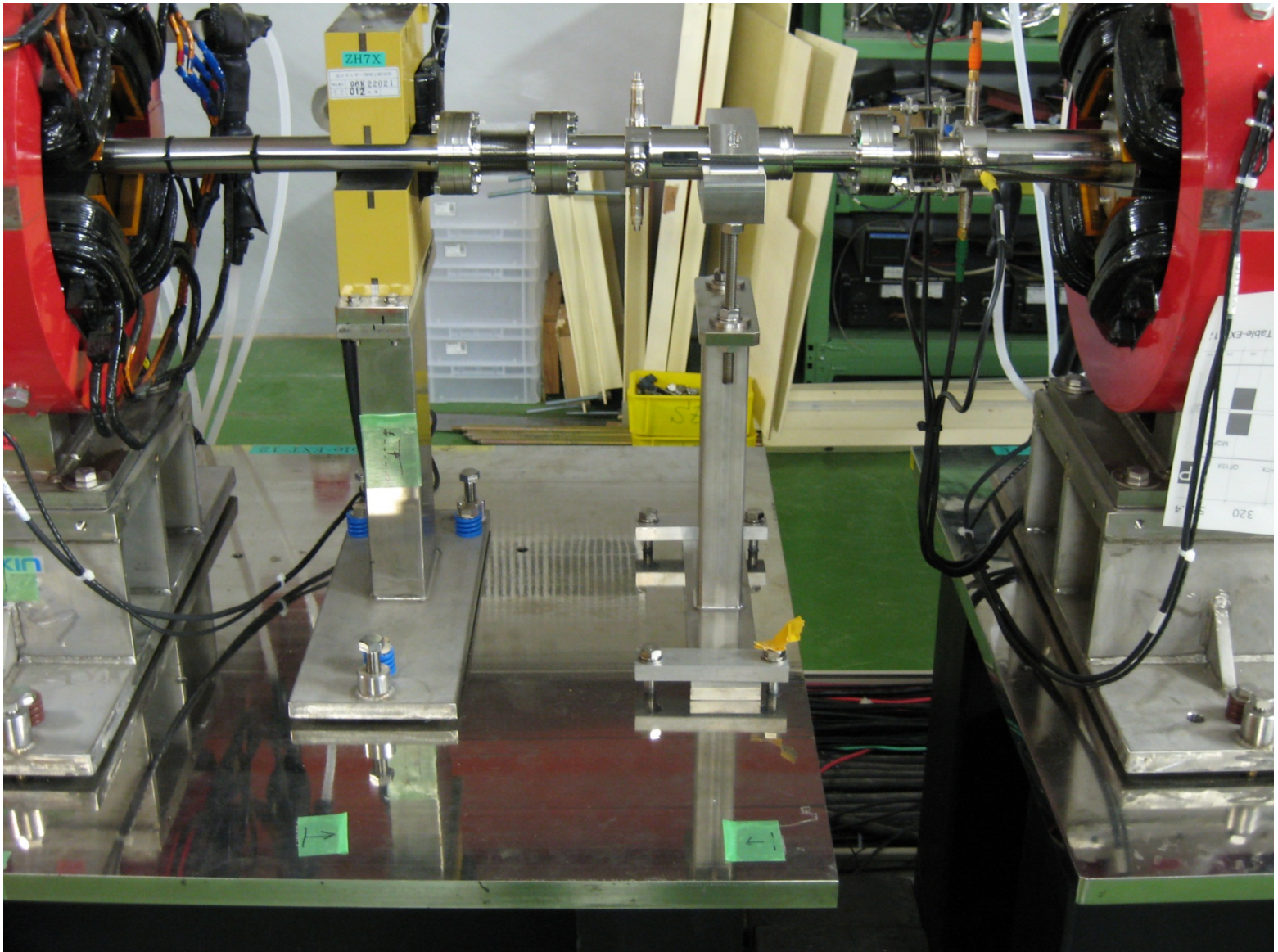
  where to put electronics?

  need to be rad hard? shielded?

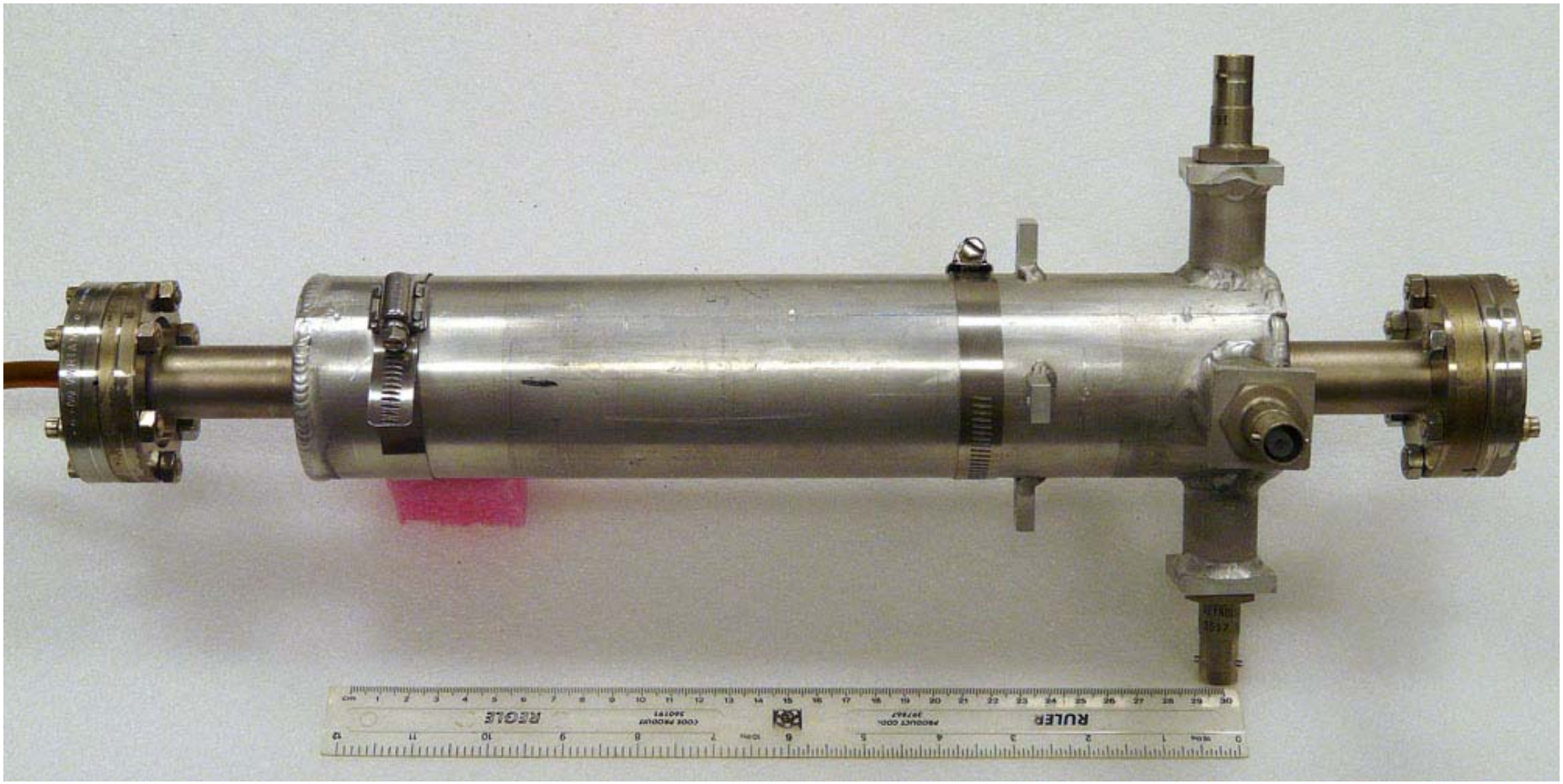
- **RF interference: beam ←→ FB electronics**

  kicker ←→ detector

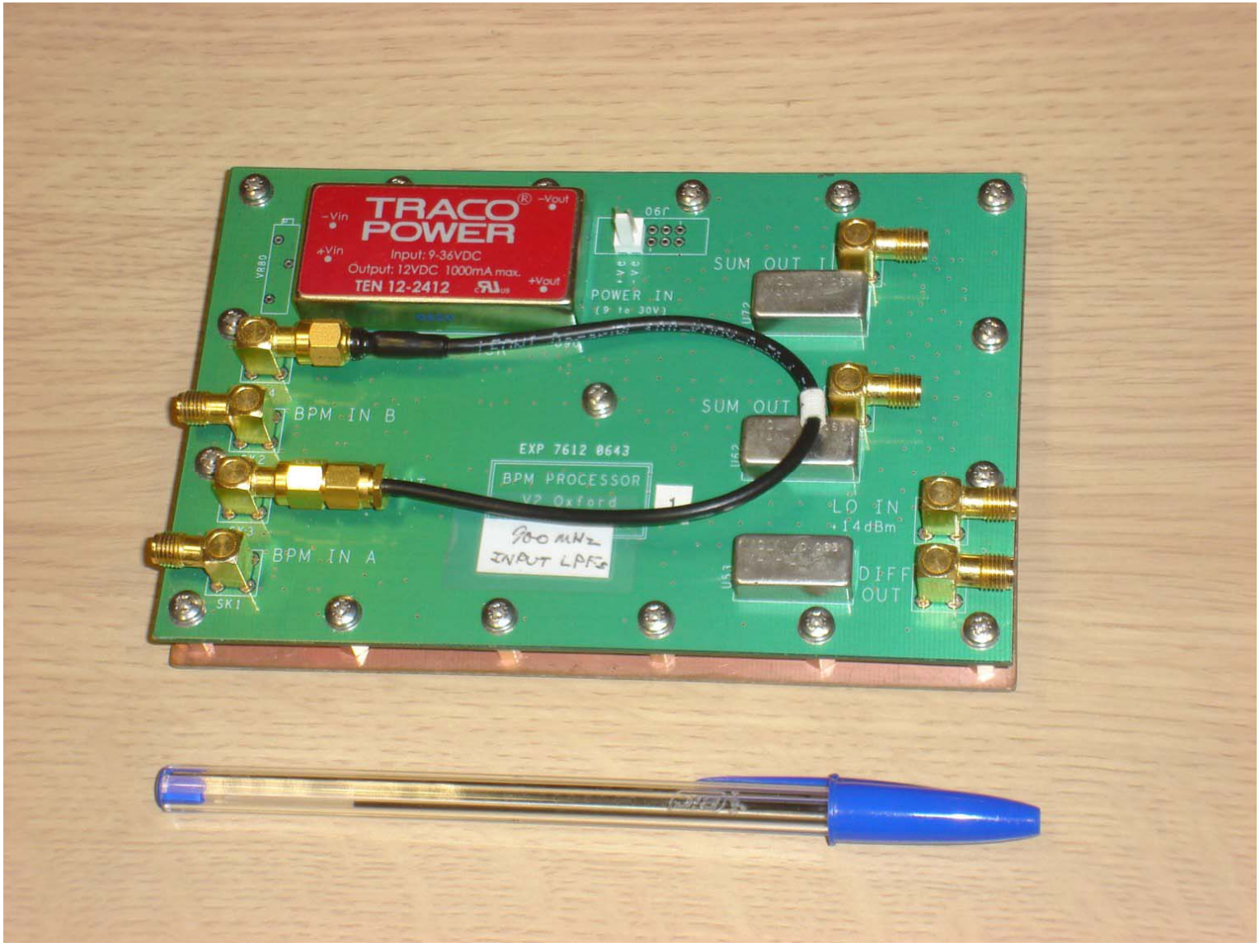
Off-shelf BPM



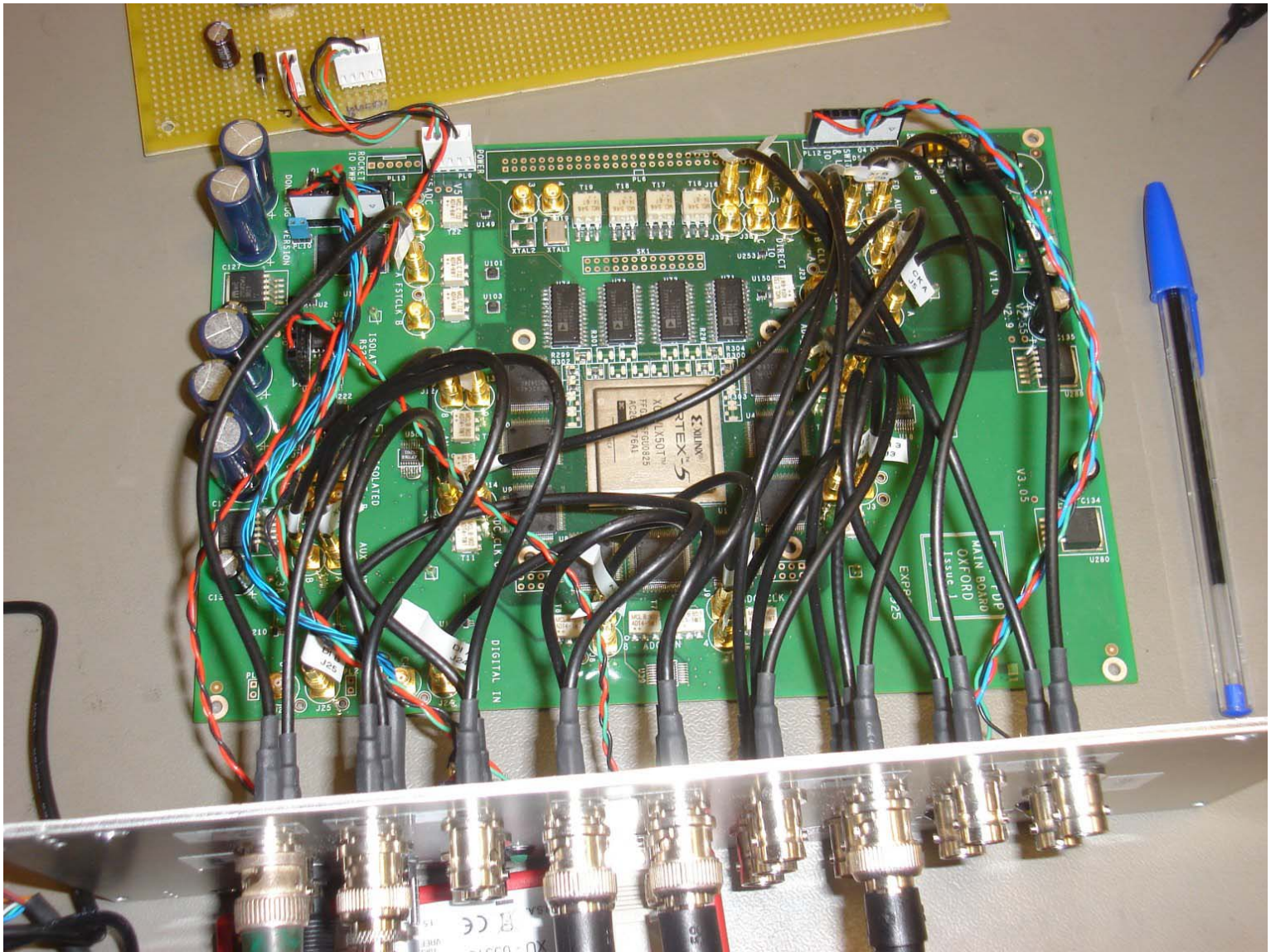
Off-shelf kicker



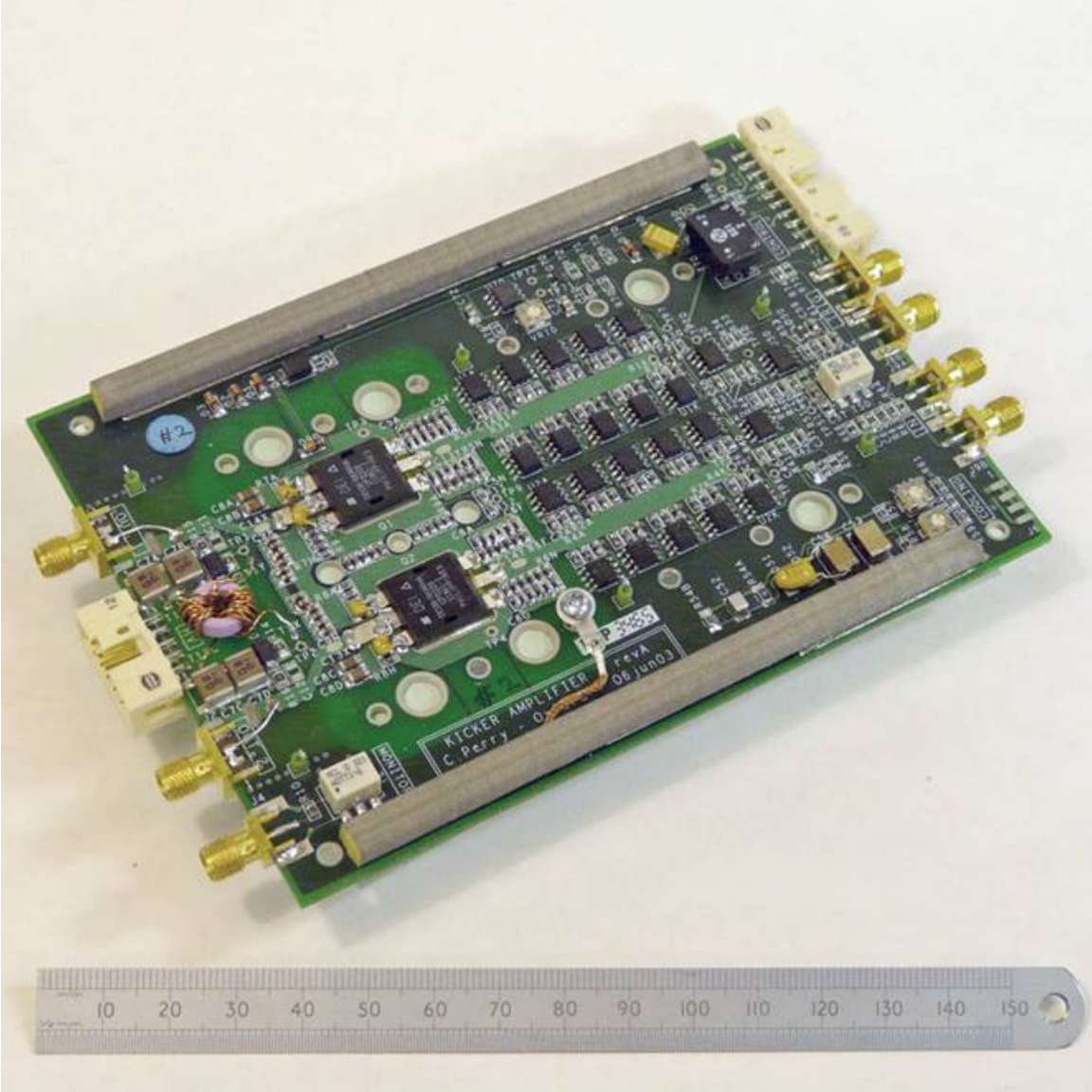
BPM processor



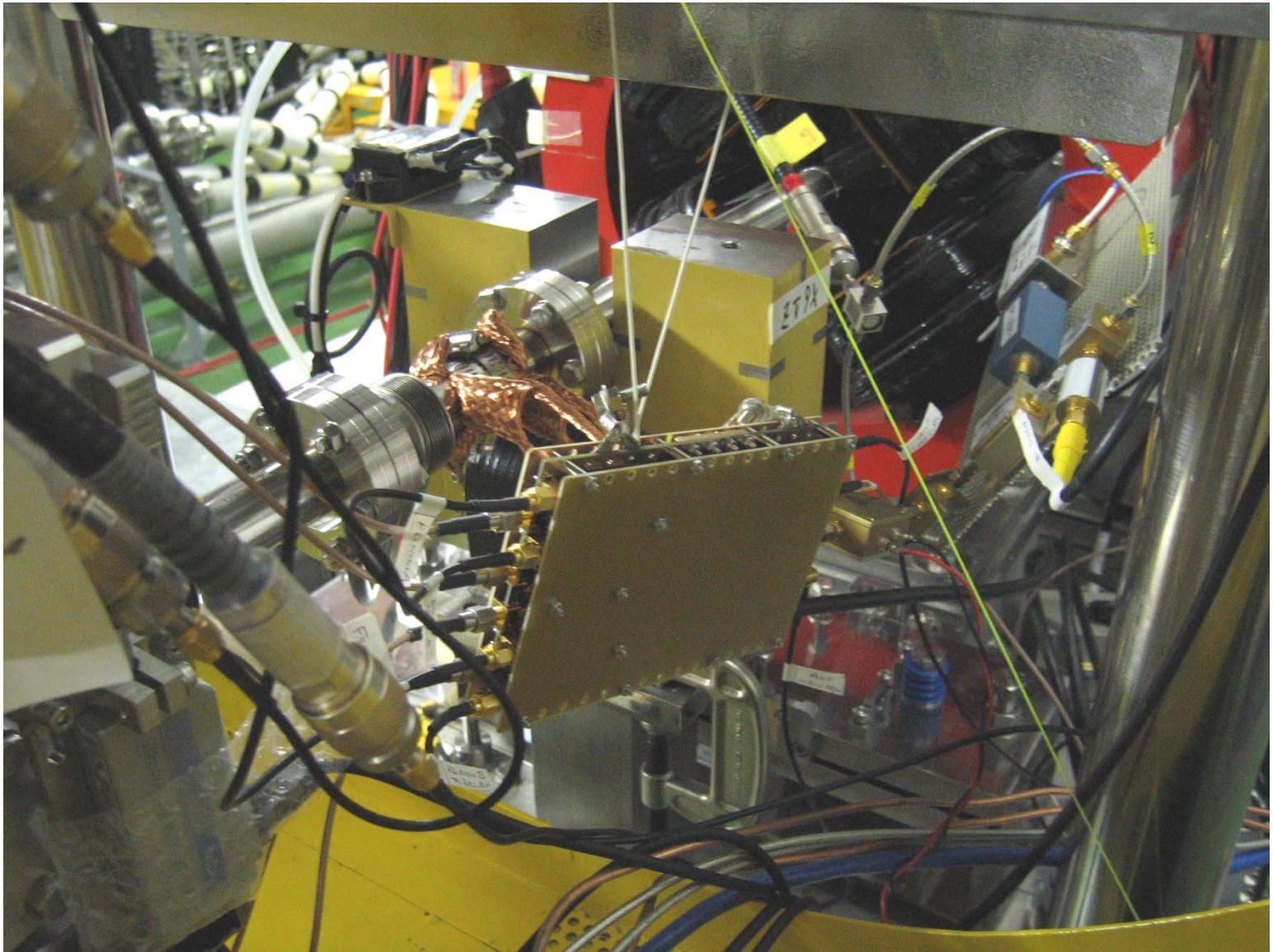
FB board


XILINX
VIRTEX-5
MAIN BOARD
OXFORD
Issue. 1
DIGITAL IN
ISOLATED

Drive amplifier



A pragmatic approach!



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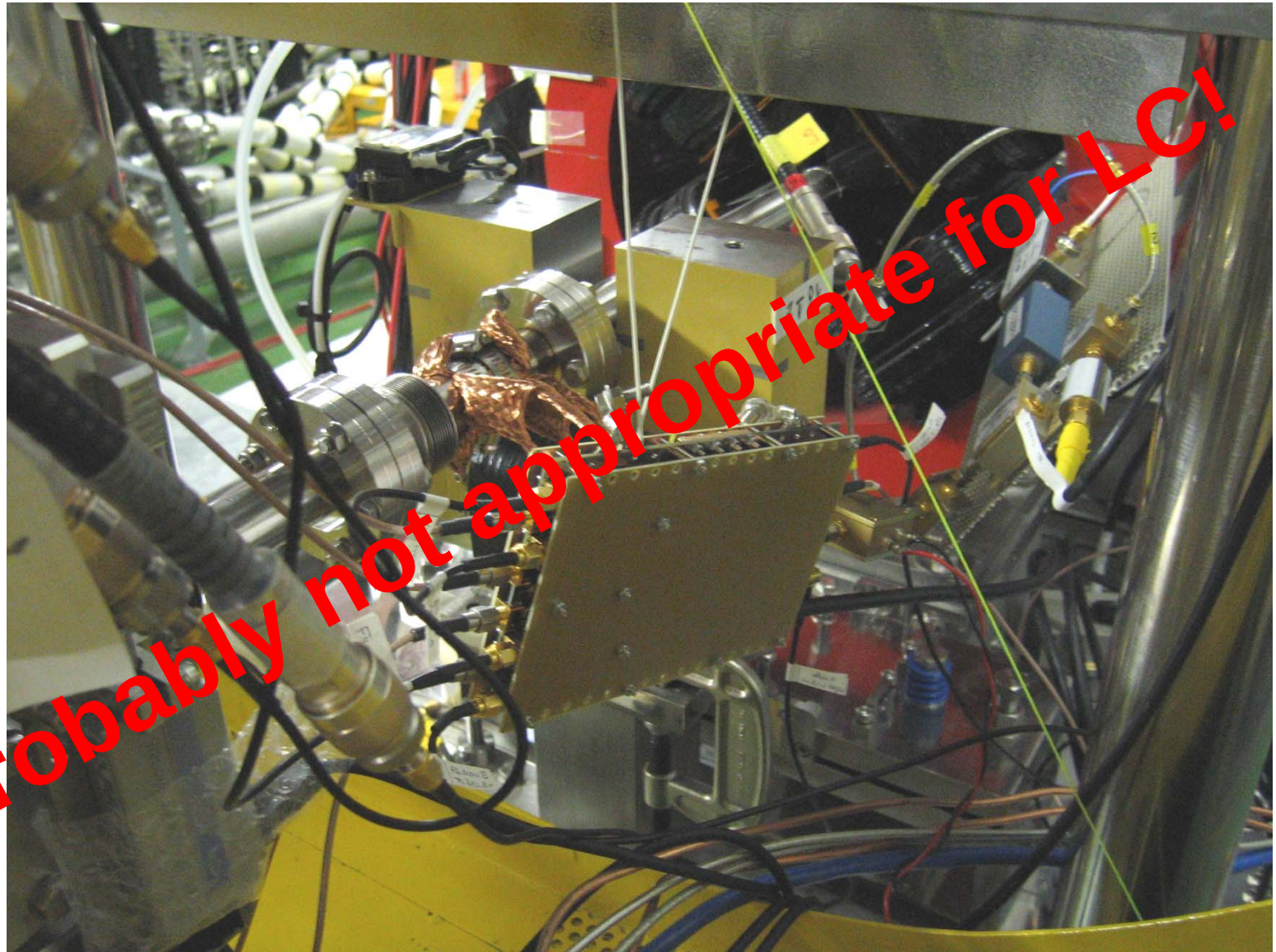
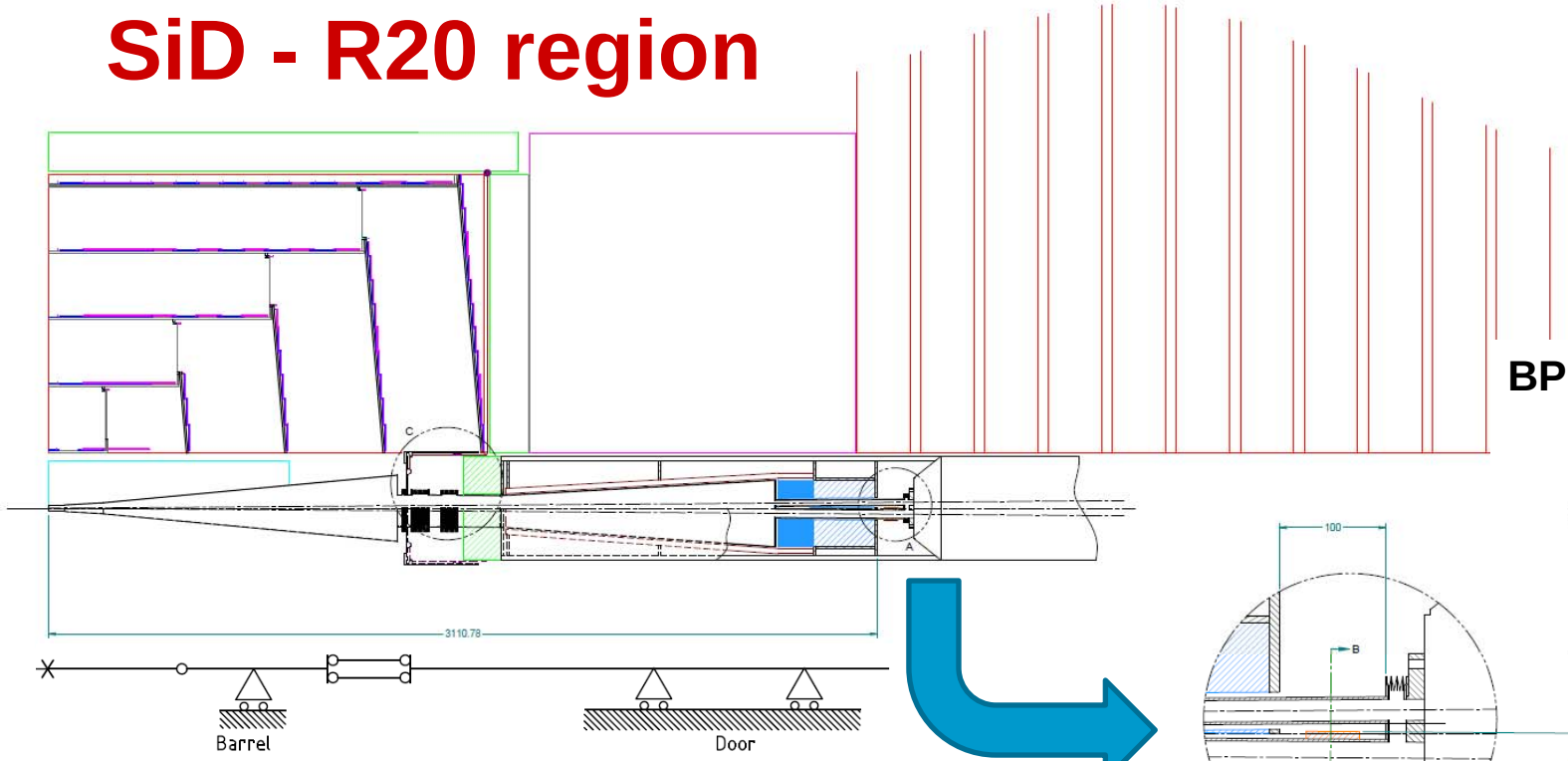
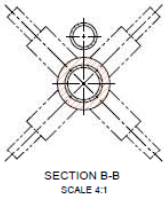


SiD - R20 region

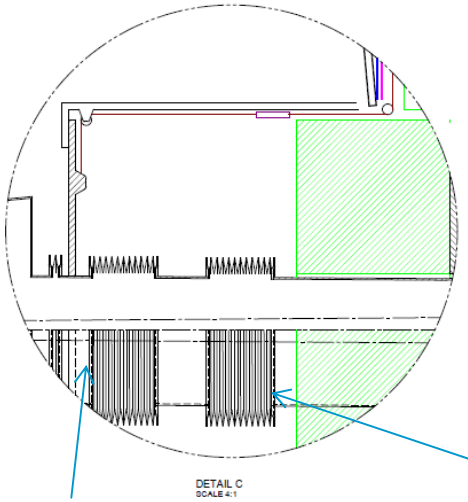
Marco Oriunno



BPM arrangement, under study



Gap Lumical vs. QD0
BPM for IP Lum. Fedback

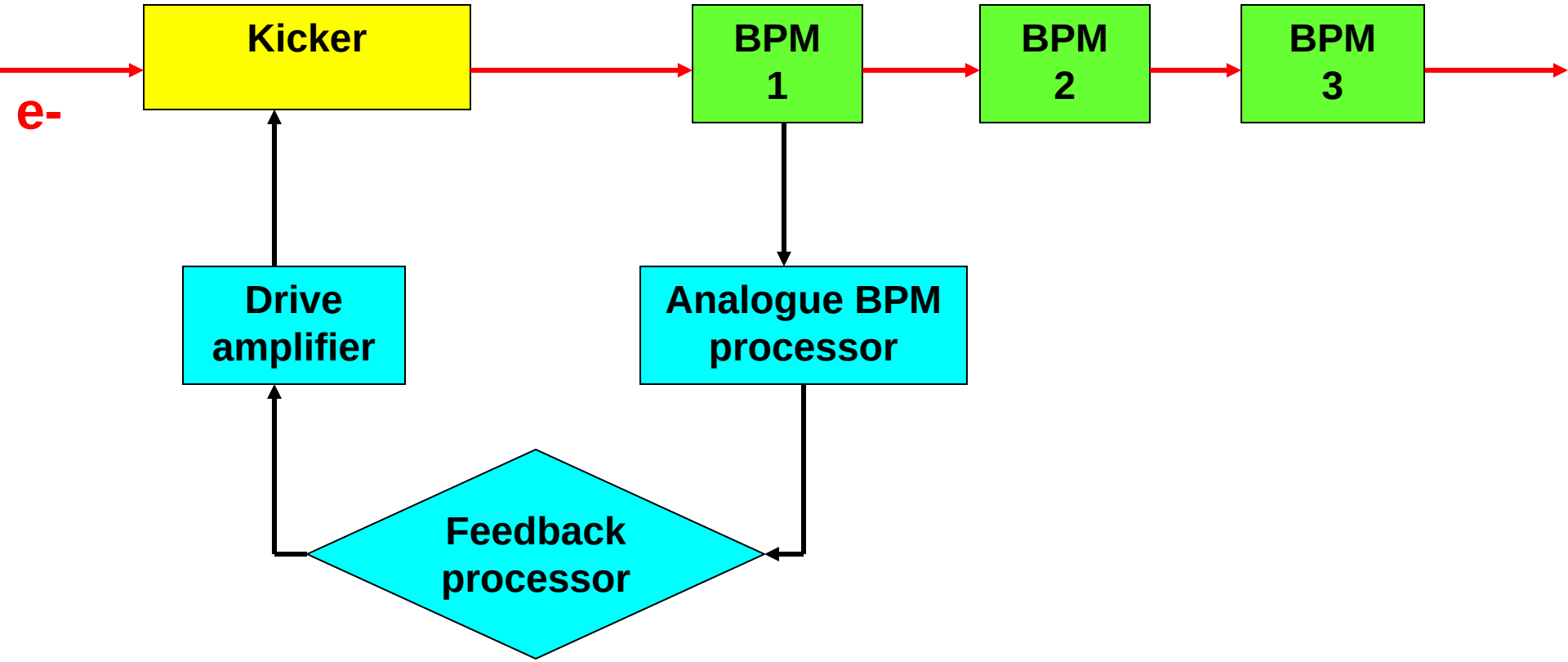


Single convolution bellow
Kinematic Mount. VTX

Multi convolution bellows
Stress Relief QD0 vs. VTX

Prototyping status

Generic prototype layout



Brief prototype history: CLIC

CLIC-relevant: all-analogue systems

Brief prototype history: CLIC

CLIC-relevant: all-analogue systems

- NLCTA (SLAC): 65 MeV beam, 170ns train, 87ps bunch spacing

FONT1 (2001-2):

First demonstration of closed-loop FB: latency 67ns

10/1 beam position correction

FONT2 (2003-4):

Improved demonstration of FB: latency 54ns

real time charge normalisation with logarithmic amplifiers

beam flattener to straighten train profile

solid-state amplifier

- ATF (KEK): 1.3 GeV beam, 56ns train, 2.8ns bunch spacing

FONT3 (2004-5):

Ultra-fast demonstration of FB: latency 23 ns

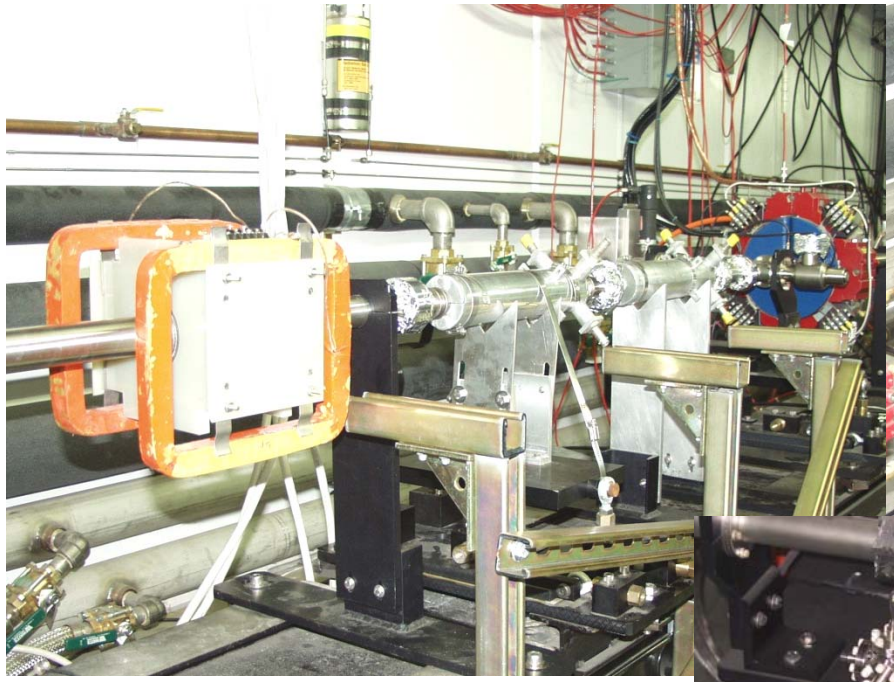
3 stripline BPMs

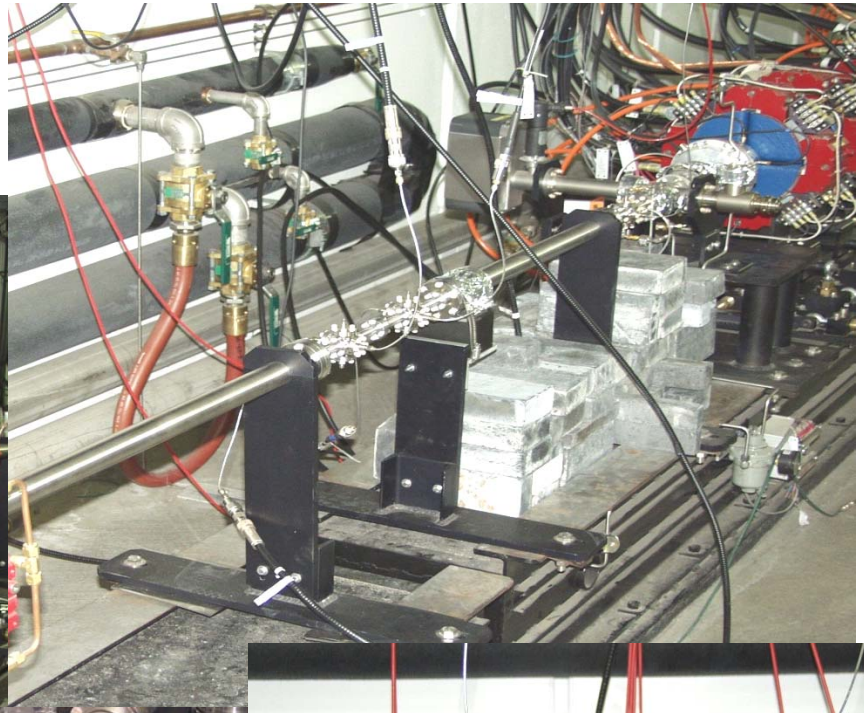
high-power solid-state amplifier

FONT2 beamline installation at SLAC NLCTA

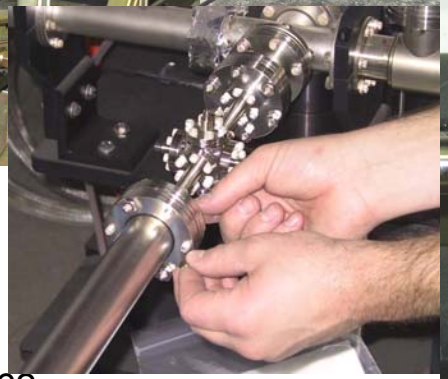
(65 MeV 170ns-long train @ 87ns spacing)

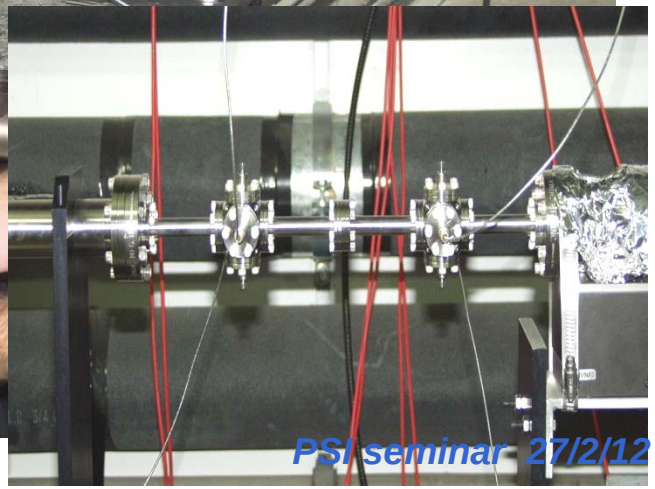
Dipole and kickers





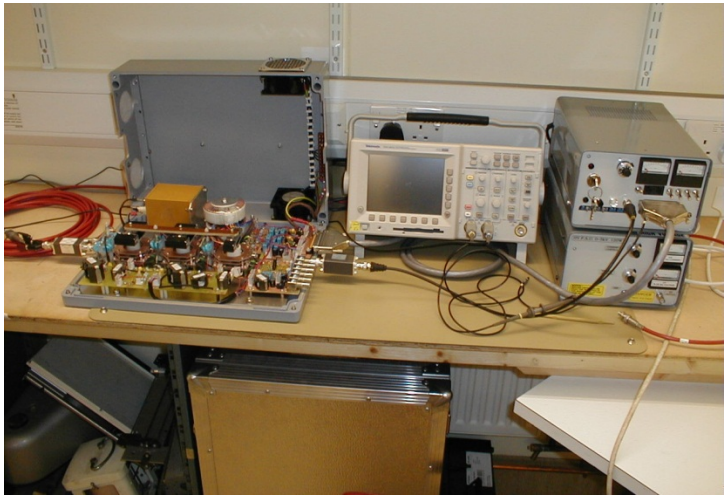
BPMs

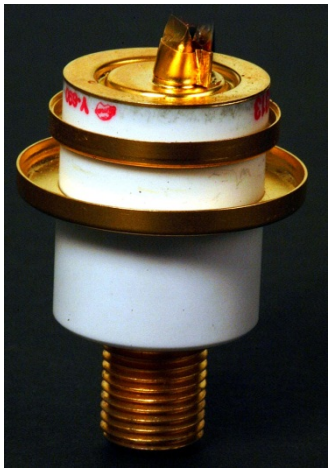




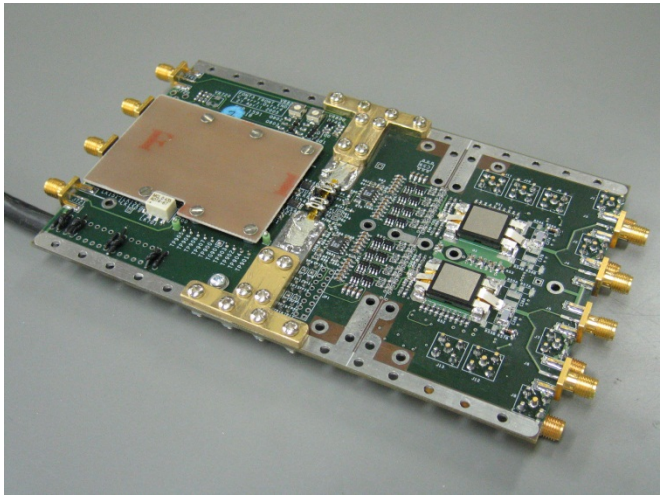
FONT: kicker driver amplifiers

FONT1 3-stage tube amplifier



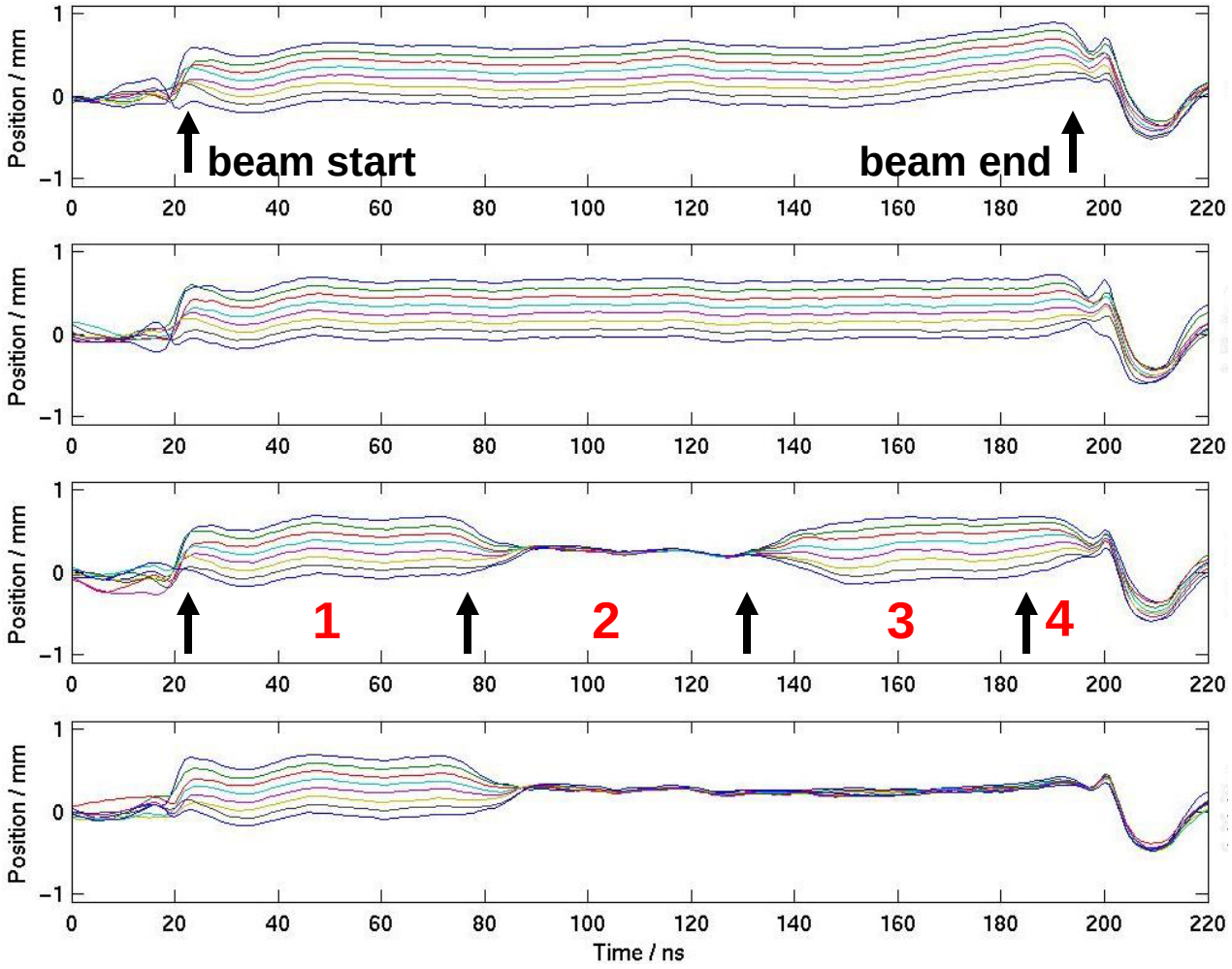


FONT3 PCB amplifer + FB



Same drive power as needed for CLIC

FONT2 results



Beam starting positions

Beam flattener on

Feedback on

Delay loop on

Brief prototype history: CLIC

CLIC-relevant: all-analogue systems

FONT2 (2003-4):

- **latency 54ns**
- **would allow about 2 correction passes for CLIC 150ns train**

FONT3: latency budget

- Time of flight kicker – BPM: 4ns
- Signal return time BPM – kicker: 6ns

  Irreducible latency: 10ns

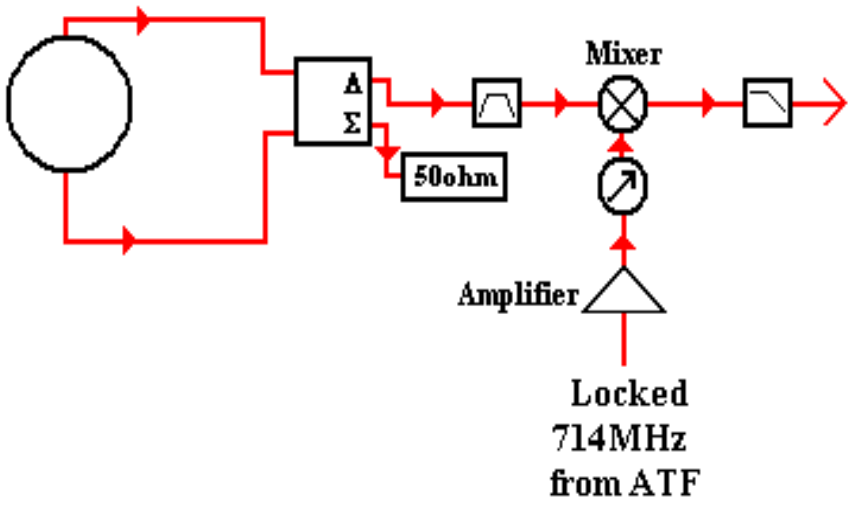
- BPM processor: 5ns
- Amplifier + FB: 5ns

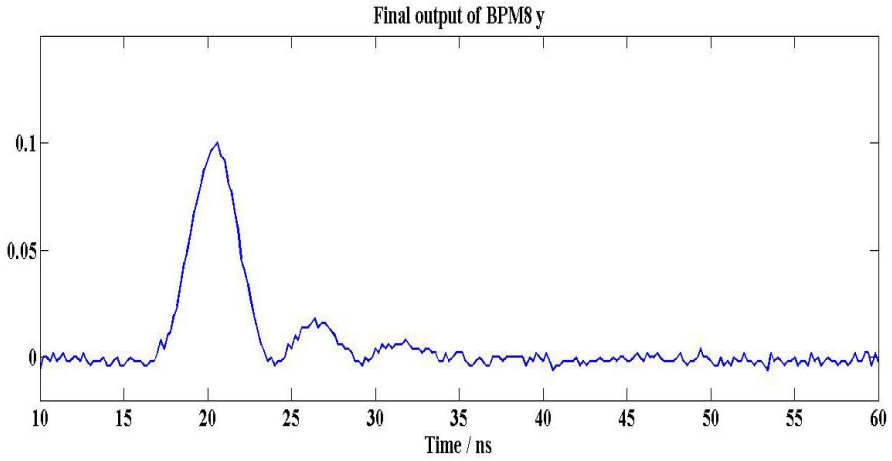
  Electronics latency: 10ns

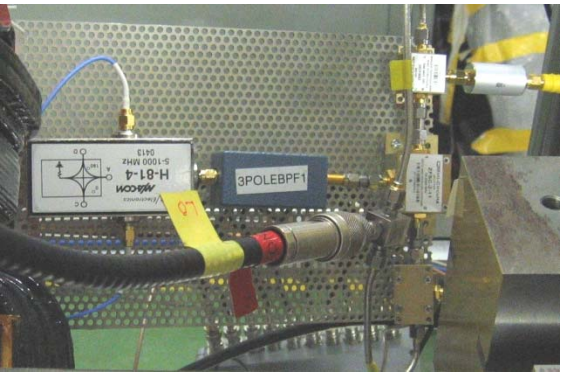
- Total latency budget: 20ns

Allows 56/20 = 2.8 periods during bunchtrain

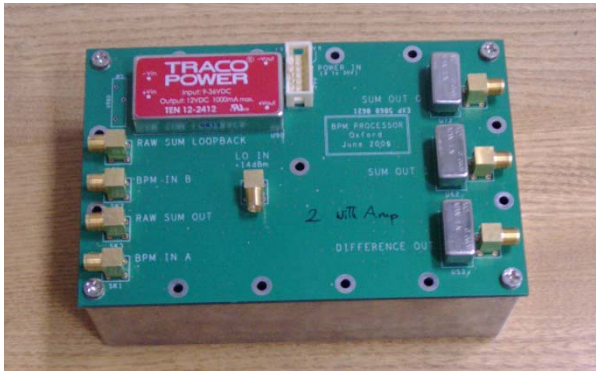
Fast analogue signal processors







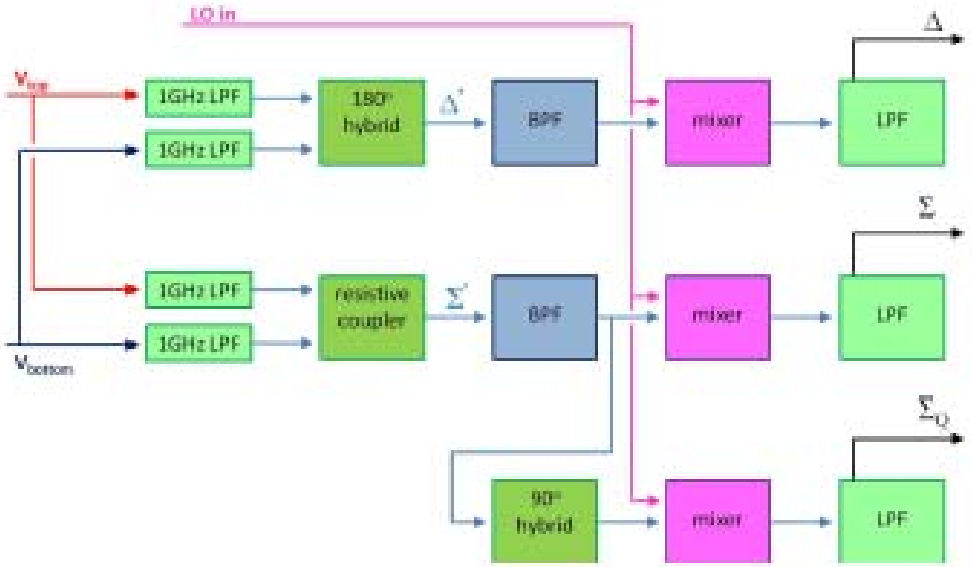
2005



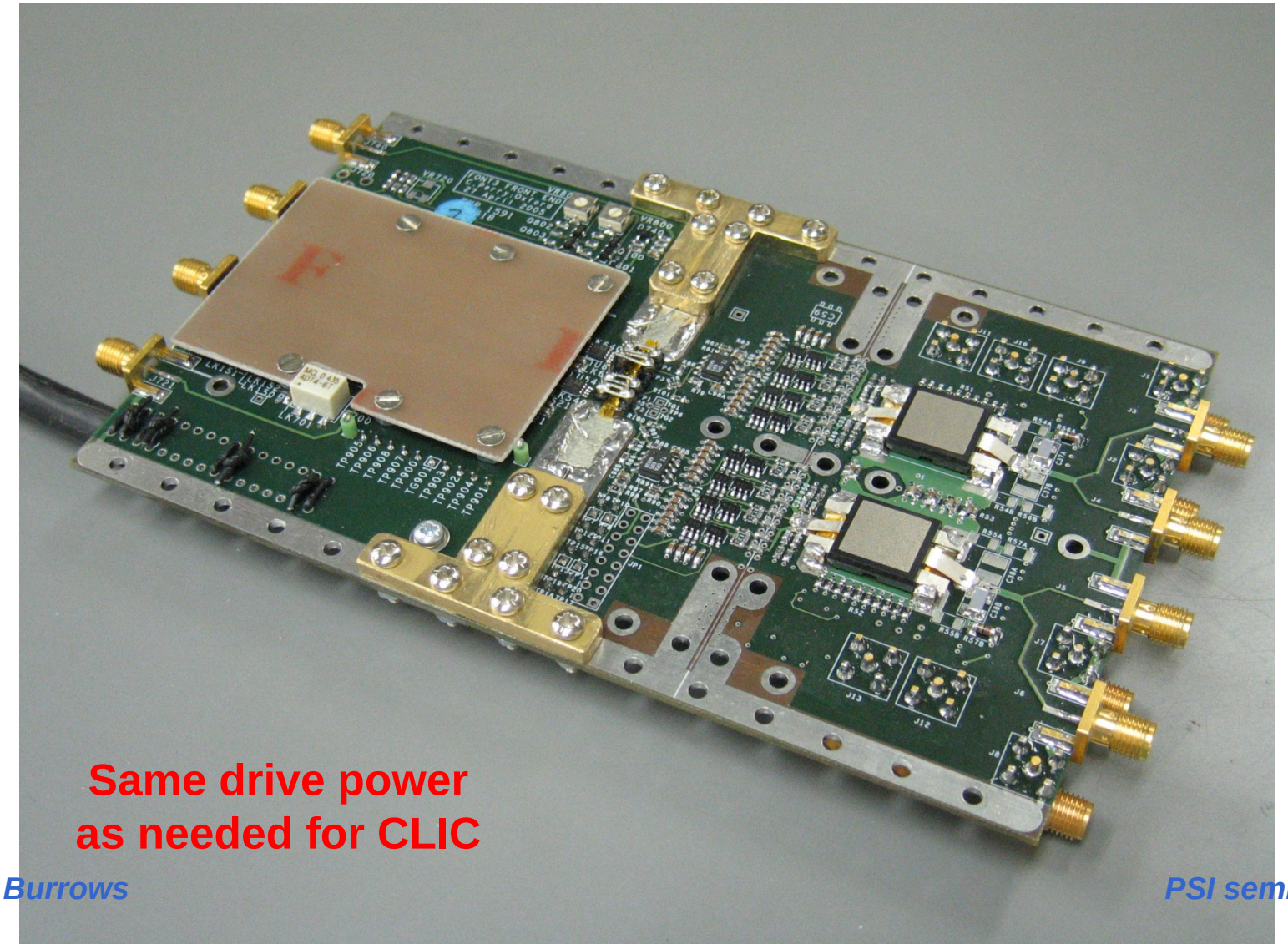
2006

2007

BPM processor architecture

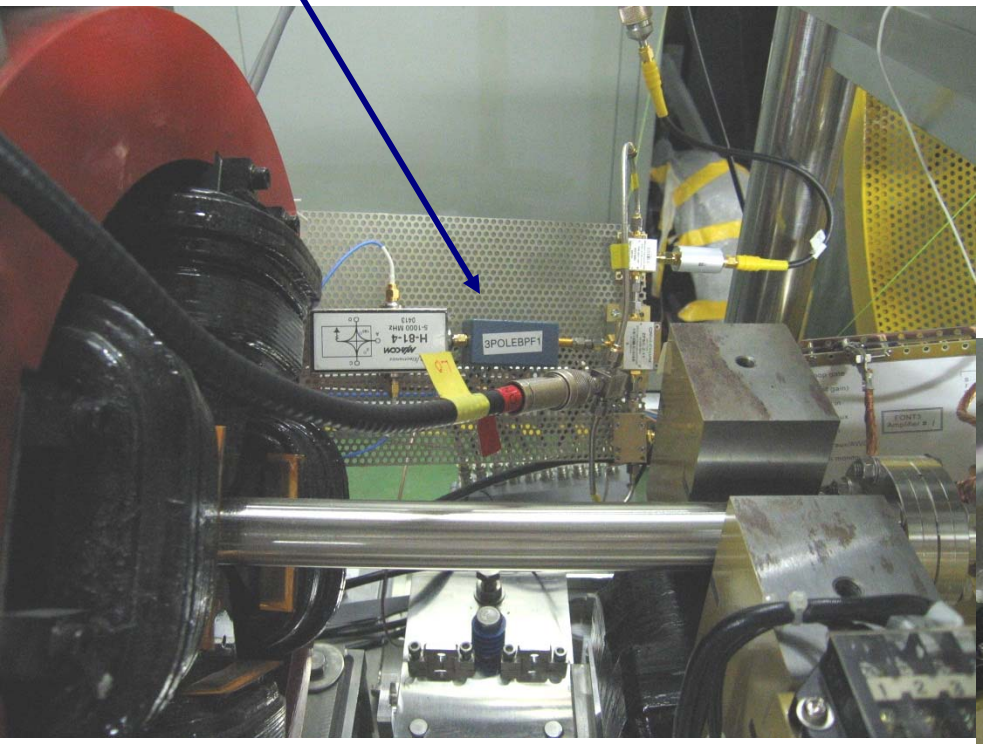


FONT3: kicker driver amplifier



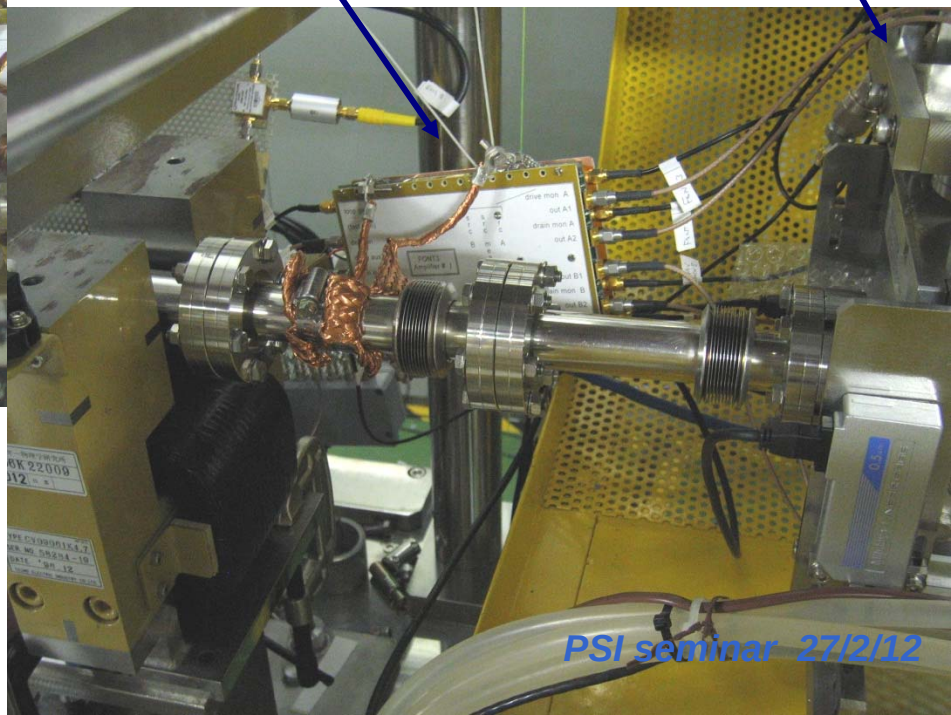
FONT3: BPM processor + amplifier/feedback installation in ATF beamline

BPM processor board

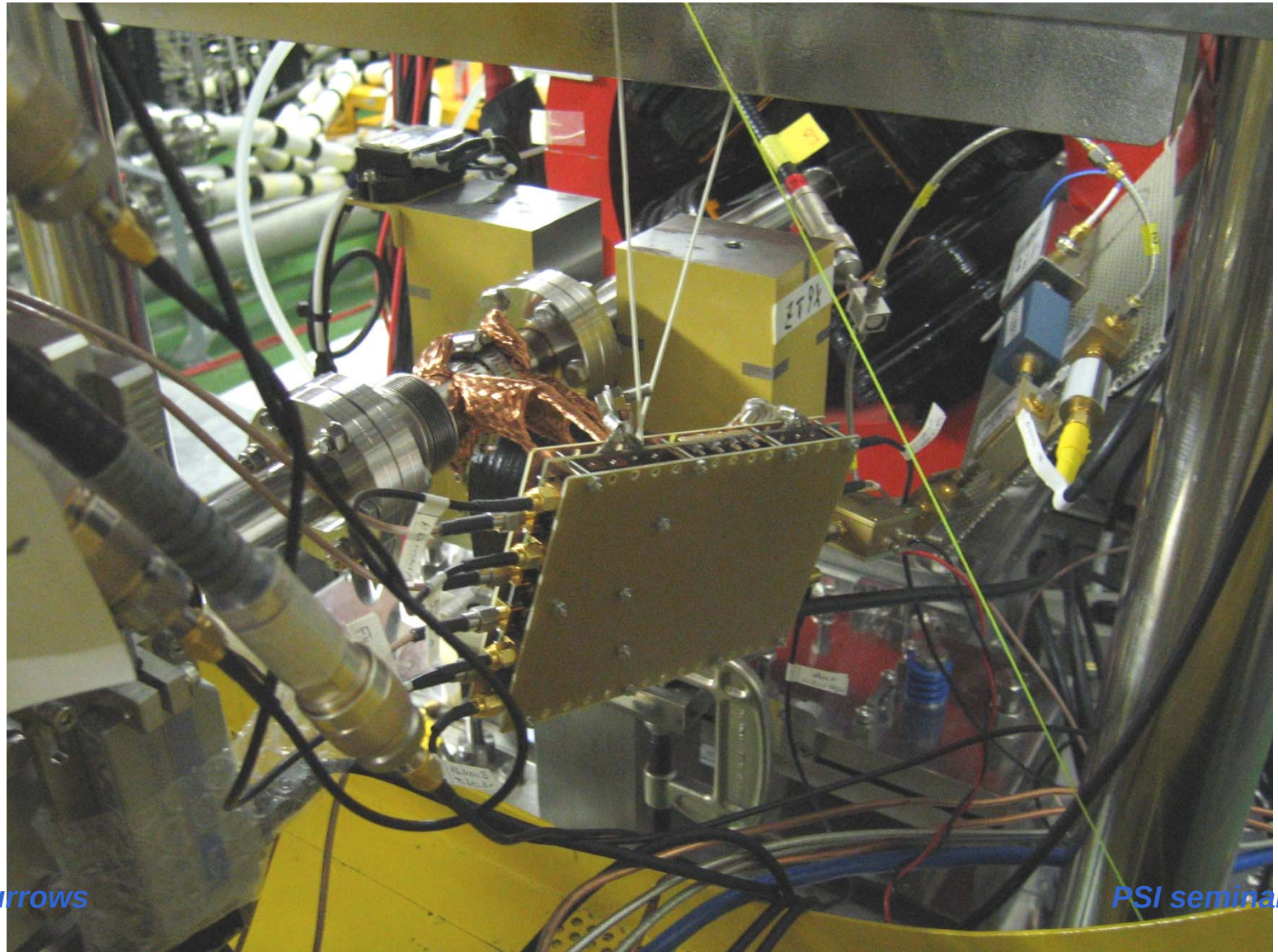


FEATHER kicker

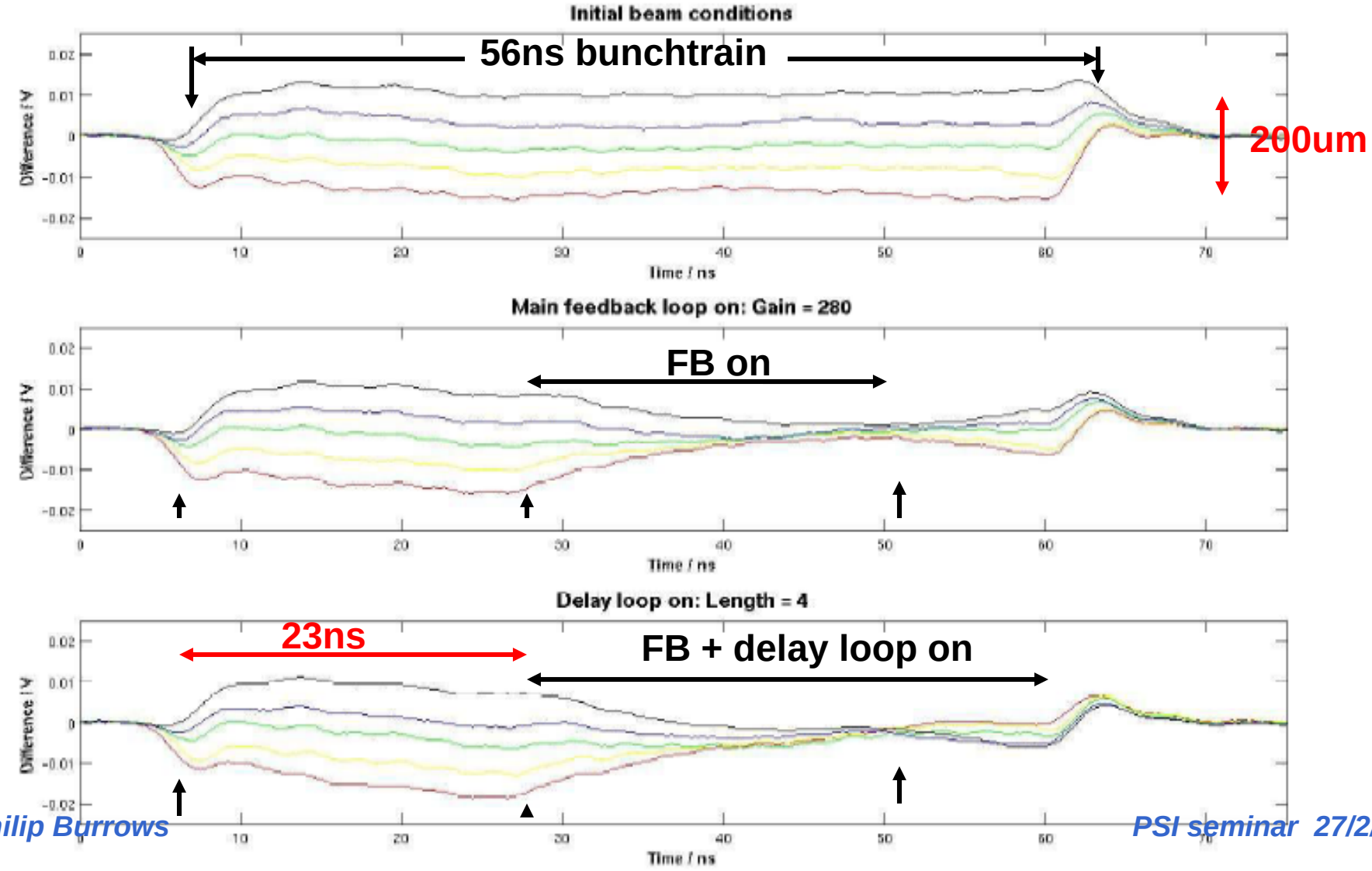
Amplifier/FB board



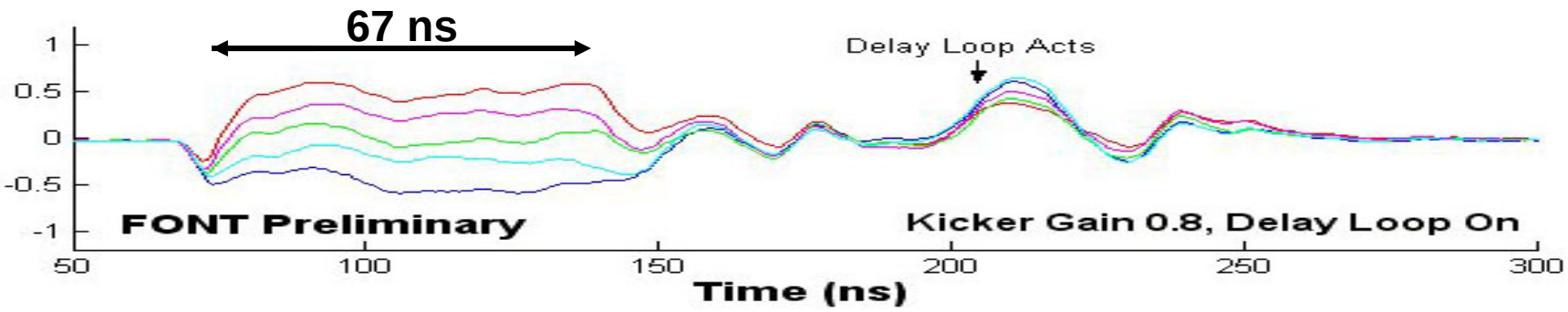
FONT3: Beamline Installation

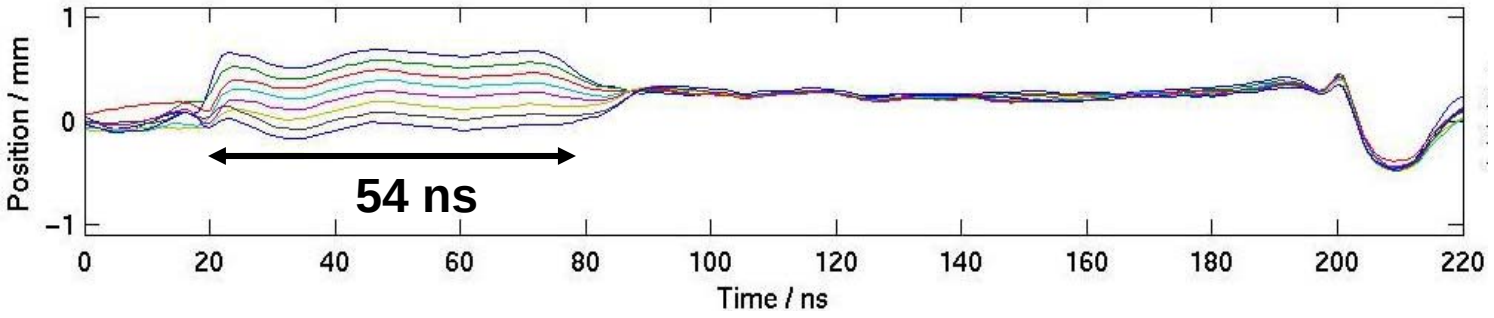


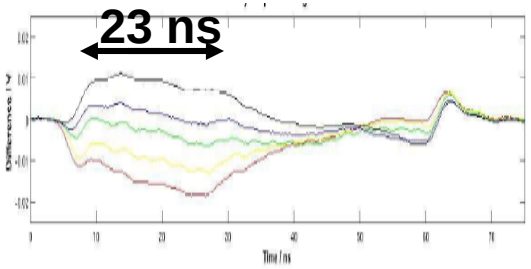
FONT3: Results (June 2005):
Delay-loop feedback w. latency 23 ns



CLIC prototype: Summary







Brief prototype history: CLIC

CLIC-relevant: all-analogue systems

FONT3 (2005):

total latency 23ns, of which 13ns electronics

translates to about 37ns at CLIC

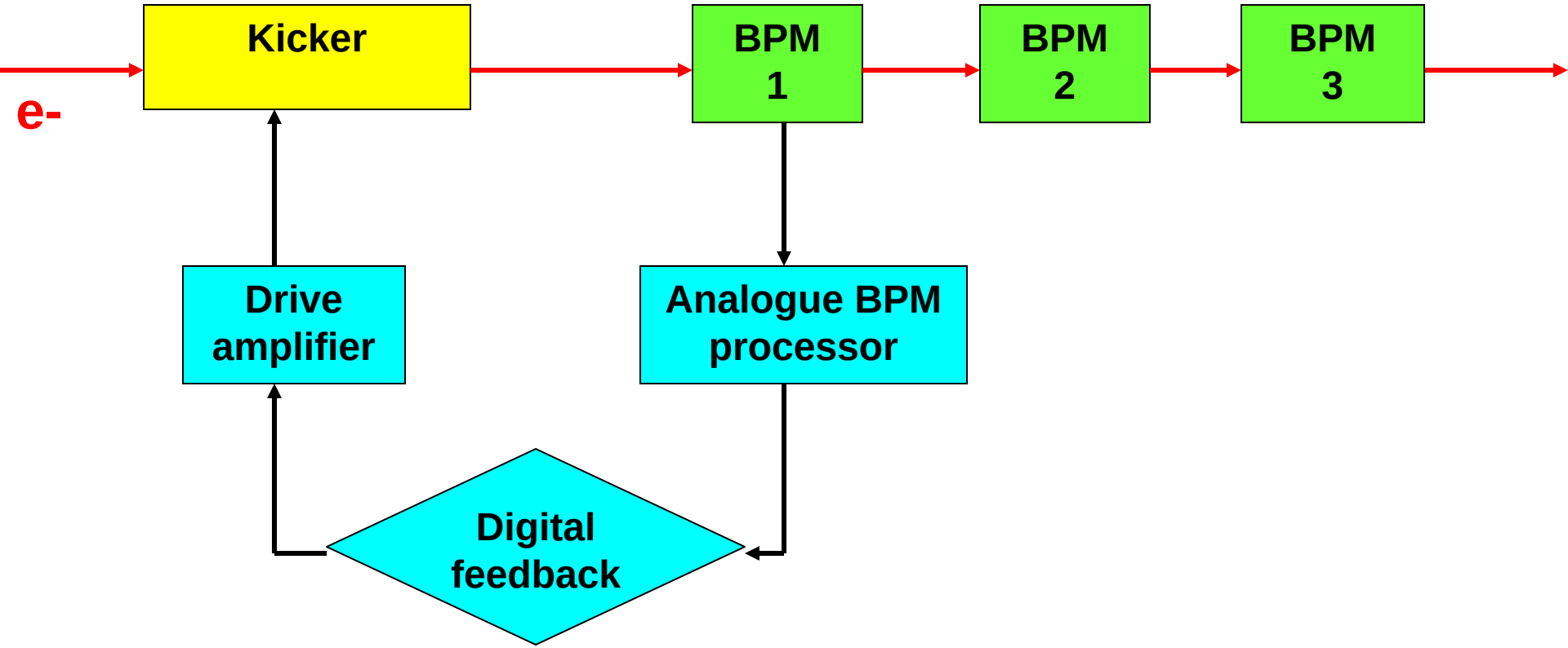
would allow about 3 correction passes for CLIC 150ns train

basic principle demonstrated: more work needed to optimise design + system performance.

Brief prototype history: ILC

ILC-relevant: digital feedback processor

Generic prototype layout: ILC



Brief prototype history: ILC

ILC-relevant: digital feedback processor

- ATF (KEK): 1.3 GeV beam, 3-bunch train, bunch spacing c. 150ns

FONT4 / ATF (2006-9):

First digital system (Virtex 4): latency 148 ns

high-power solid-state amplifier (pulse length up to 10us)

FONT5 / ATF2 (2009-10):

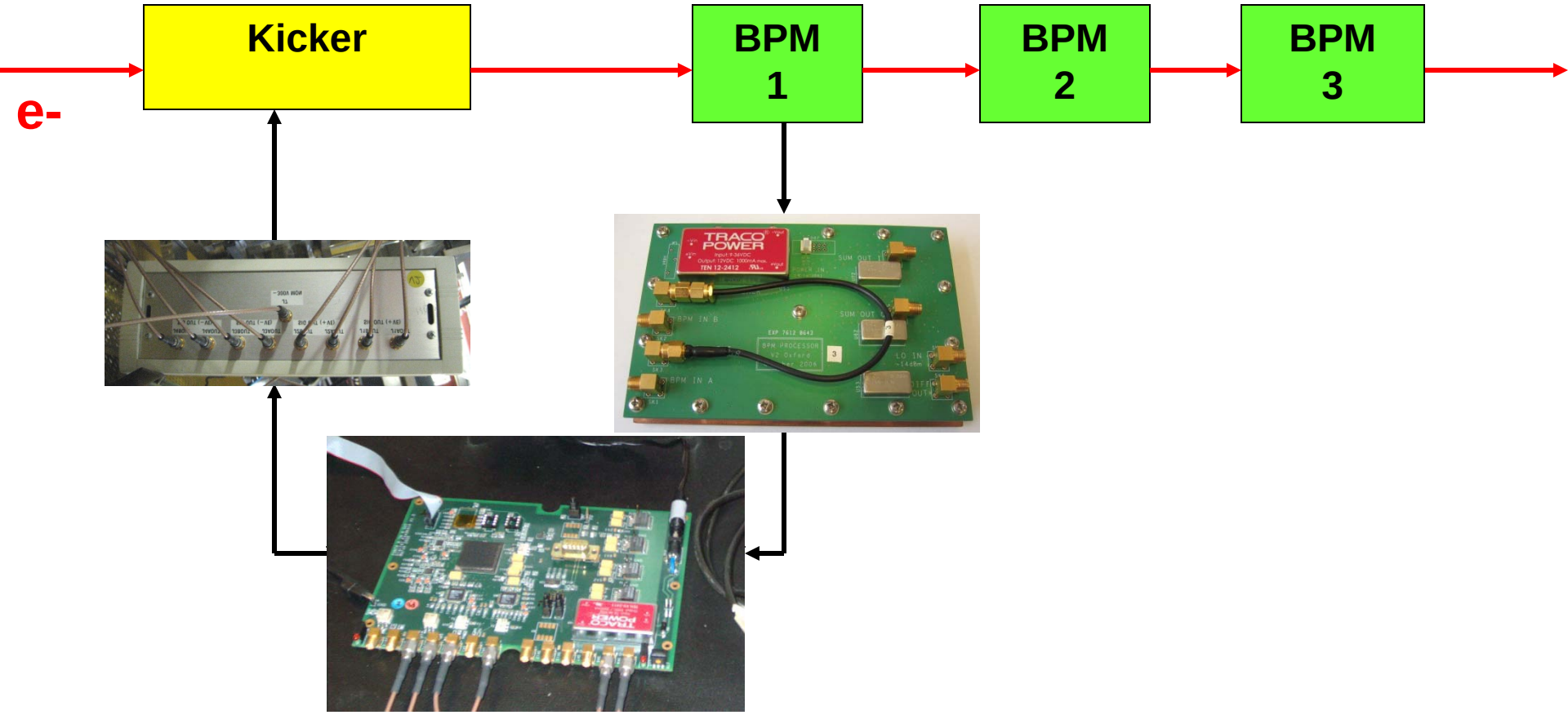
Faster system (Virtex 5): latency 133 ns

coupled-loop system

correction of y and y'

3 BPMs and 2 kickers

FONT4 ILC prototype at KEK/ATF



Kicker driver amplifier

Specifications:

- **+- 15A (kicker terminated with 50 Ohm)**
- **+- 30A (kicker shorted at far end)**
- **35ns risetime (to 90%)**
- **pulse length 10 us (specified for 20-60 bunches)**
- **repetition rate 10 Hz**

Outline design done in Oxford

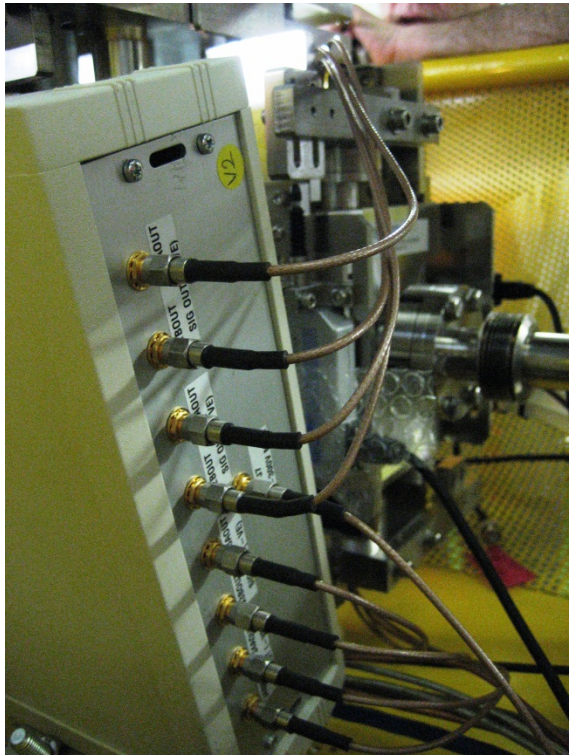
Order placed with TMD Technologies Sept 06

Two prototype units delivered Dec 06

Tested numerous times with beam in 2007

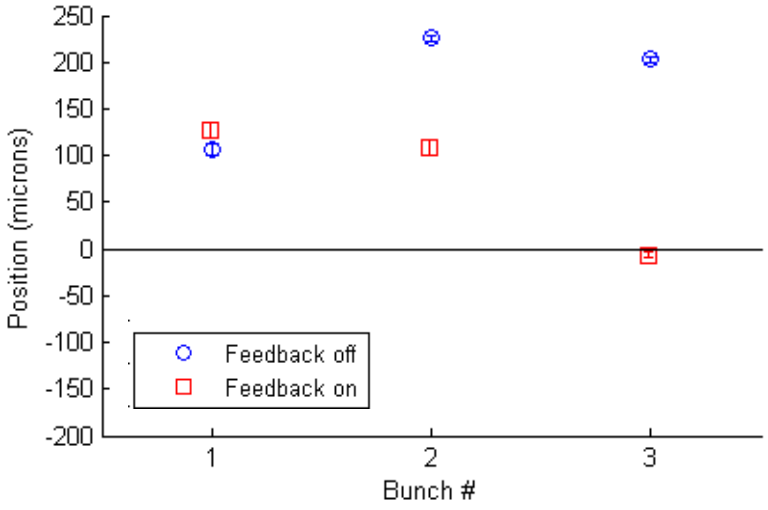
Modifications made

3rd unit purchased in 2009



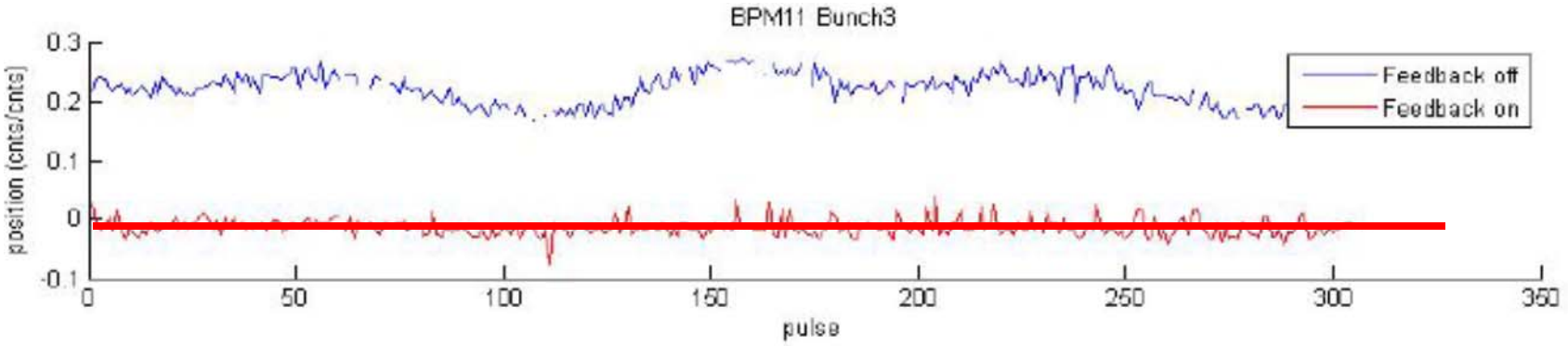
FONT4 results

- **FONT4 basic operation demonstrated in 2008 running:**



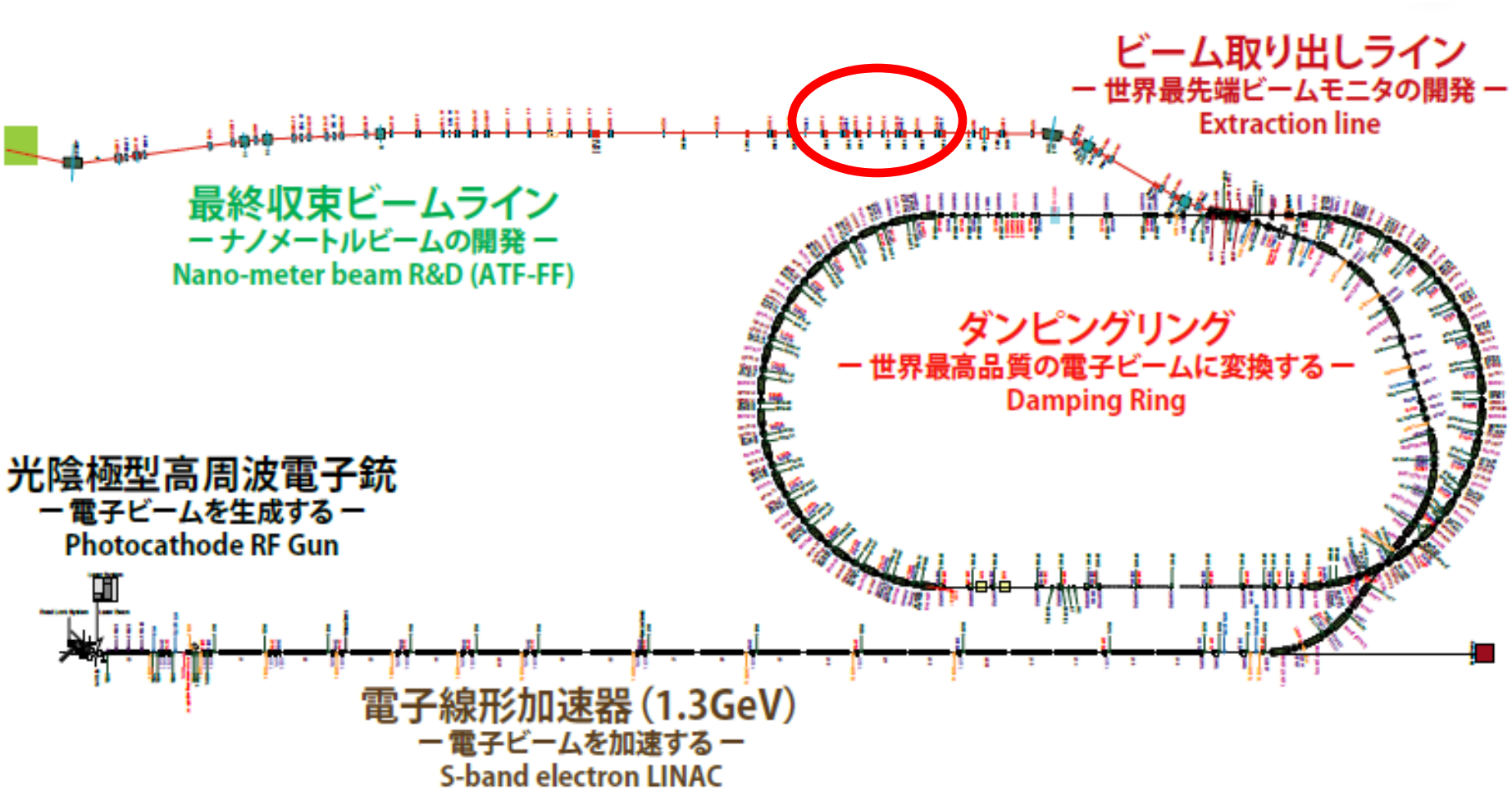
FONT4 results

- **FONT4 basic operation demonstrated in 2008 running:**

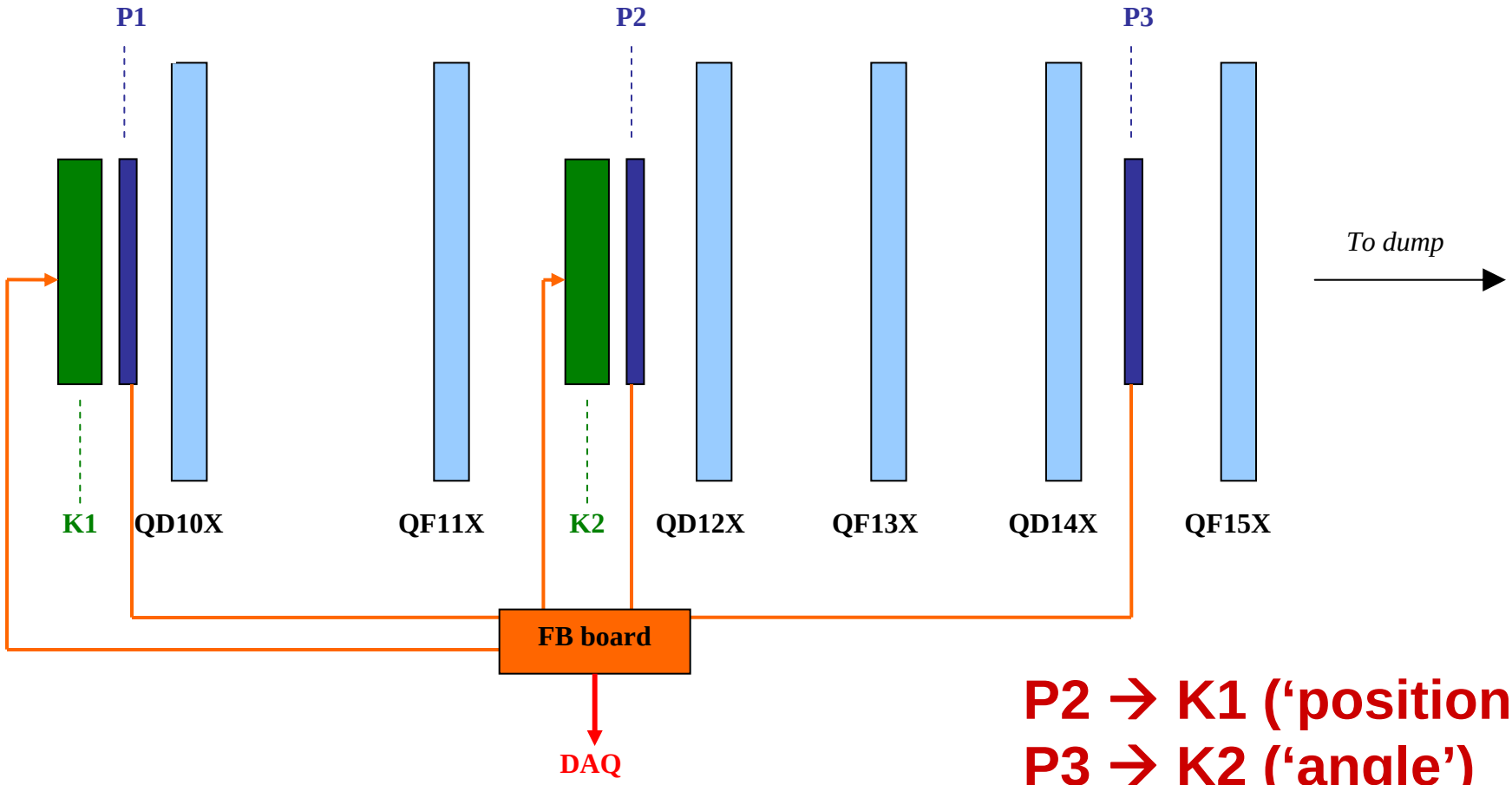


→ beam feedback along single axis (y)
with few micron resolution

FONT5 location

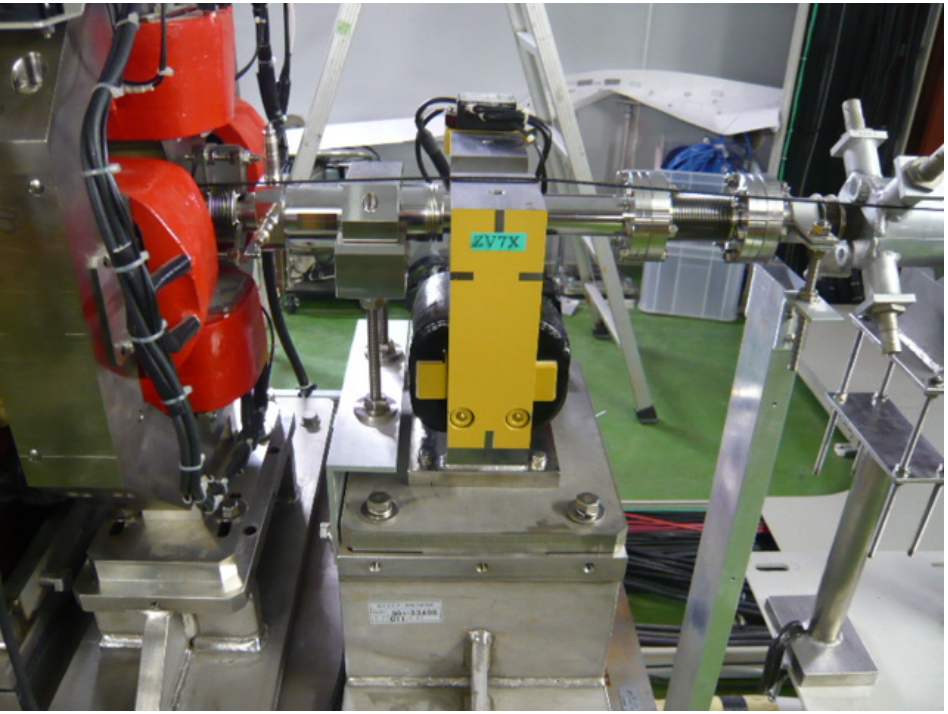


Flexible operation mode

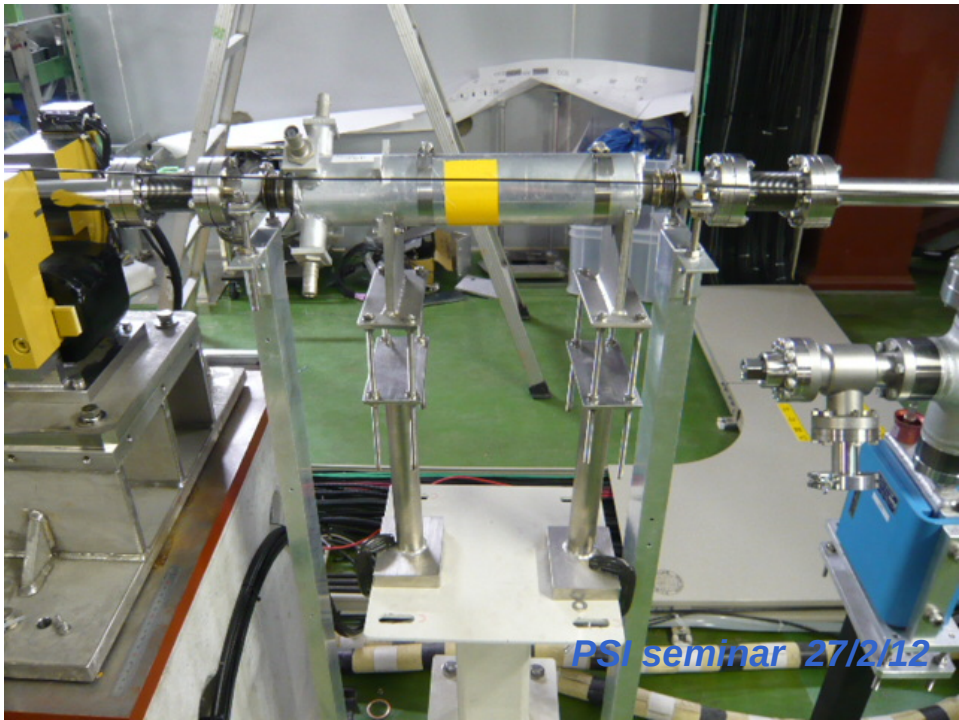


P2 → K1 ('position')
P3 → K2 ('angle')
P3 → K1

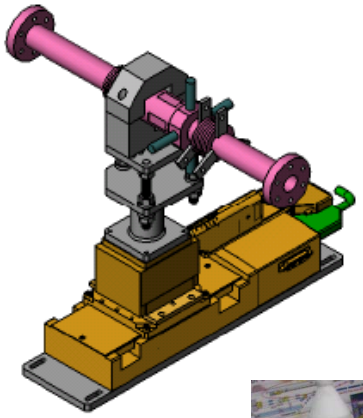
FONT5 hardware

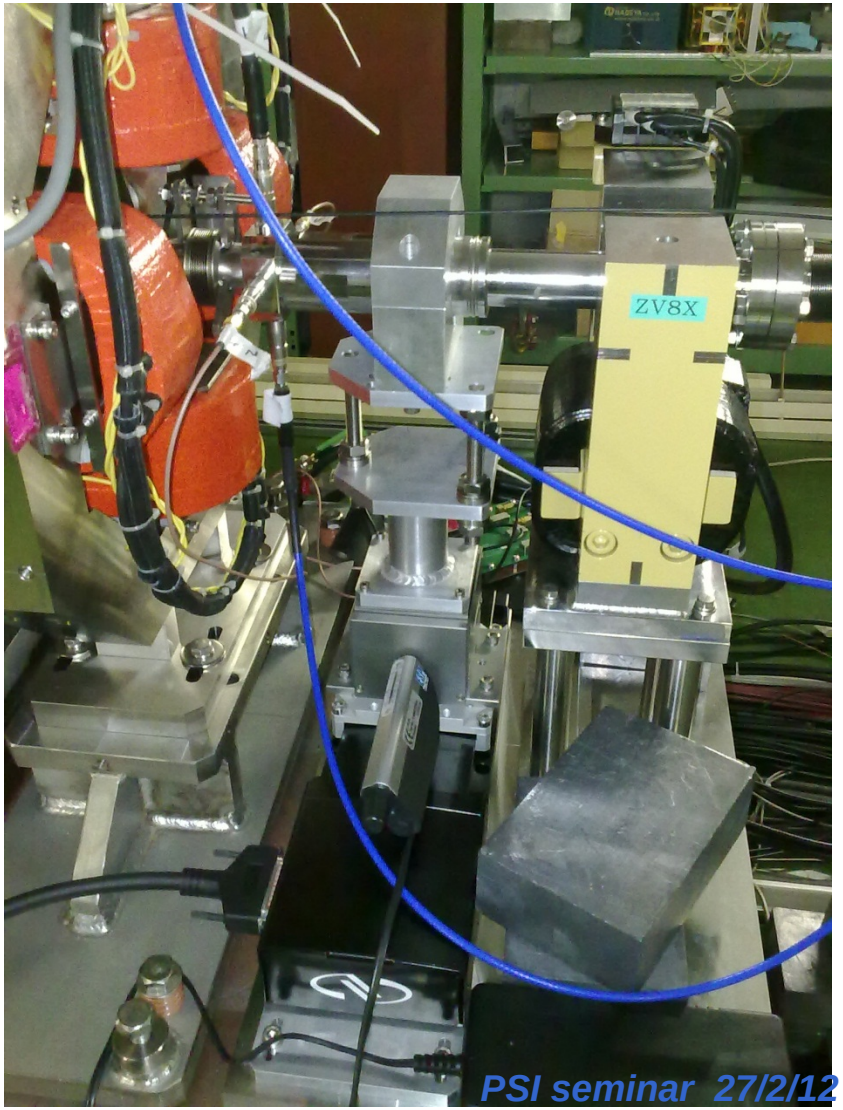


3 new BPMs and 2 new kickers installed in new ATF2 extraction line February 2009

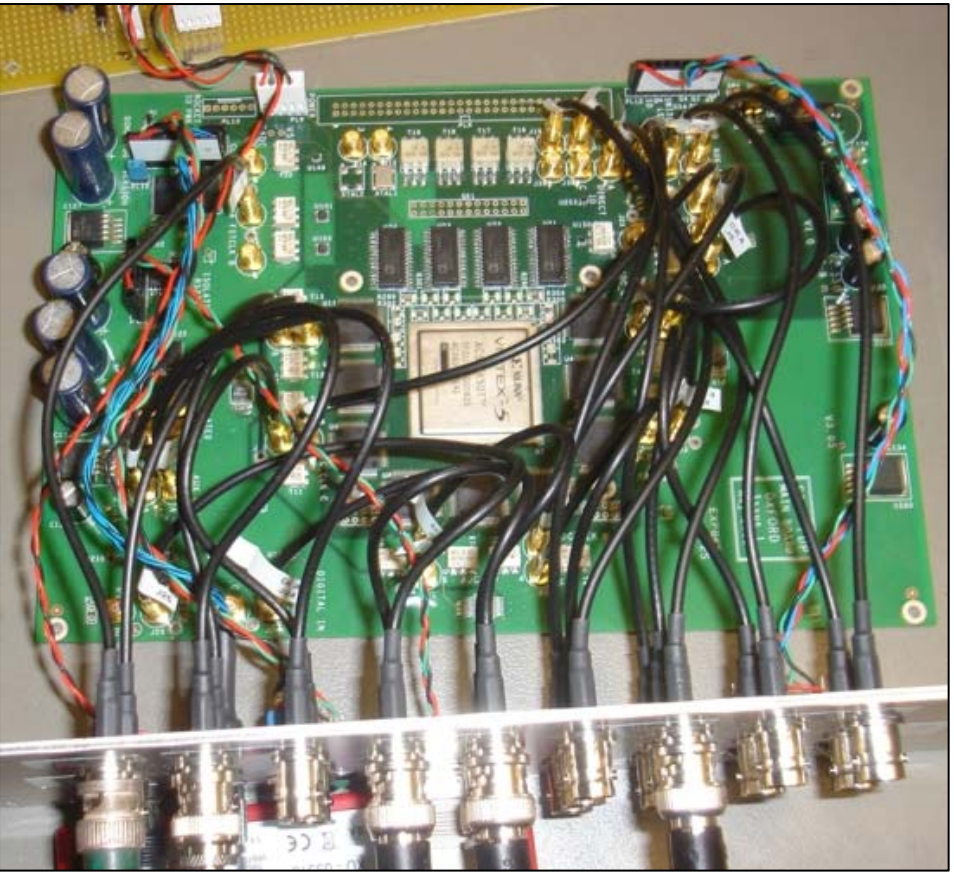


Valencia FONT BPM movers





New FONT5 digital FB board



Xilinx Virtex5 FPGA

9 ADC input channels (TI ADS5474)

4 DAC output channels (AD9744)

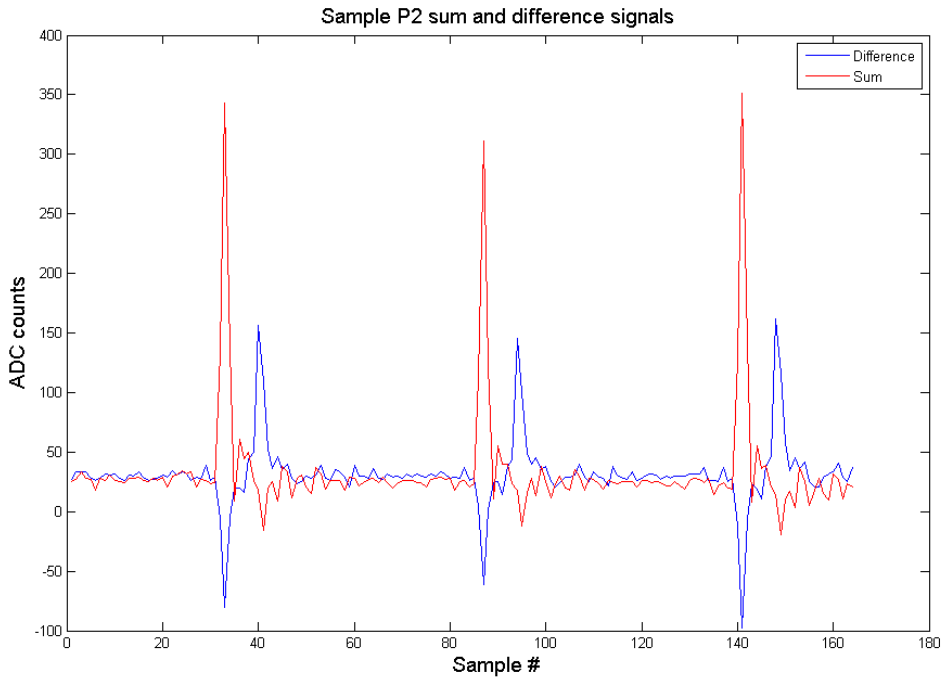
Clocked at 357 MHz phase-locked to beam

4x faster than FONT4

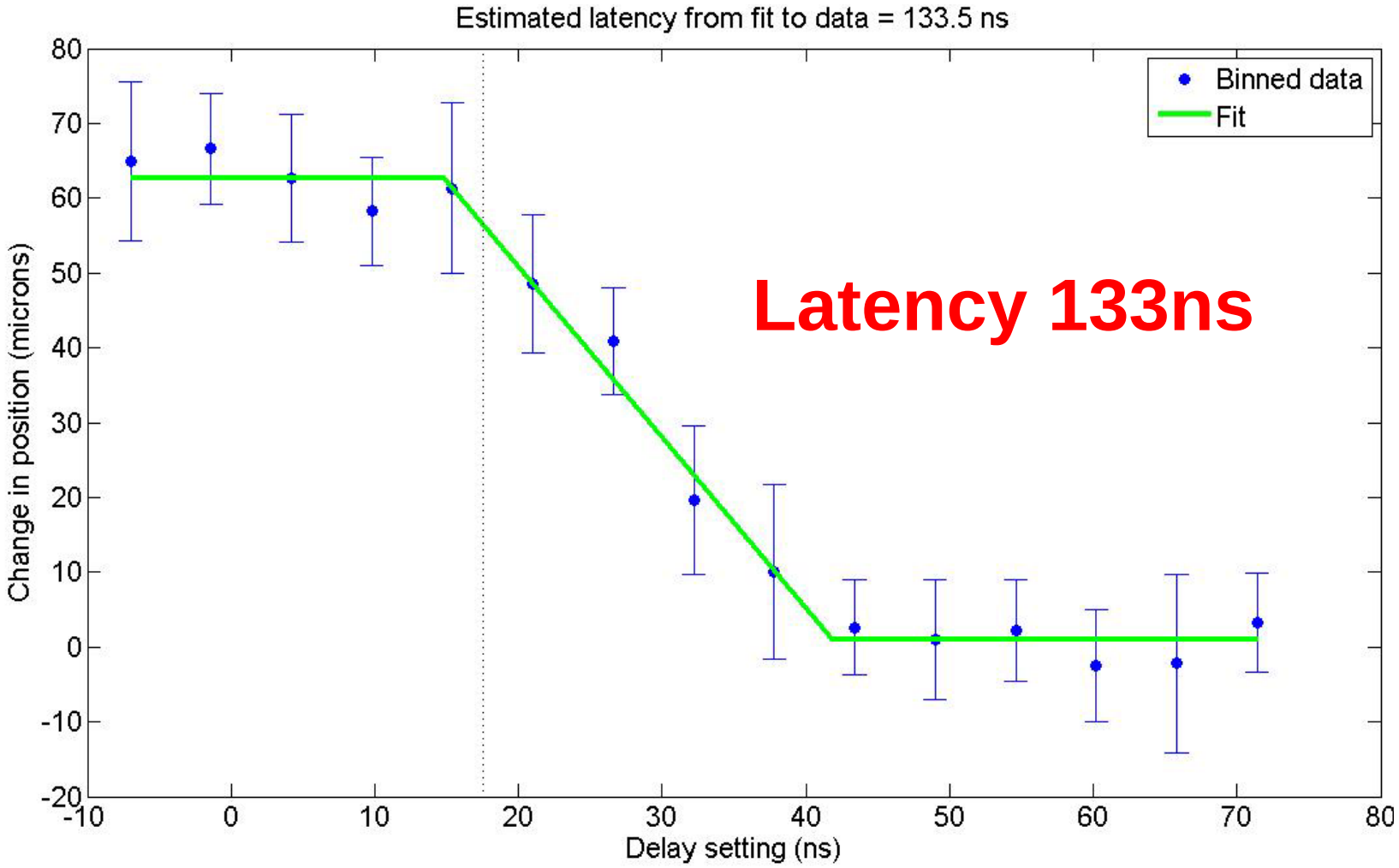
FONT5 DAQ

One damping ring cycle (463ns) data returned each pulse:

- **RS232 over ethernet**
- **All BPM sum (charge) and difference signals**
- **Absolute sample time adjustable in 70ps taps: accurate peak sampling**
- **Ratio of difference to sum peaks gives y-position**
- **Pedestal subtraction w. on-board trim DACs (no latency gain)**



FONT5 latency: P2 → K1 loop



Latency estimate

- Time of flight kicker – BPM: 12ns
- Signal return time BPM – kicker: 32ns

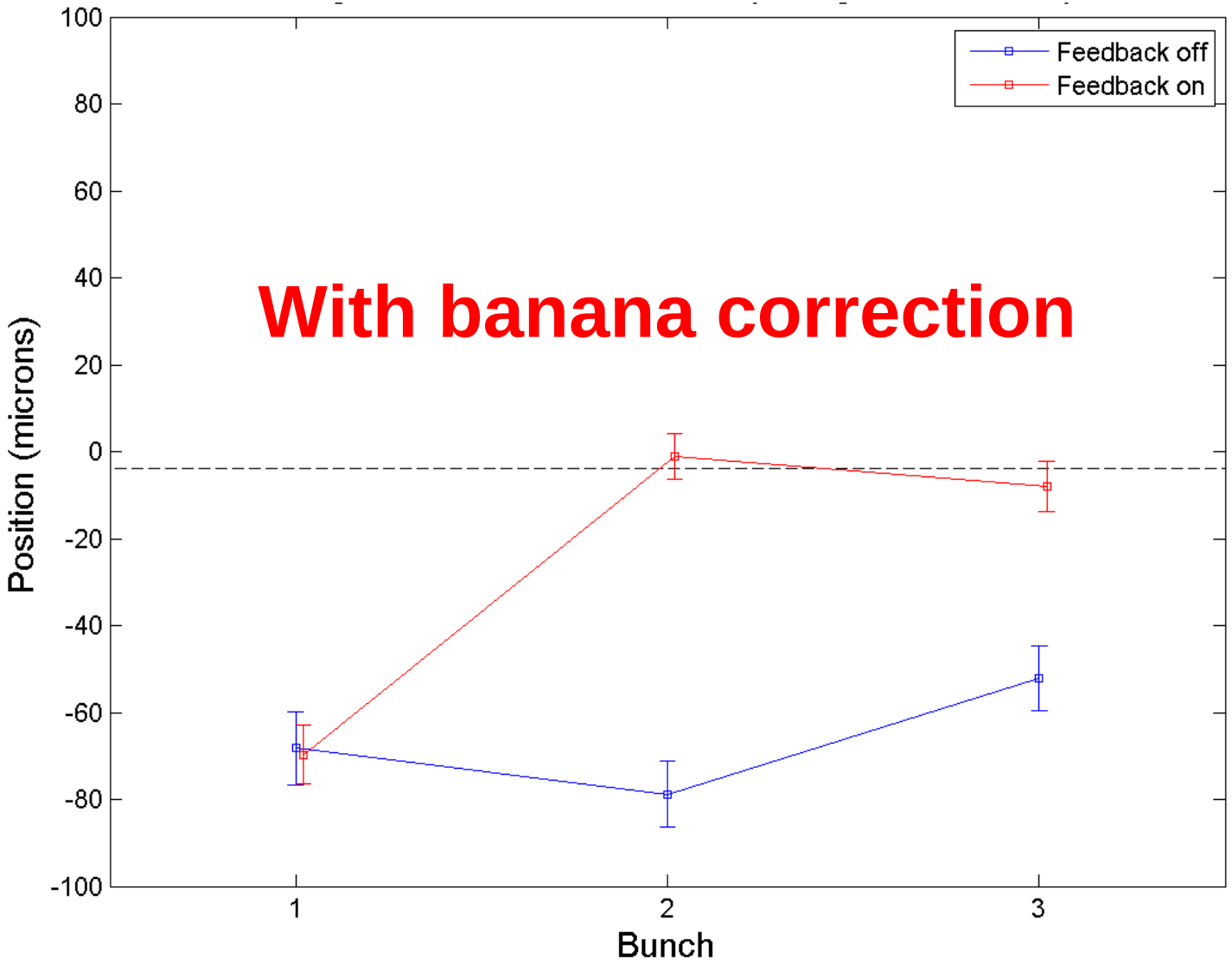
  Irreducible latency: 44ns

- BPM processor: 10ns
- ADC/DAC (4.5 357 MHz cycles) 14ns
- Signal processing (8 357 MHz cycles) 22ns
- FPGA i/o 3ns
- Amplifier 35ns
- Kicker fill time 3ns

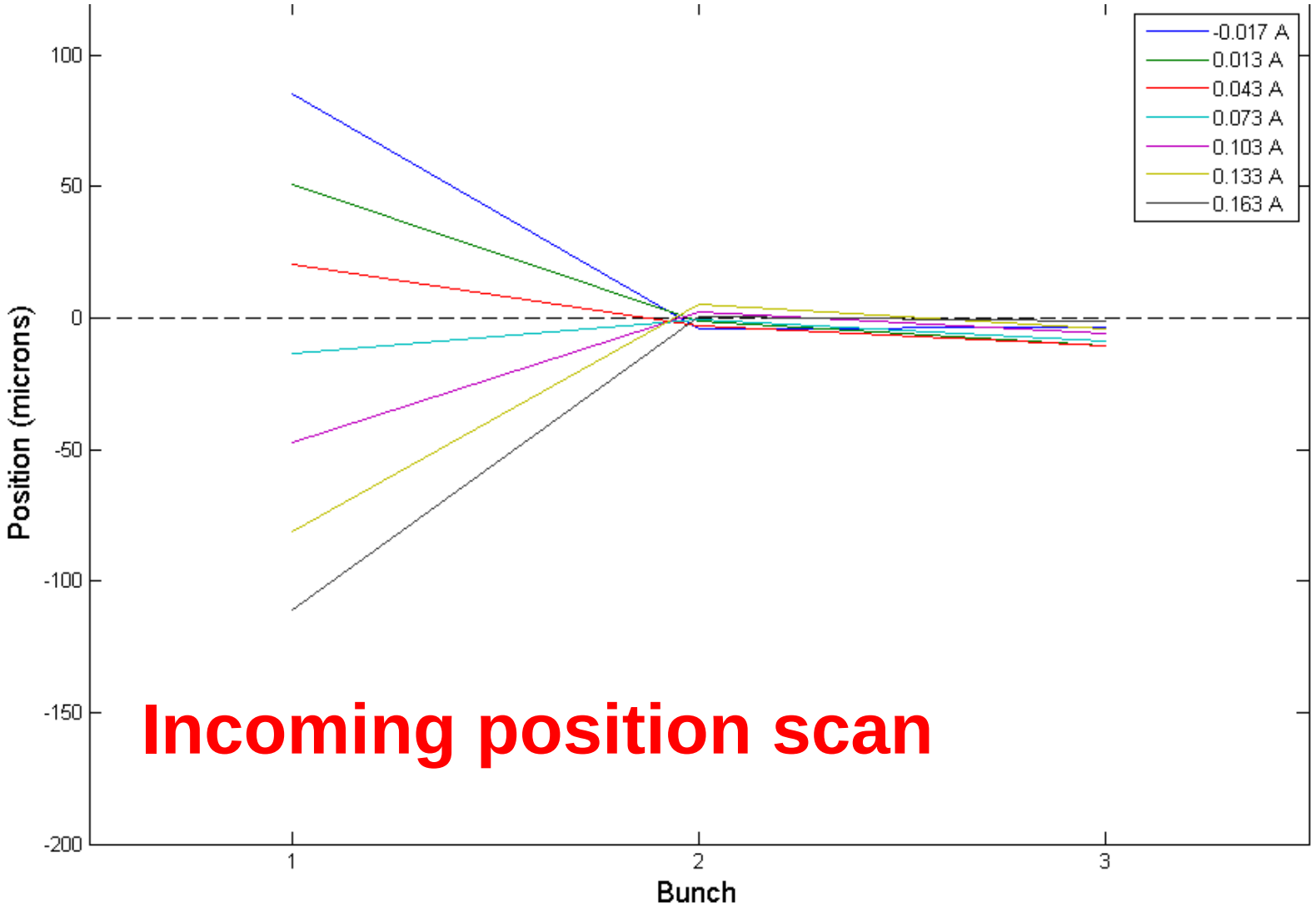
  Electronics latency: 87ns

- Total latency budget: 131ns

P2 → K1 loop performance

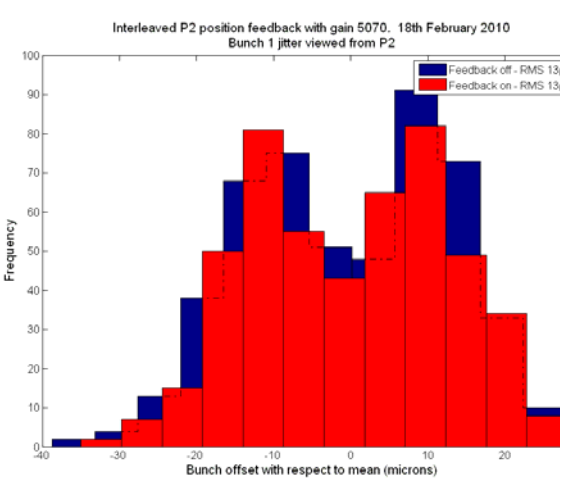


P2 → K1 loop performance

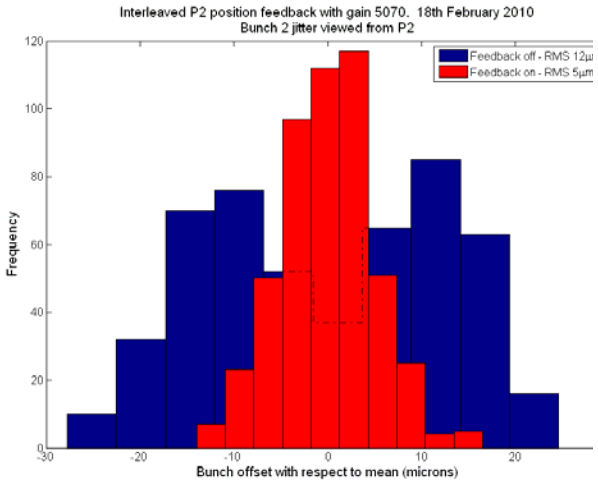


P2 → K1 loop jitter reduction

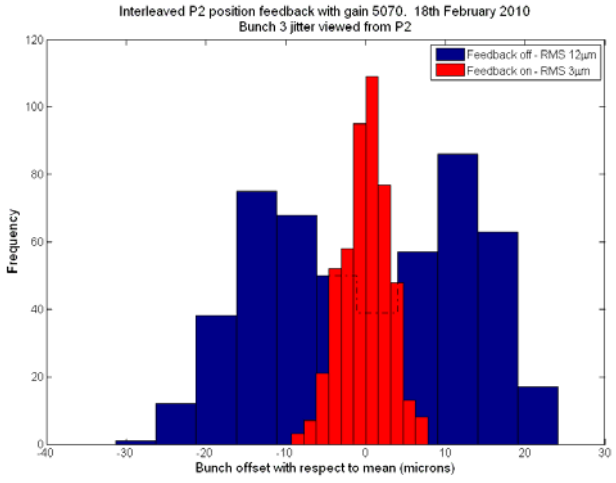
Bunch 1



Bunch 2



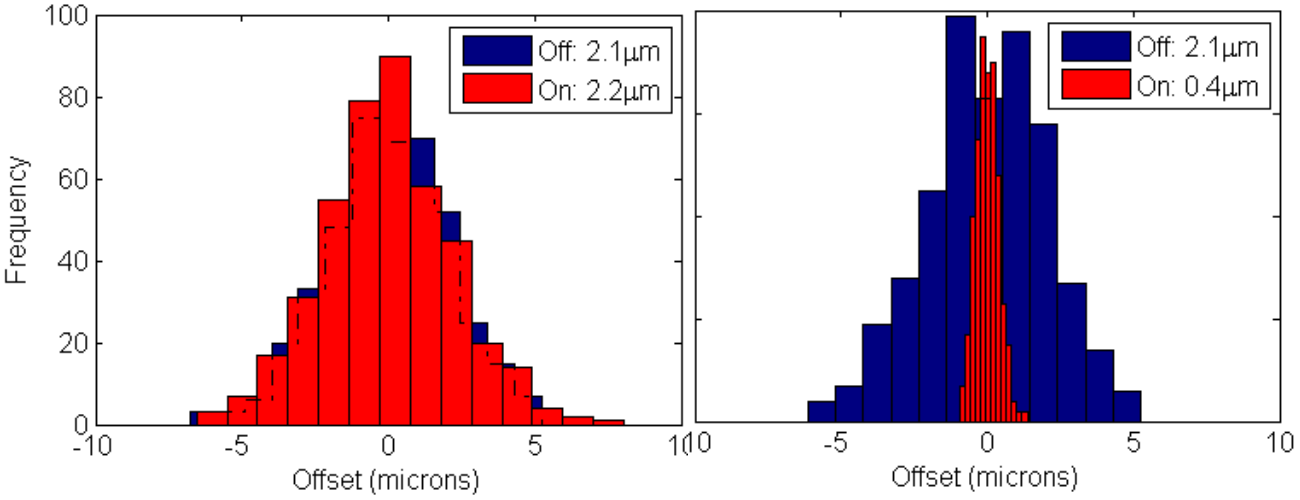
Bunch 3



13 um → 5 um → 3 um

P2 → K1 loop jitter reduction

Bunch 1 **Bunch 2**

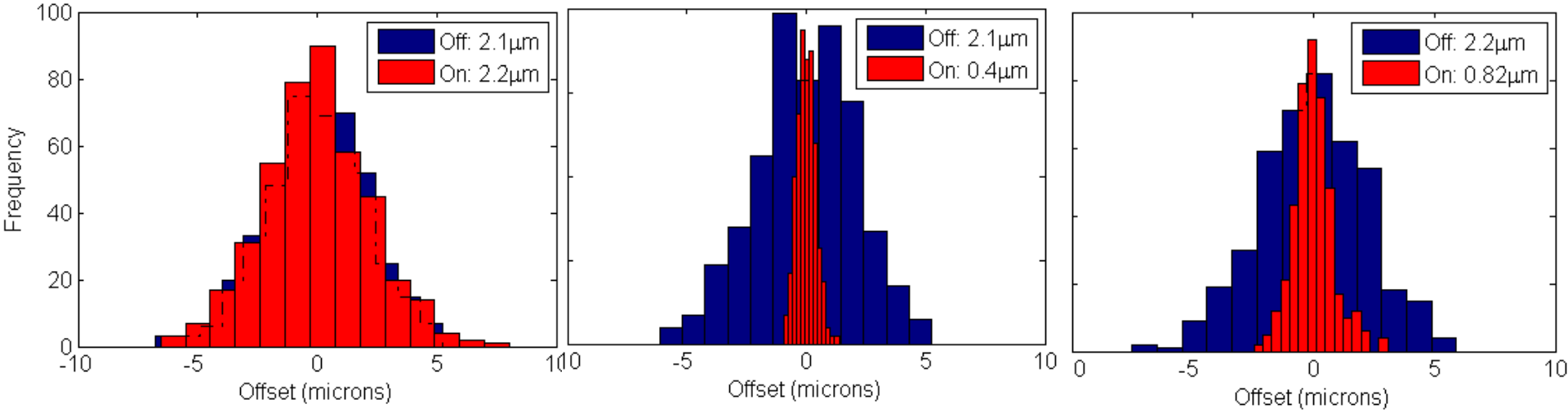


2.1 um → 0.4 um

Factor of 5 jitter reduction

P2 → K1 loop jitter reduction

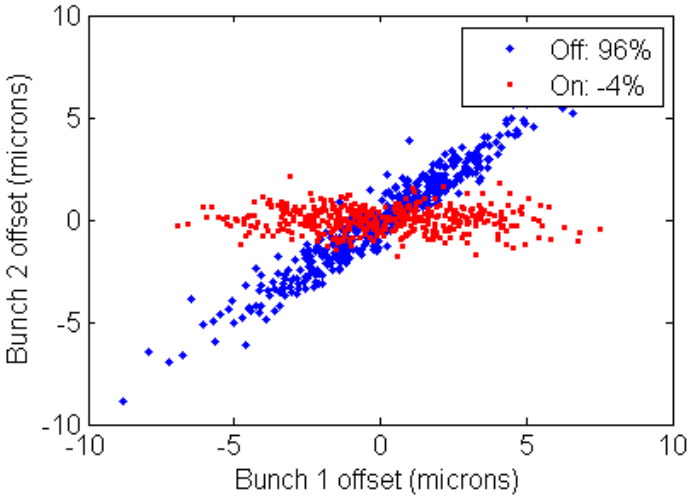
Bunch 1 **Bunch 2** **Bunch 3**



2.1 um → **0.4 um** → **0.8 um**

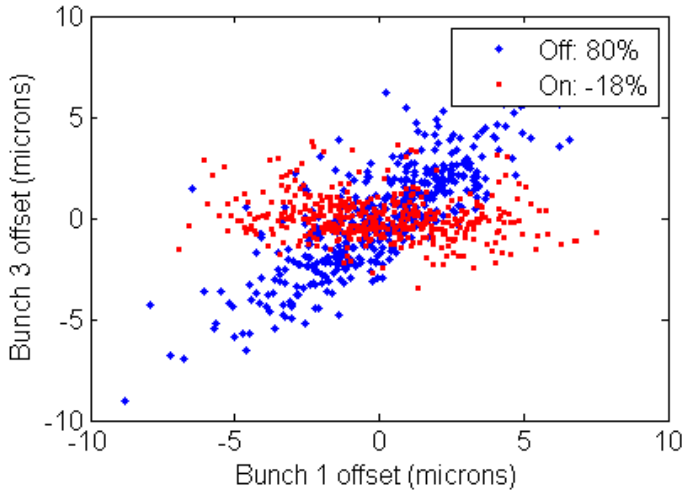
Bunch correlations

Bunch 2



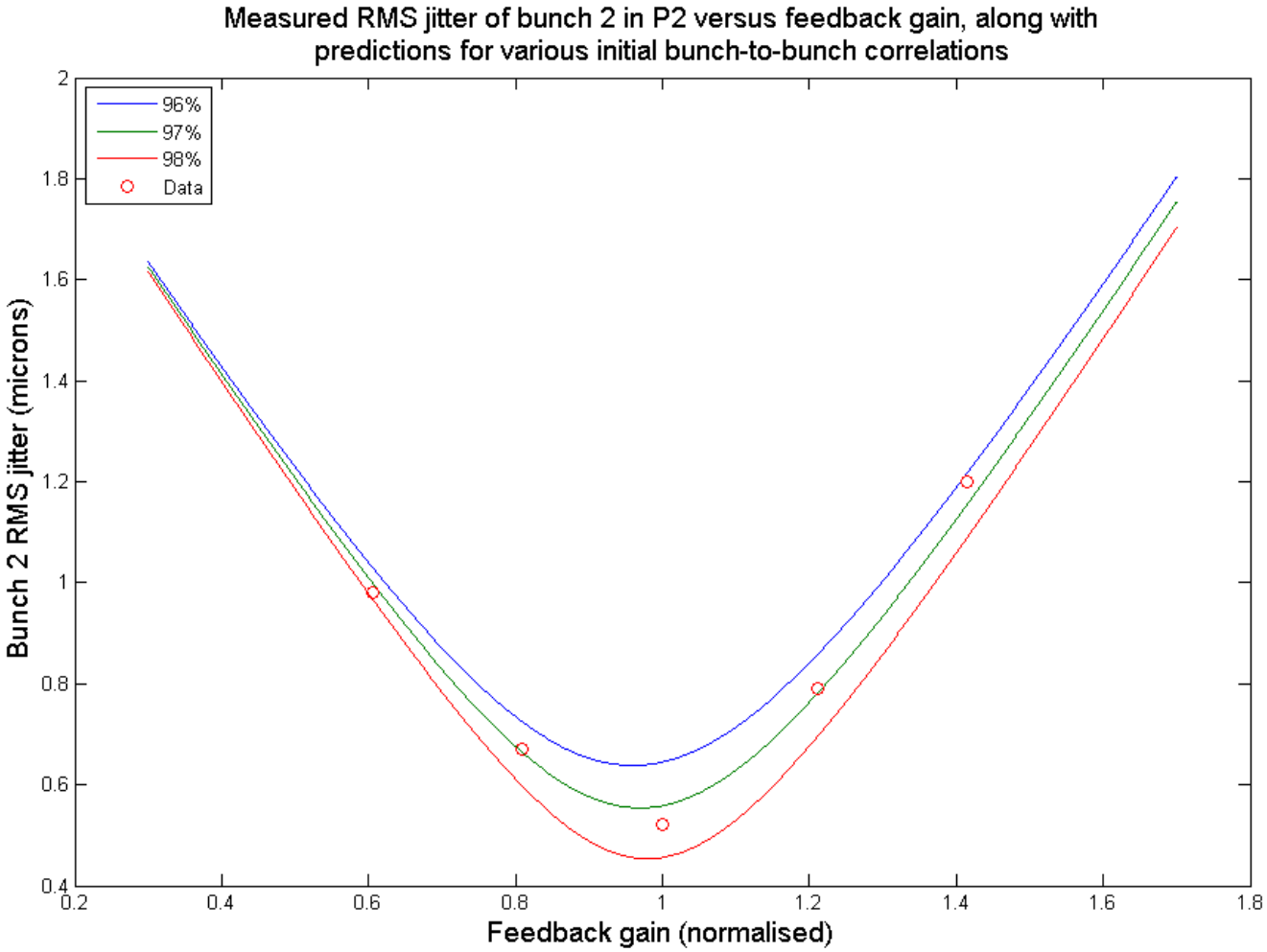
Bunch 1

Bunch 3

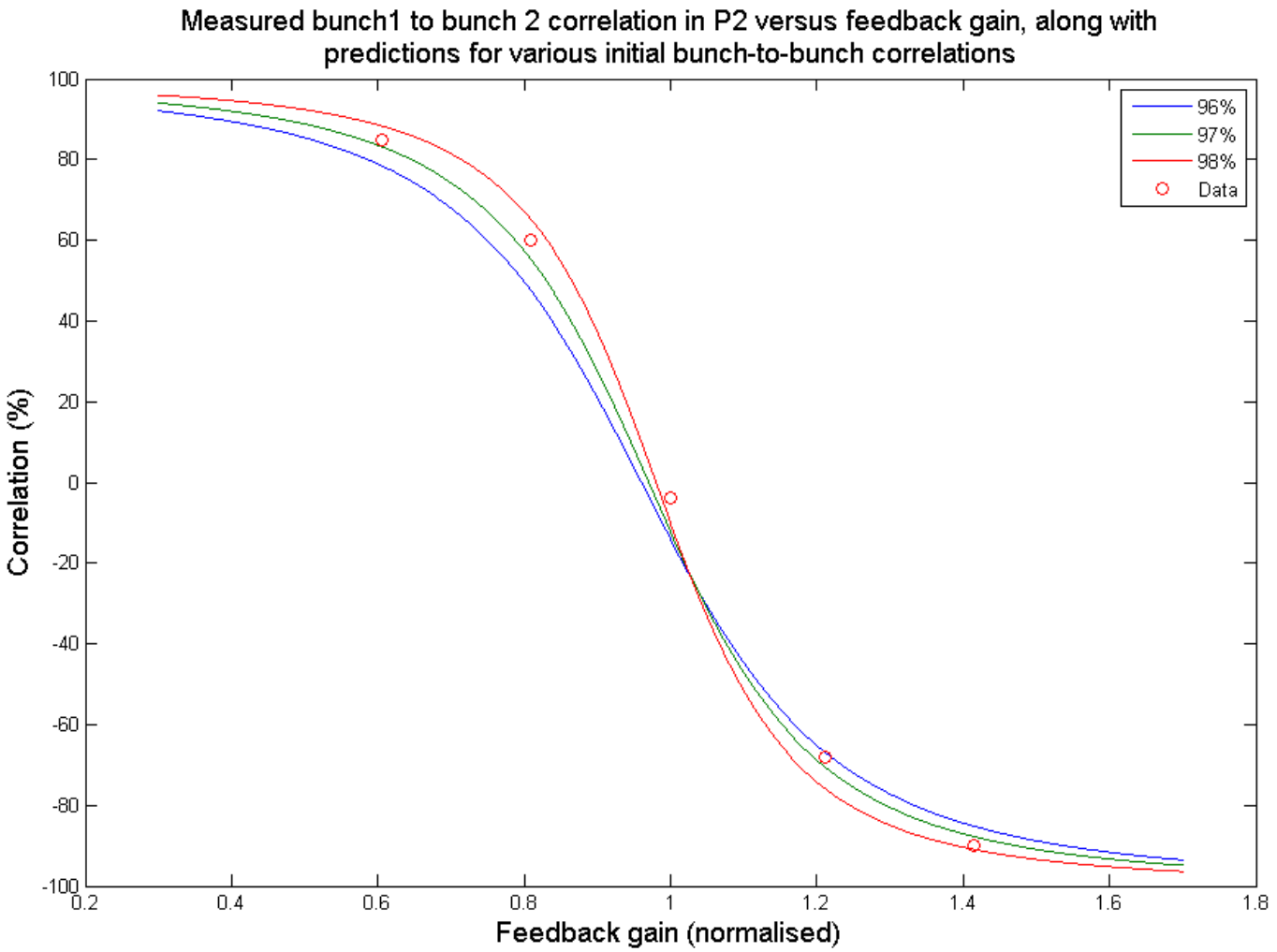


Bunch 1

FB correction vs. gain



Bunch correlations vs. gain



BPM processor resolution tests

- **3 BPM processors (5,7,10) on BPM P2**

  25/10/11 8-hour shift:

  0.55 0.56 0.60 μm

  0.56 0.54 0.51 μm

  0.53 0.40 0.35 μm

  0.50 0.35 0.33 μm

  0.45 0.44 0.35 μm

  0.50 0.43 0.36 μm

Beam position jitter 3- 4 μm

BPM processor resolution tests

- **3 BPM processors (5,7,10) on BPM P2**

25/10/11 8-hour shift:

0.55 0.56 0.60 μm

0.56 0.54 0.51 μm

0.53 0.40 0.35 μm

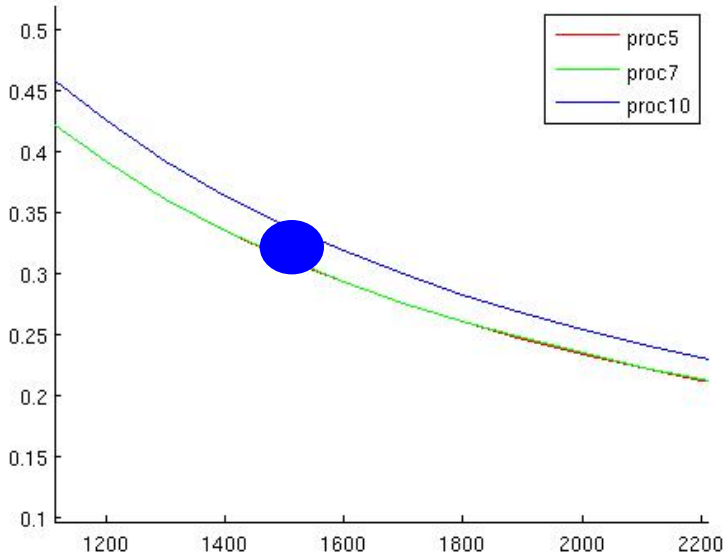
0.50 0.35 0.33 μm

0.45 0.44 0.35 μm

0.50 0.43 0.36 μm

Beam position jitter 3- 4 μm

expectation from ADC noise alone:

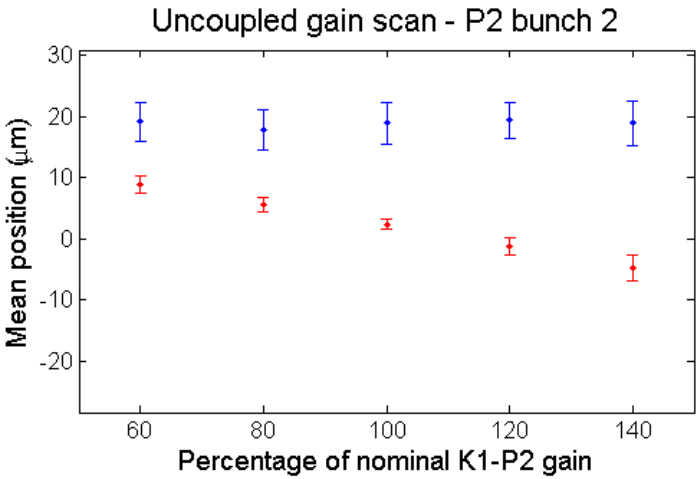


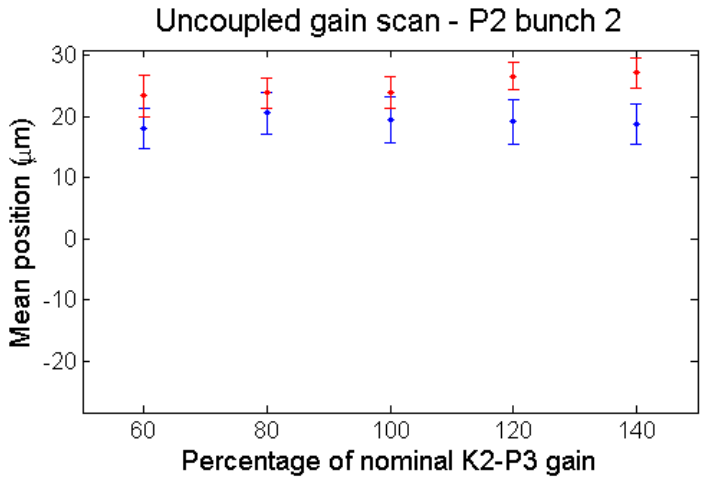
Gain matrix

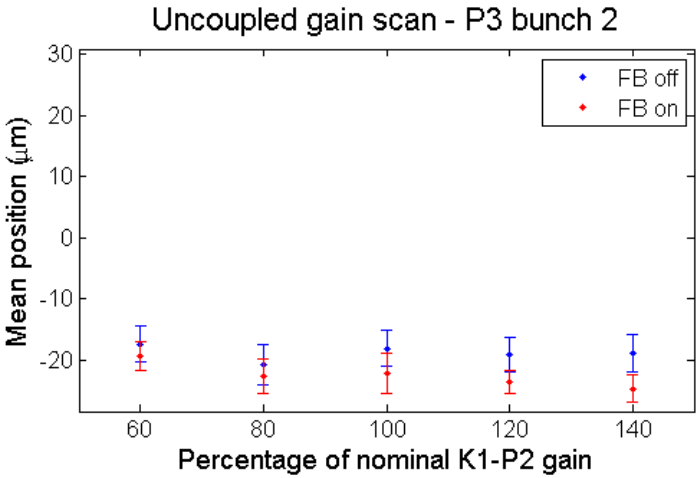
G (K1 - P2) **G (K1 - P3)**

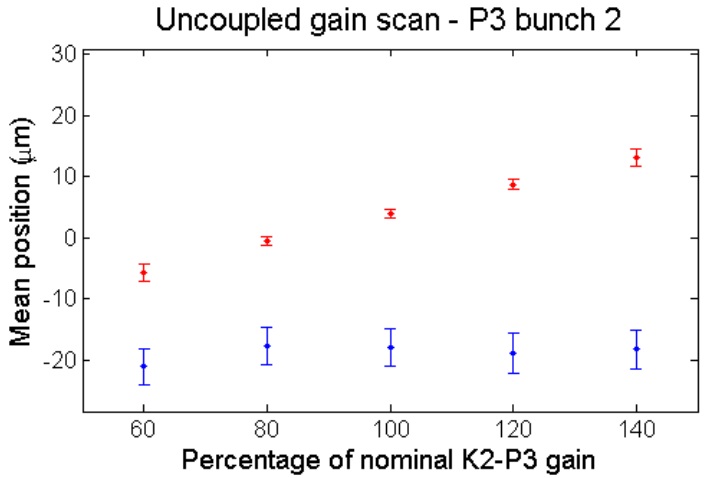
G (K2 - P2) **G (K2 - P3)**

Uncoupled loop gain scans

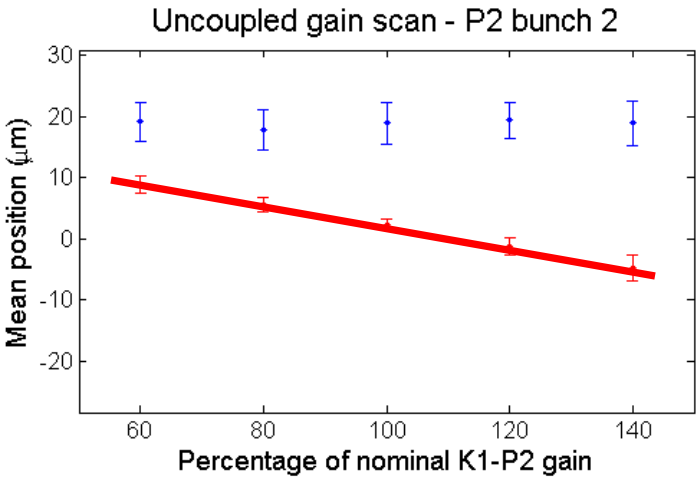


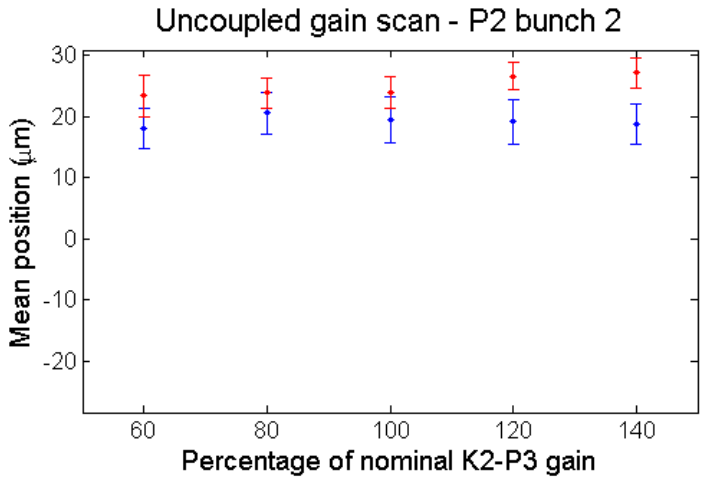


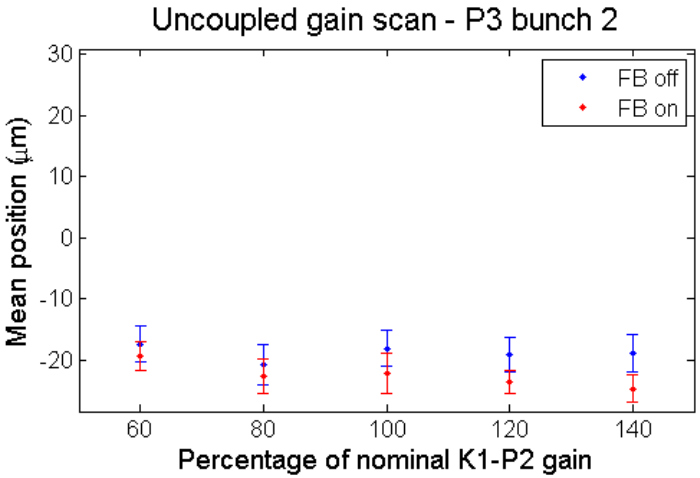


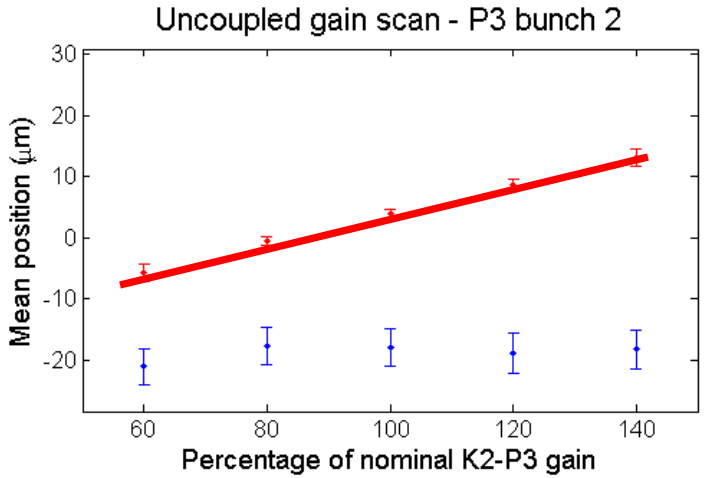


Uncoupled loop gain scans

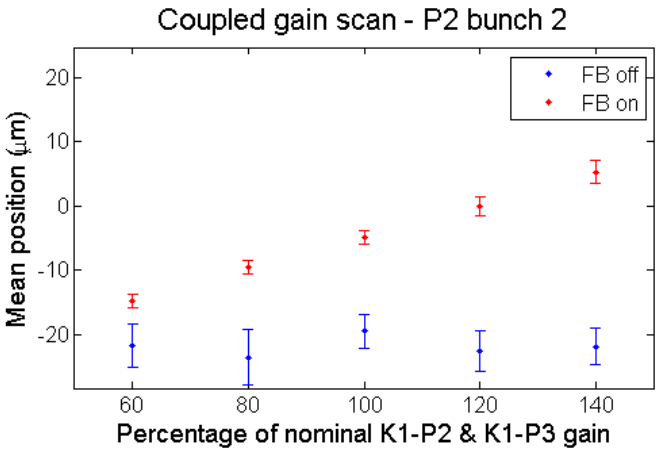


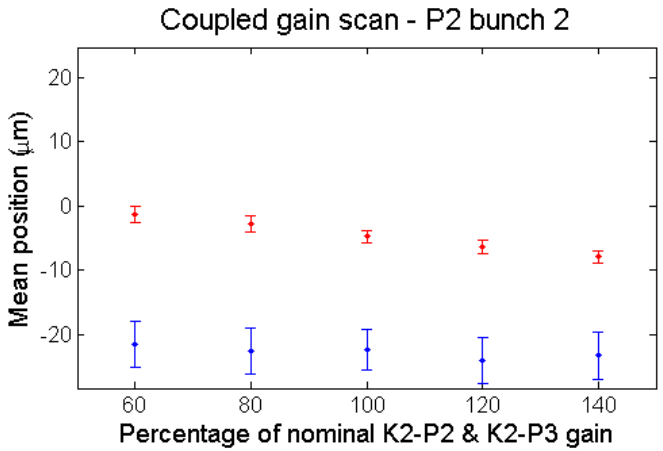


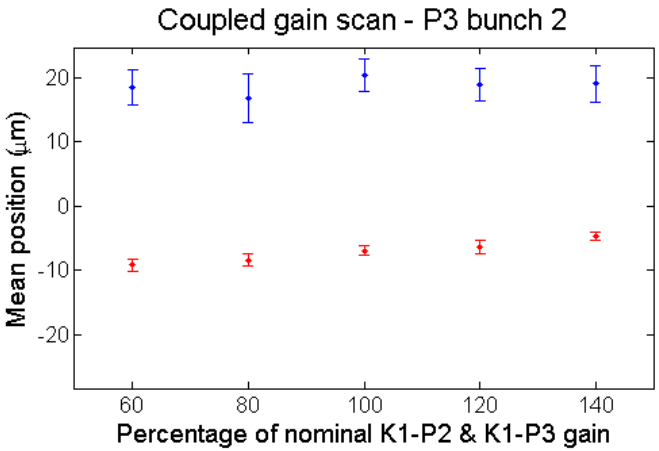


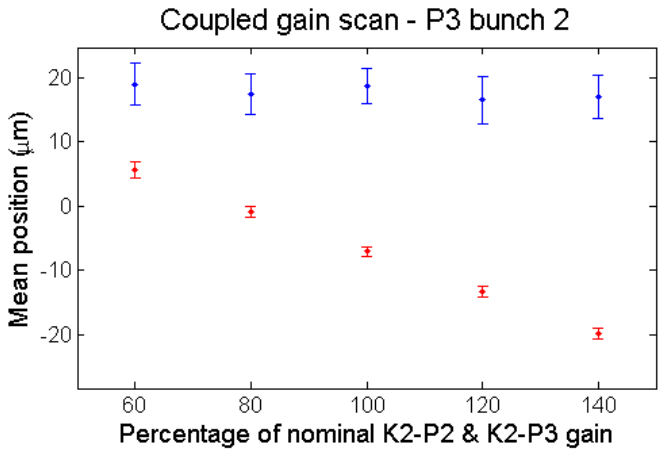


Coupled loop gain scans

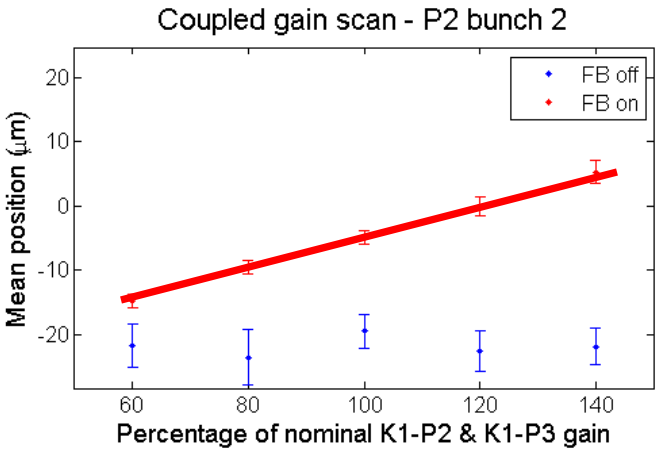


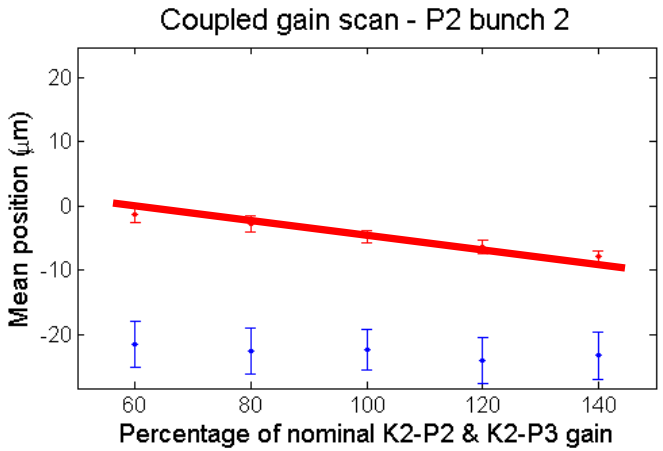


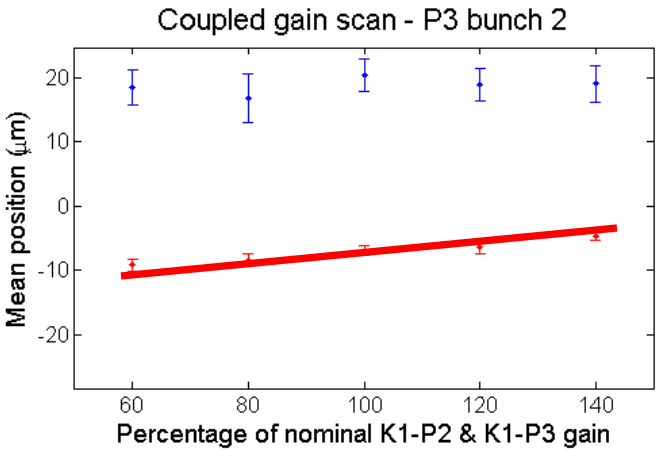


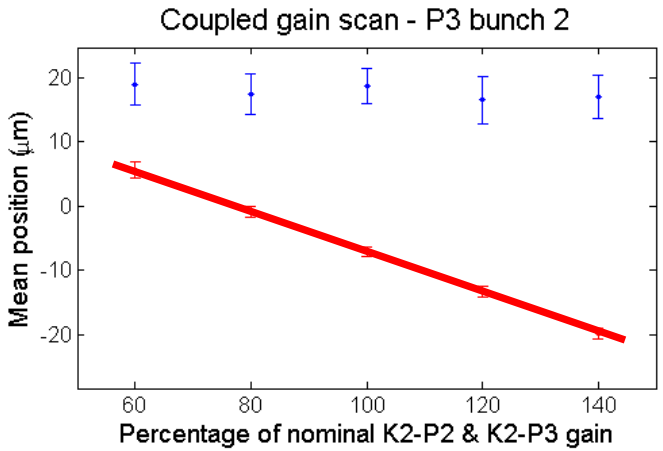


Coupled loop gain scans









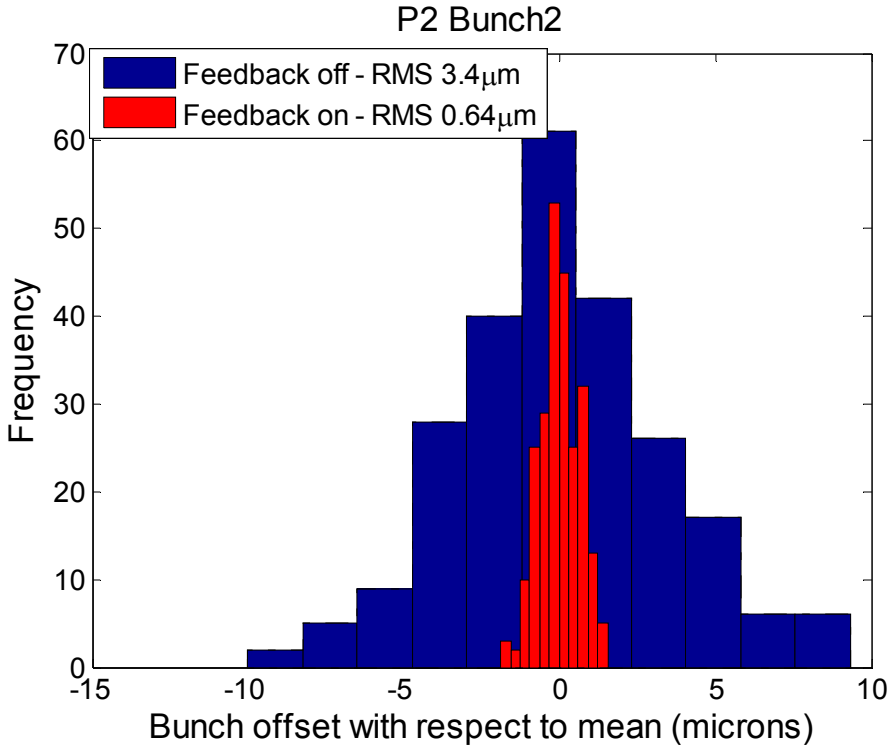
Feedback Performance

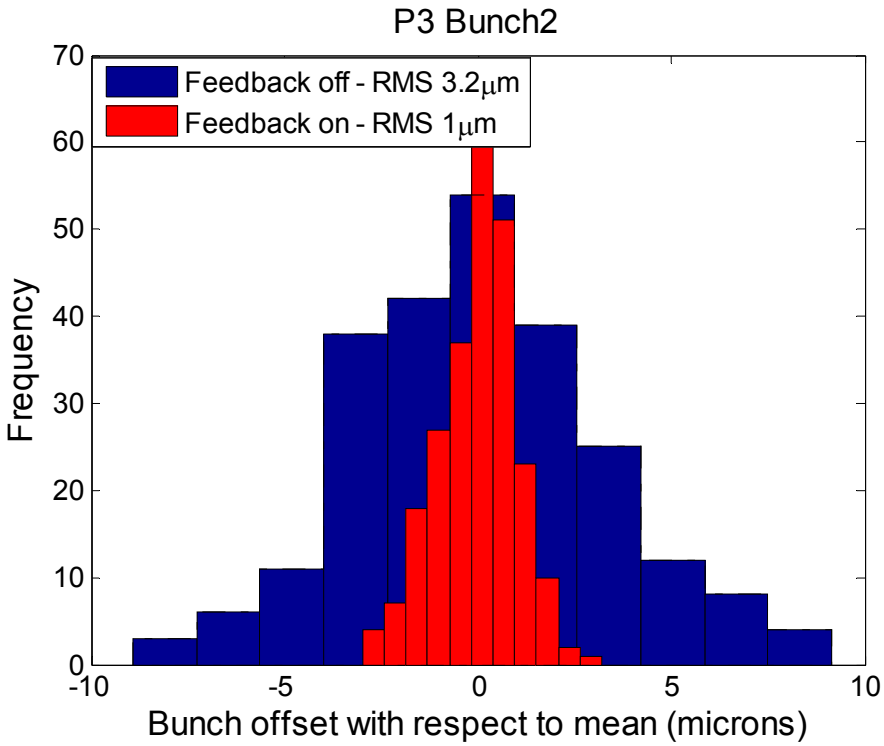
(example FB Run 6 13/12)

bunch	1	2
	FB off	FB off
Jitter P2	3.42	3.42
P3	3.24	3.21

Feedback Performance

(example FB Run 6 13/12)





Feedback Performance

(example FB Run 6 13/12)

bunch	1		2	
	FB off	on	FB off	on
Jitter P2	3.42	3.39	3.42	0.64
P3	3.24	3.16	3.21	1.04

Feedback Performance

(example FB Run 6 13/12)

bunch	1		2		
	FB off	on	FB off	on	Pred.
Jitter P2	3.42	3.39	3.42	0.64	
1-2 correl 98%					0.67
P3	3.24	3.16	3.21	1.04	
1-2 correl 97%					0.83

$$\sigma_2'^2 = \sigma_1^2 + \sigma_2^2 - 2\sigma_1\sigma_2\rho_{12} \geq 2\sigma_r^2$$

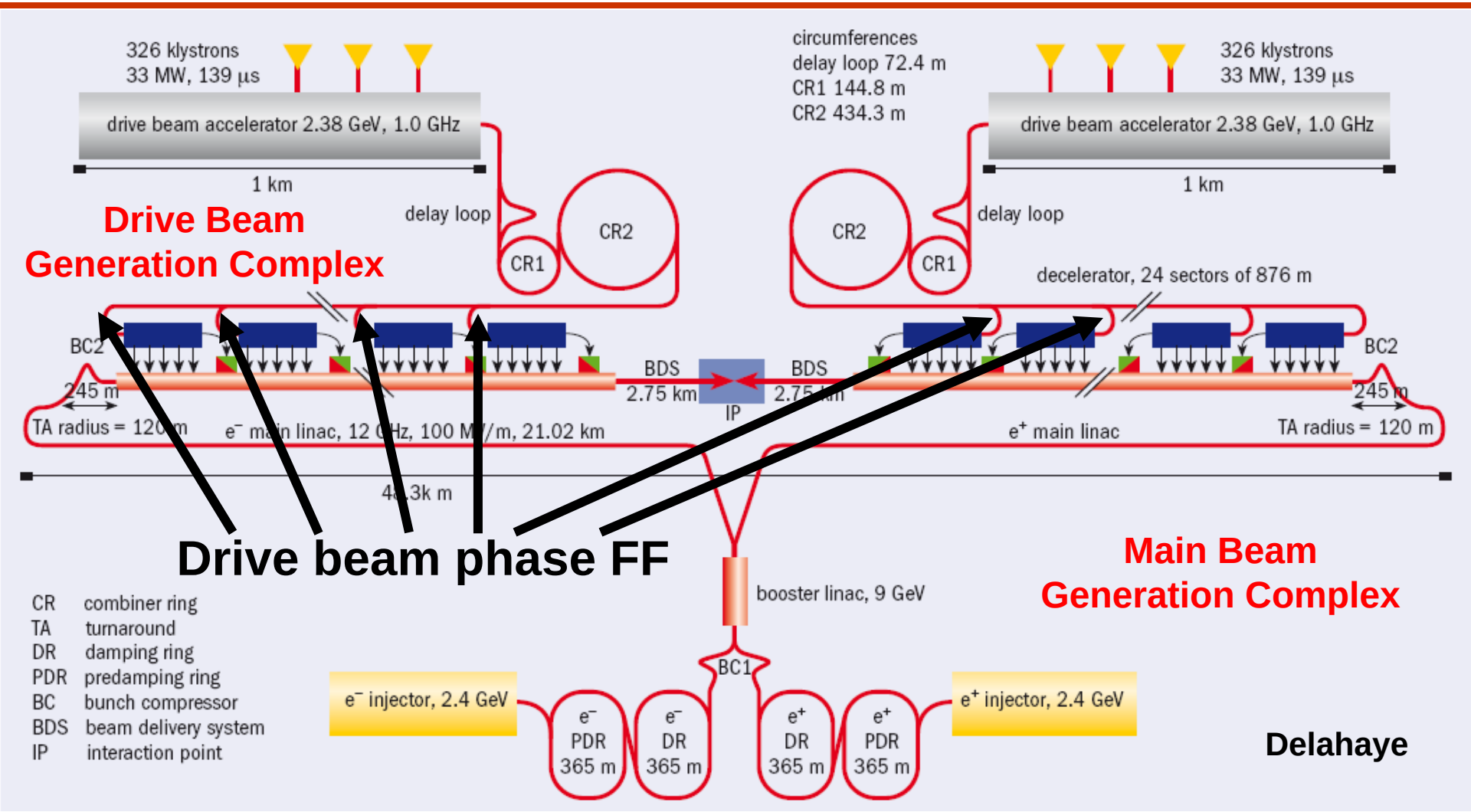
Summary

- **Intra-train beam feedback concept well advanced**
- **Conceptually-engineered designs for ILC + CLIC**
- **All-analogue prototypes (CLIC) developed and tested at NLCTA + ATF:**

  → electronics latency c. 13ns
- **Digital prototypes developed and tested at ATF + ATF2:**

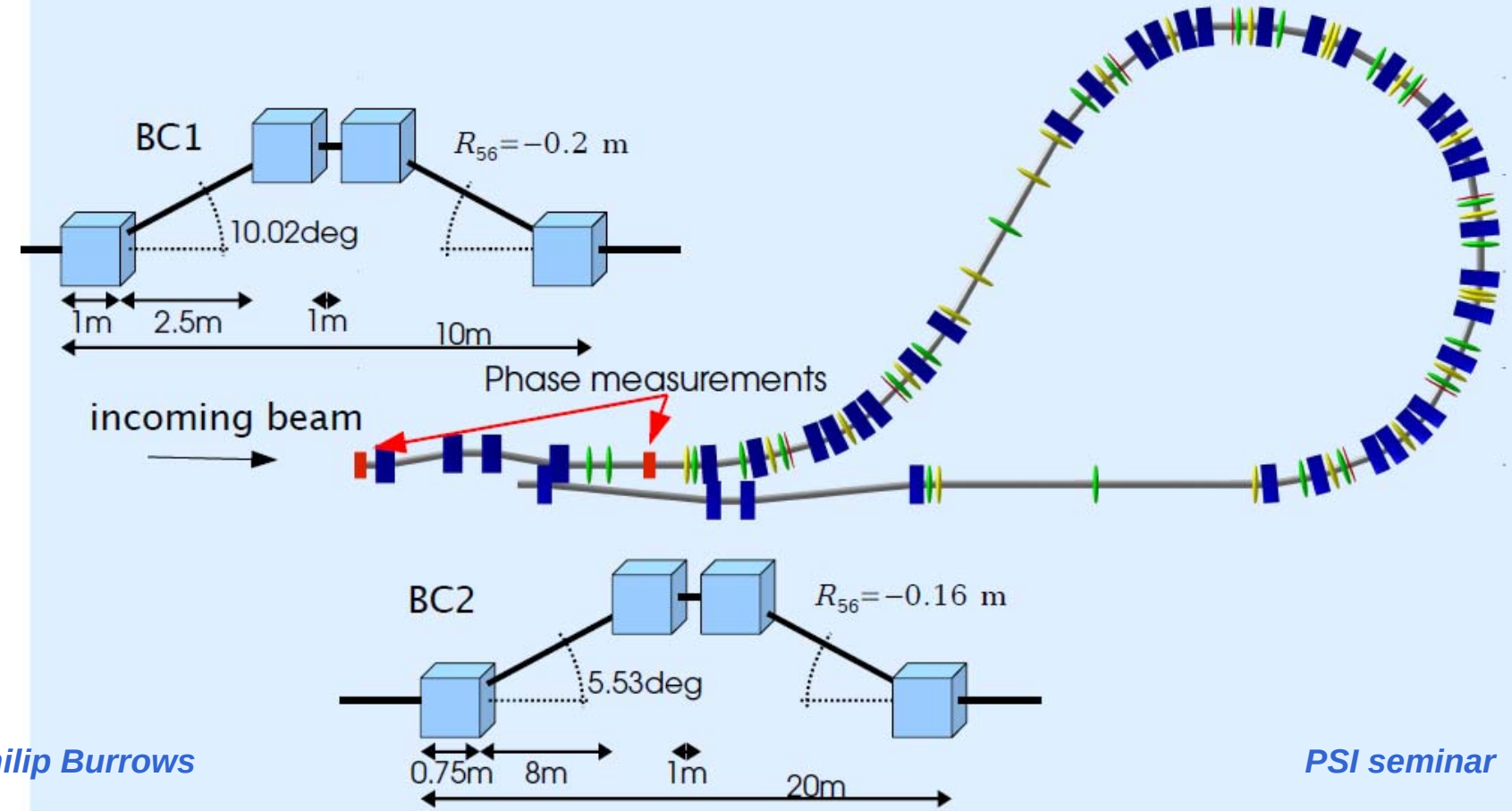
  → electronics latency c. 90ns
- **Conceptual design for CLIC phase feed-forward**
- **Techniques generally applicable**

Compact Linear Collider (CLIC)

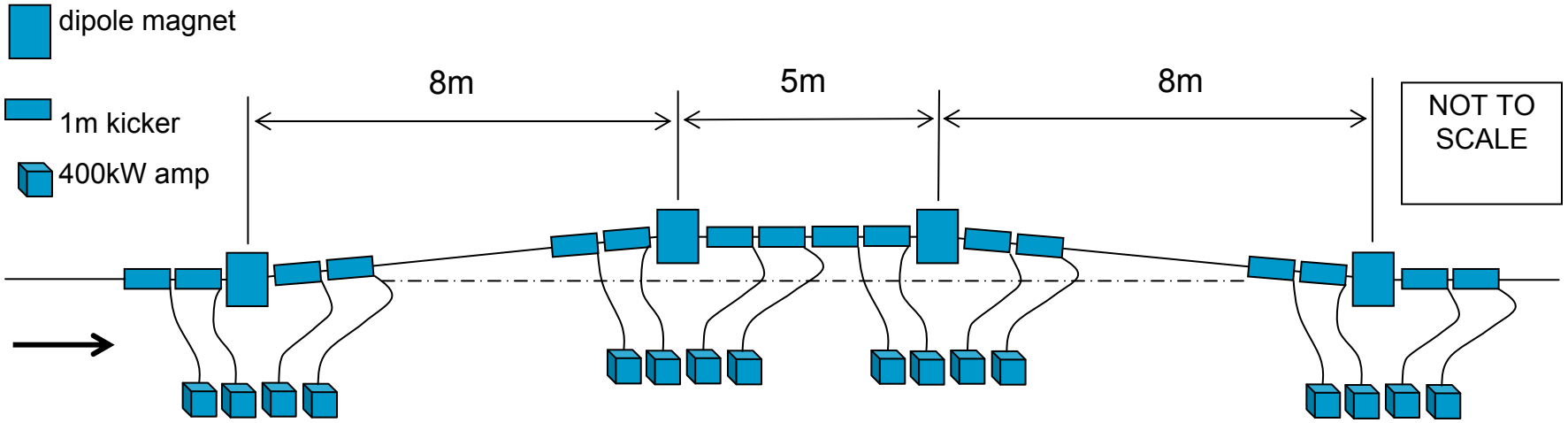


CLIC drive beam phase FF

Basic idea: Measurement of phase and energy error in front of the loop, phase correction behind the loop by adjusting deflection in the second chicane.

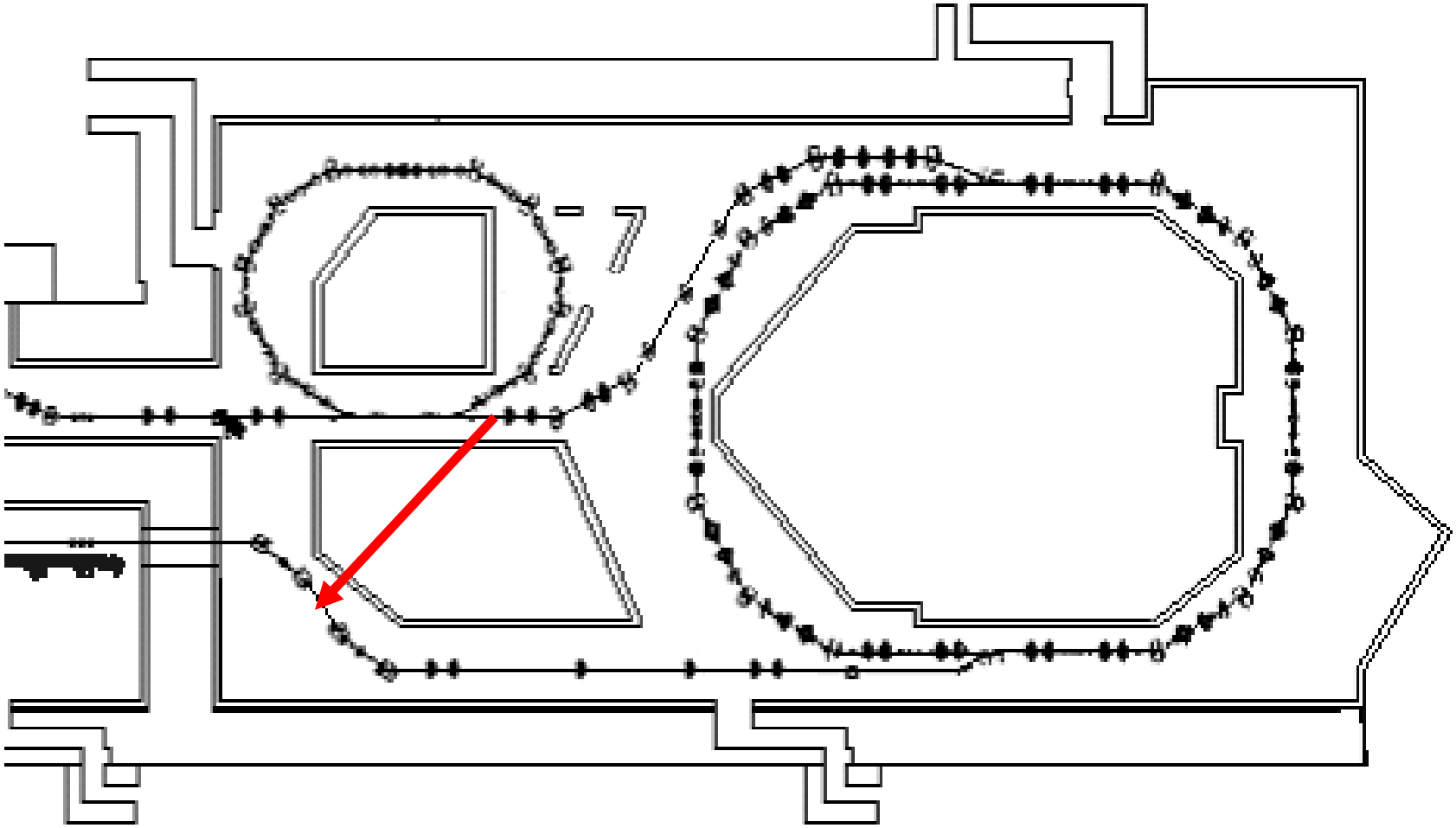


A Preliminary System Concept



- **+- 375 urad kick at each bend**
- **0.5% energy spread, 1m dispersion -> 5mm rms**
- **beam pipe diameter >> 50mm**
- **4 kickers at each bend**
- **> 400kW peak power amplifier to each kicker**

CTF3 phase FF prototype



Extra material

Beam tracking simulations

(Javier Resta Lopez)

Macroparticle tracking through the BDS using the code PLACET

Luminosity calculation using the code Guinea-Pig

Ground motion:

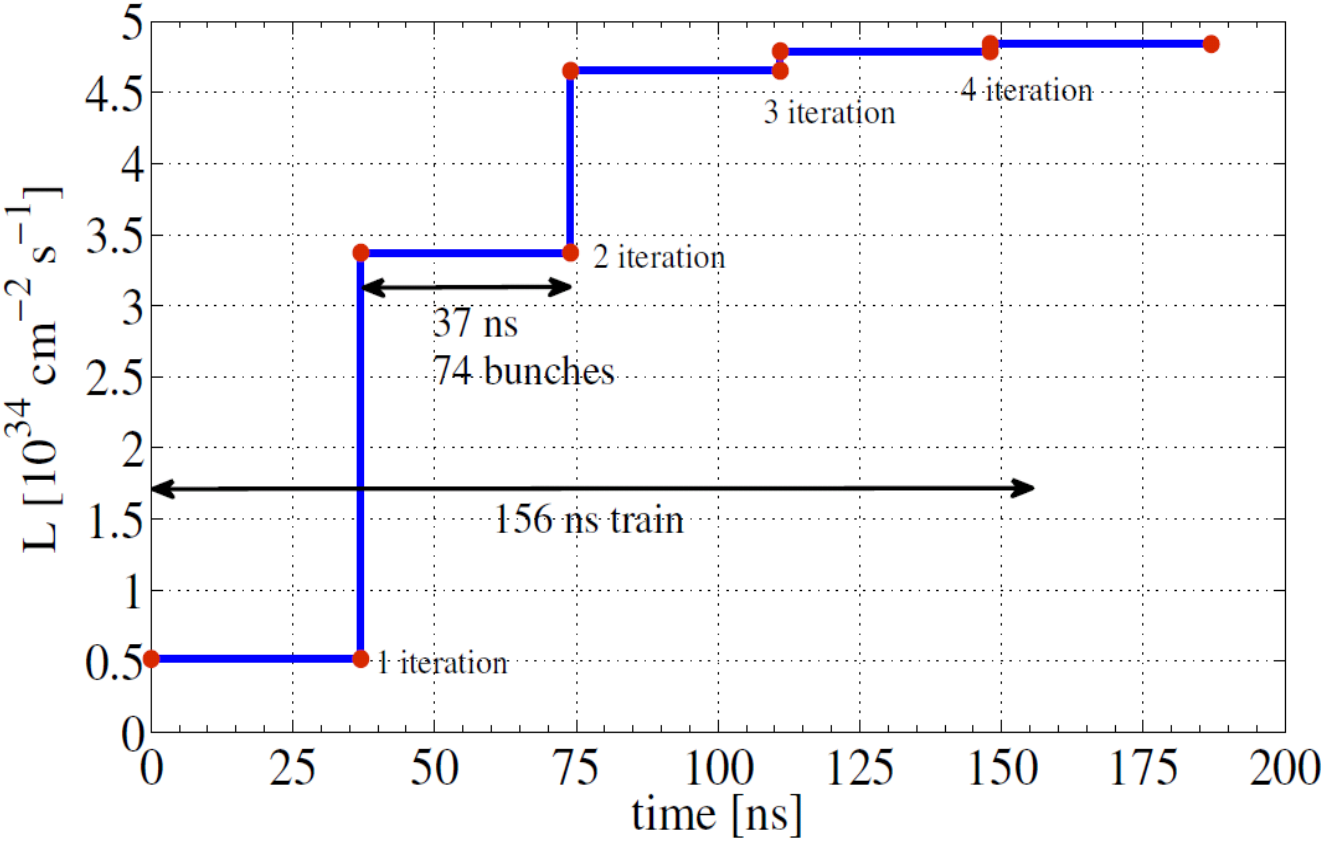
- **In the following simulations we apply 0.02 s (corresponding to f_{rep}=50 Hz) of GM (A. Seryi's models) to the CLIC BDS**

- **What is the RMS vertical beam-beam offset at the IP we have to deal with?**
  - **Simulation of 100 random seeds:**

GM model	rms Δy^* [nm] (in units of σ_y^*)
A (CERN)	0.035 (0.04)
B (SLAC and FNAL)	0.47 (0.52)
C (DESY)	8.9 (9.9)
K (KEK)	6.4 (7.1)

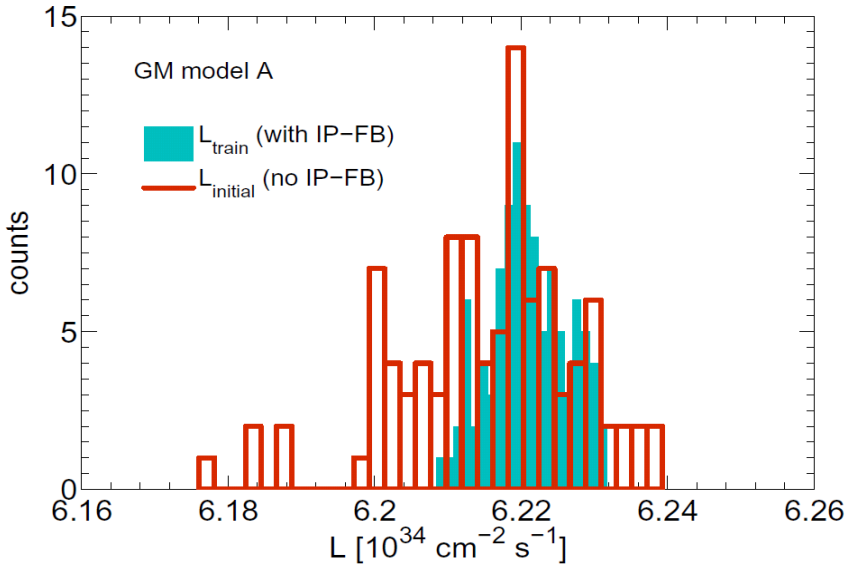
Luminosity performance with IP FB

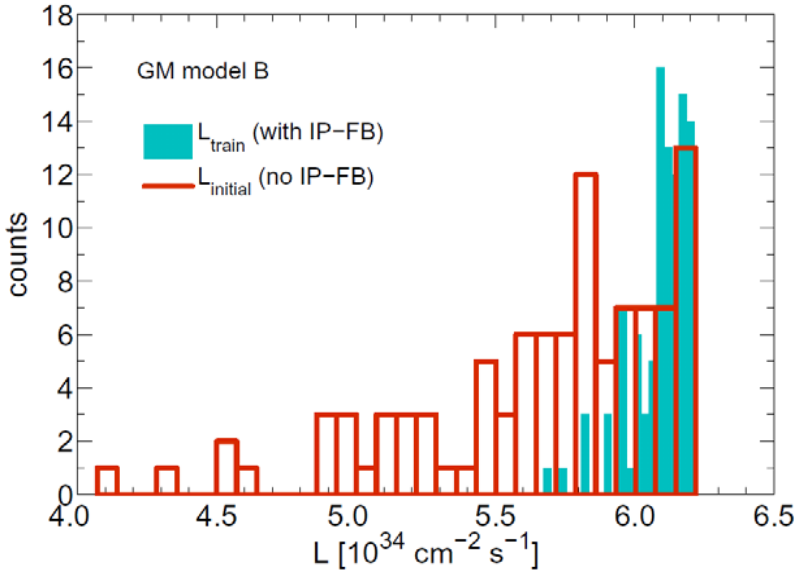
Simulation time structure:
Example applying a single random seed of GM C



CLIC luminosity result with IP FB

For quiet sites:





The generated IP-jitter is relatively small after 0.02 s of GM

Model A:

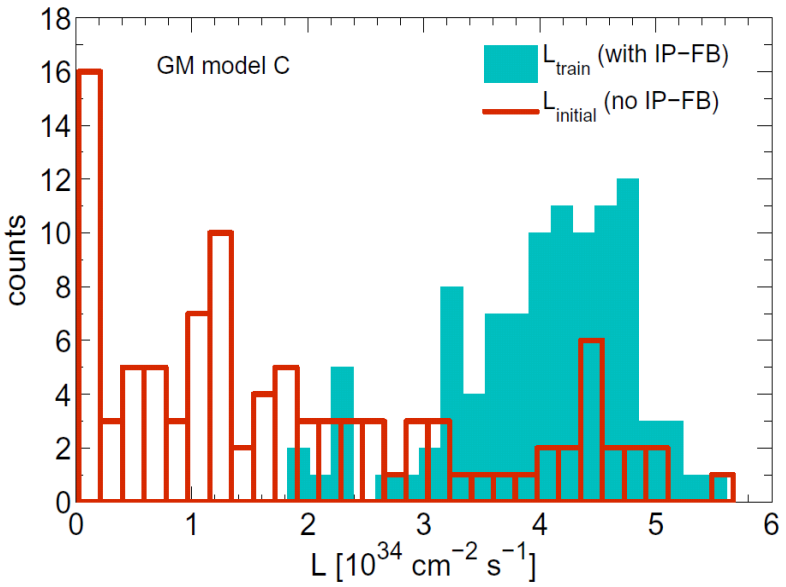
- Without any correction: mean $\Box L/L_0\Box_{train}$=99.88%
- With IP-FB: mean $\Box L/L_0\Box_{train}$=99.97%
  std reduced by a factor 2

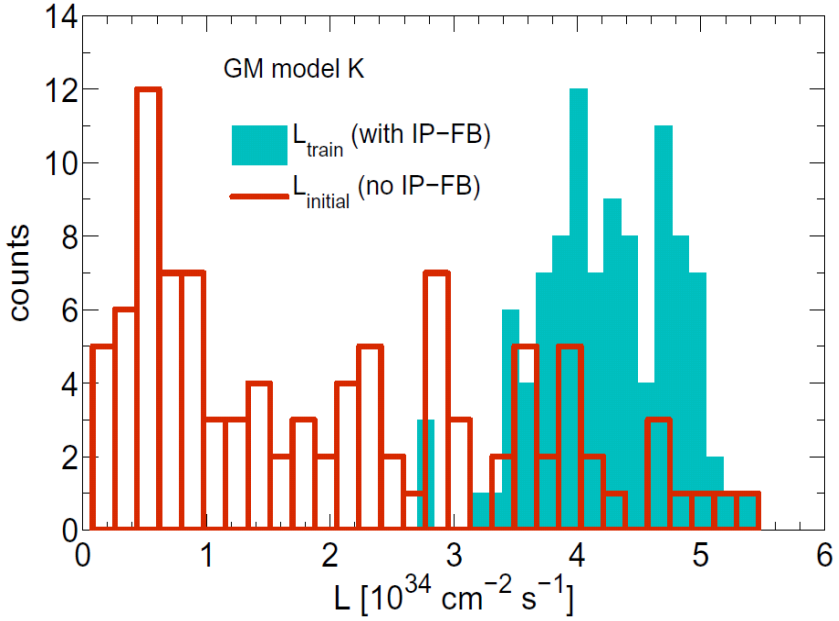
Model B:

- Without any correction: mean $\Box L/L_0\Box_{train}$=91.1%
- With IP-FB: mean $\Box L/L_0\Box_{train}$=97.86%
  std reduced by a factor 4

CLIC luminosity result with IP FB

For noisy sites:





In these cases significant luminosity degradation

Model C:

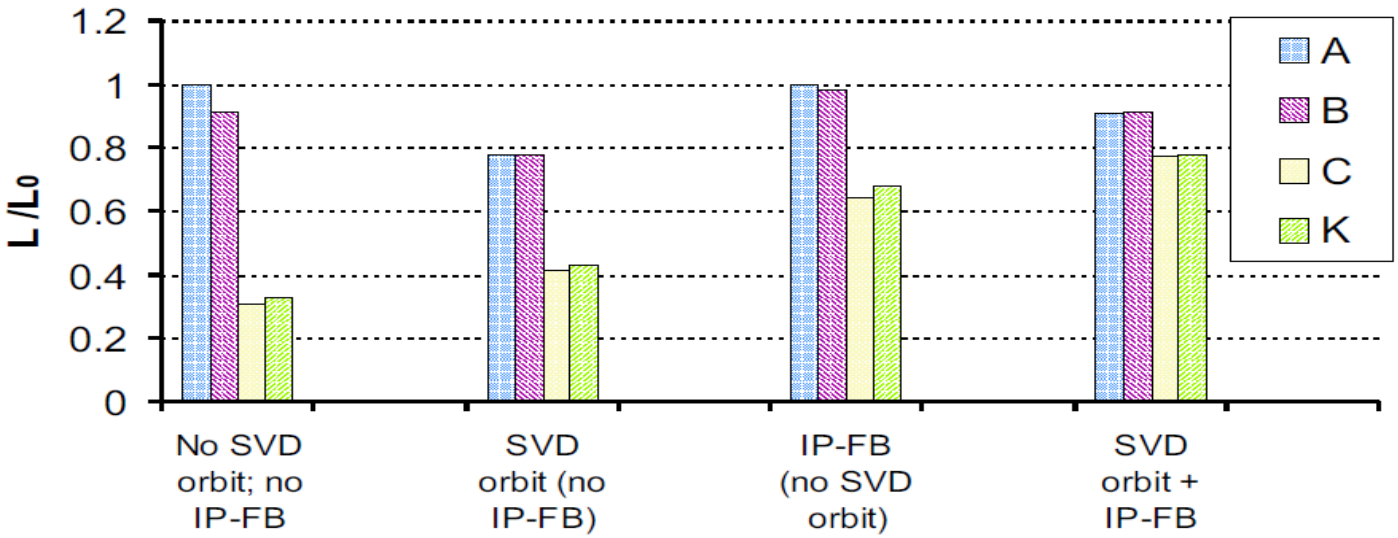
- Without any correction: mean $\Box L/L_0\Box_{train}$=30.52% & High standard deviation!
- With IP-FB: mean $\Box L/L_0\Box_{train}$=64.15% std reduced by a factor 2

Model K:

- Without any correction: mean $\Box L/L_0\Box_{train}$=32.53% & High standard deviation!
- With IP-FB: mean $\Box L/L_0\Box_{train}$=67.82% std reduced by a factor 3

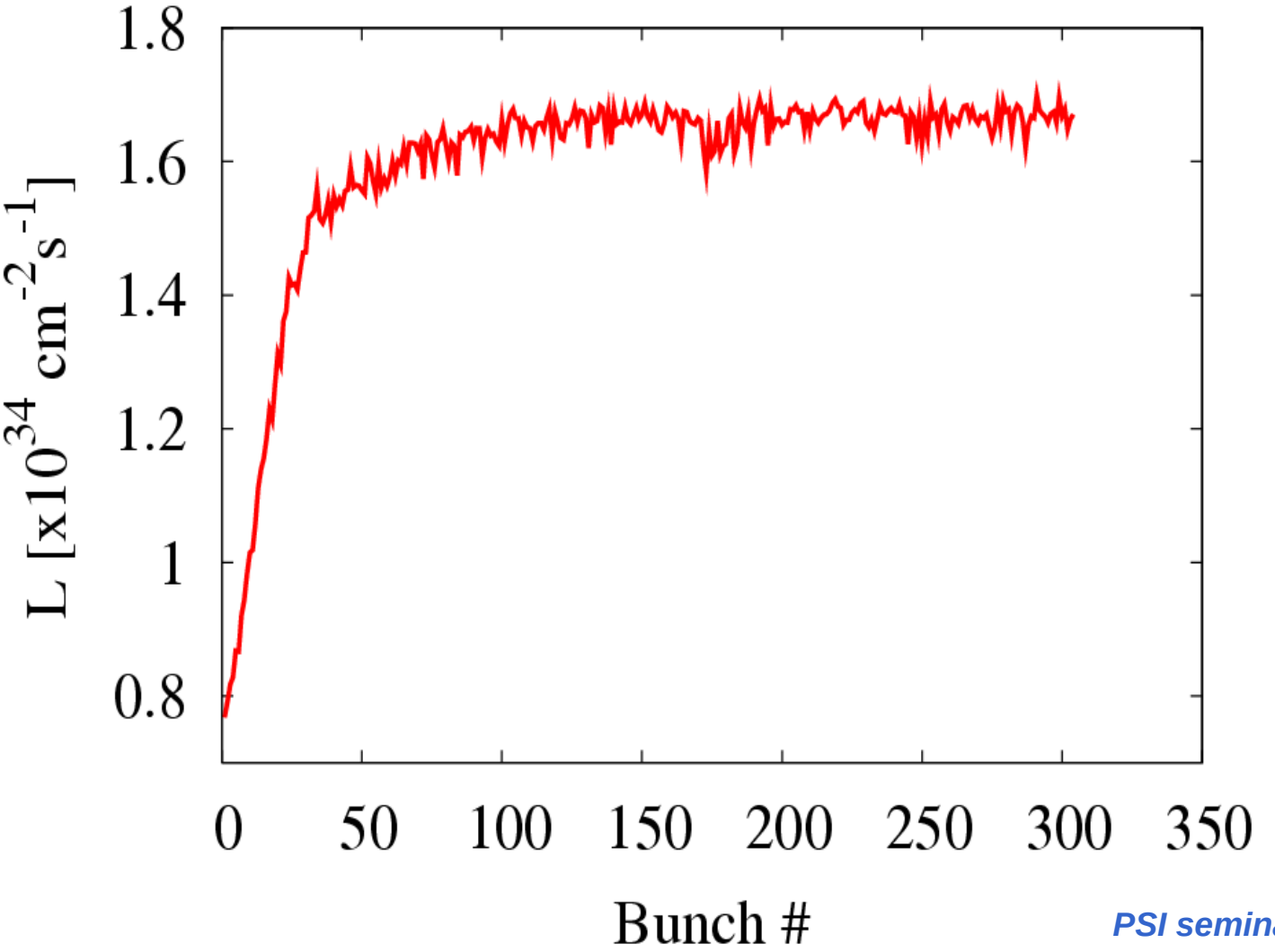
Luminosity results summary

Simulate effect of IP feedback and slow orbit FB in BDS



SVD orbit correction
BPM resolution ~100 nm

ILC IP intra-train FB performance



Other CLIC possibilities

Fast amplifier prototype for drive beam phase instability feed-forward system:

10 deg capture range → 0.2 deg phase stability

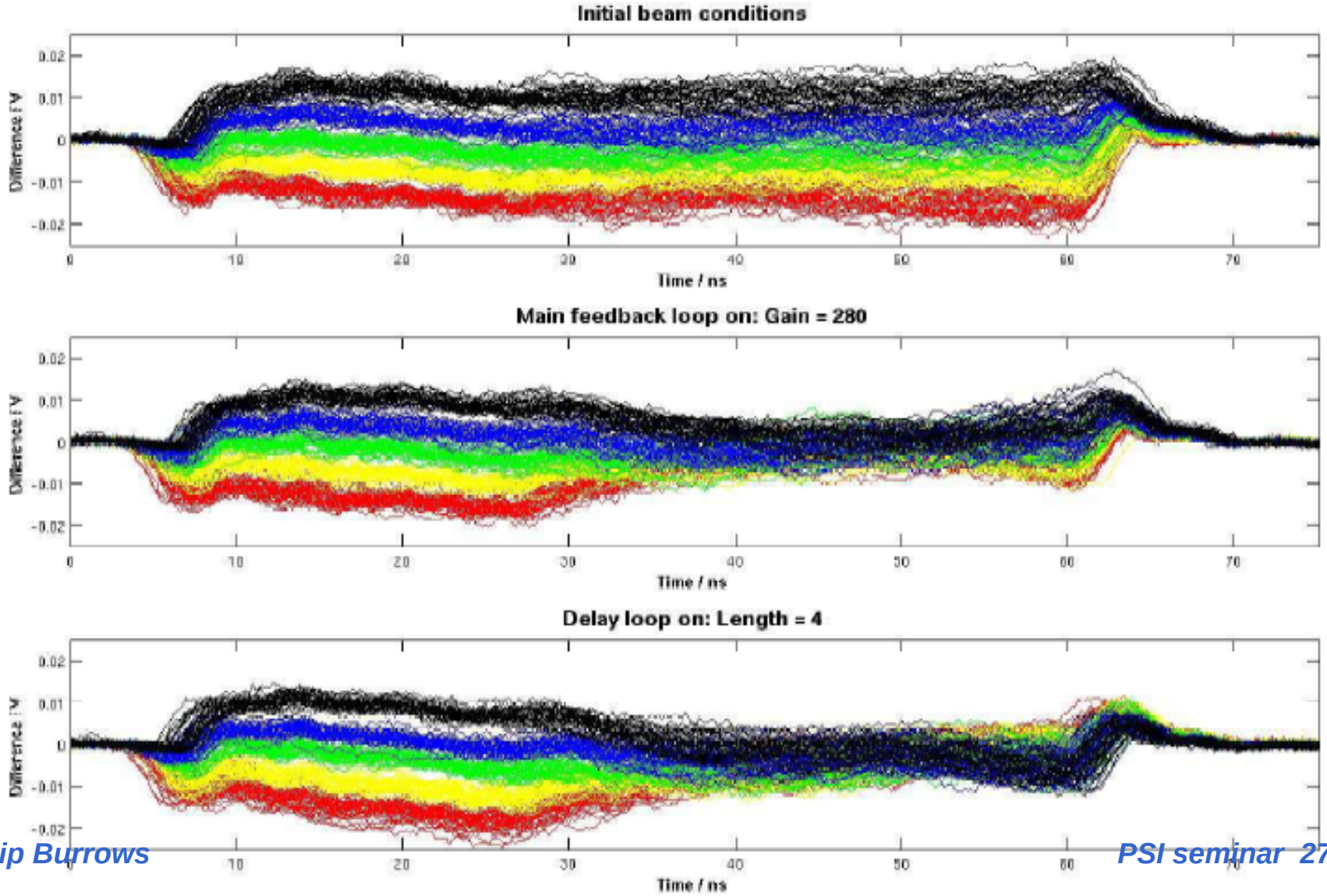
+-375urad max. beam deflection

very serious thought and R&D needed

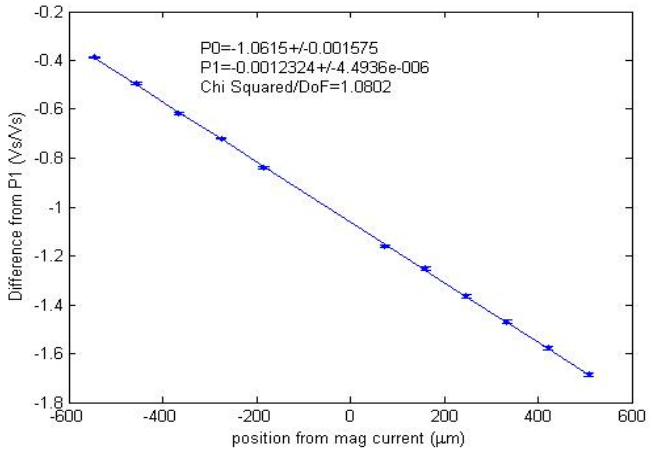
prototyping and tests at CTF3?

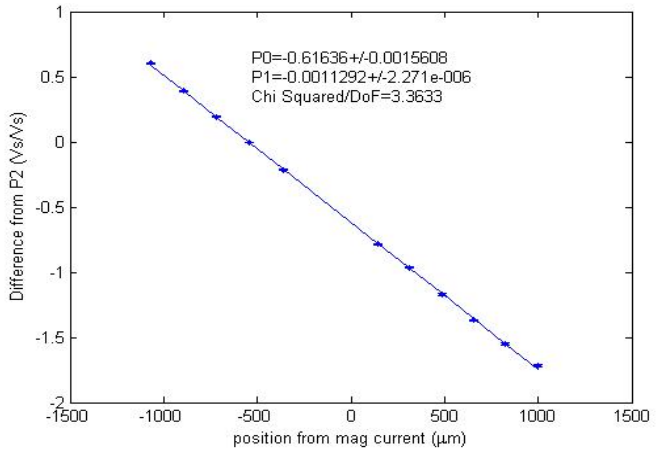
FONT3: Results (June 2005)

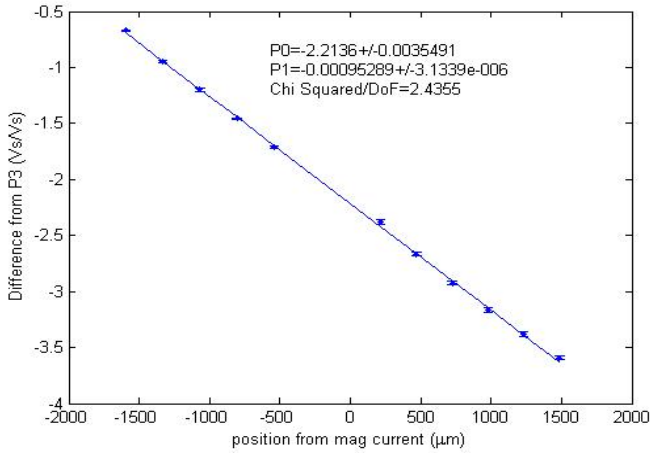
40 pulses per position setting



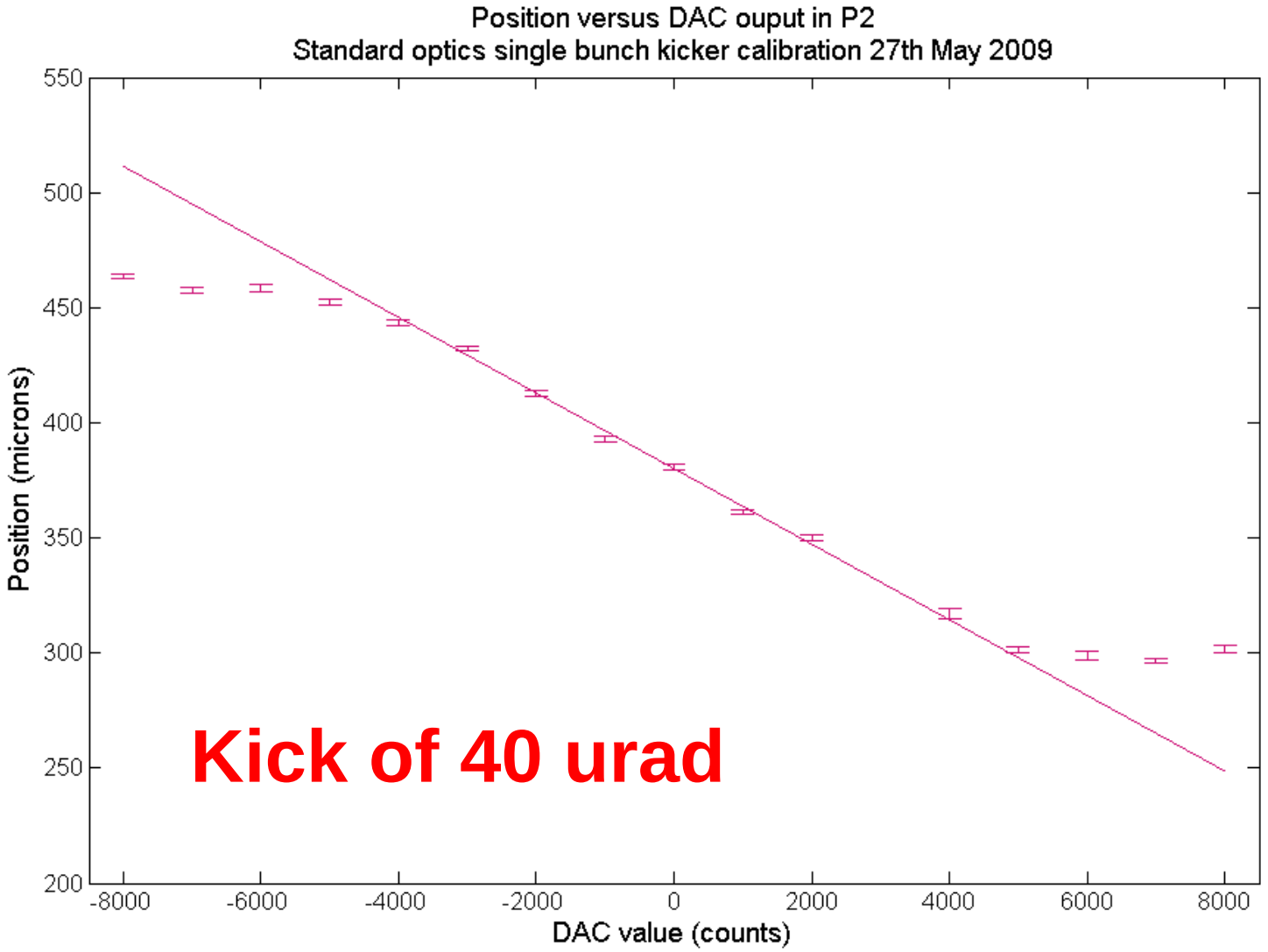
Example: BPM calibrations



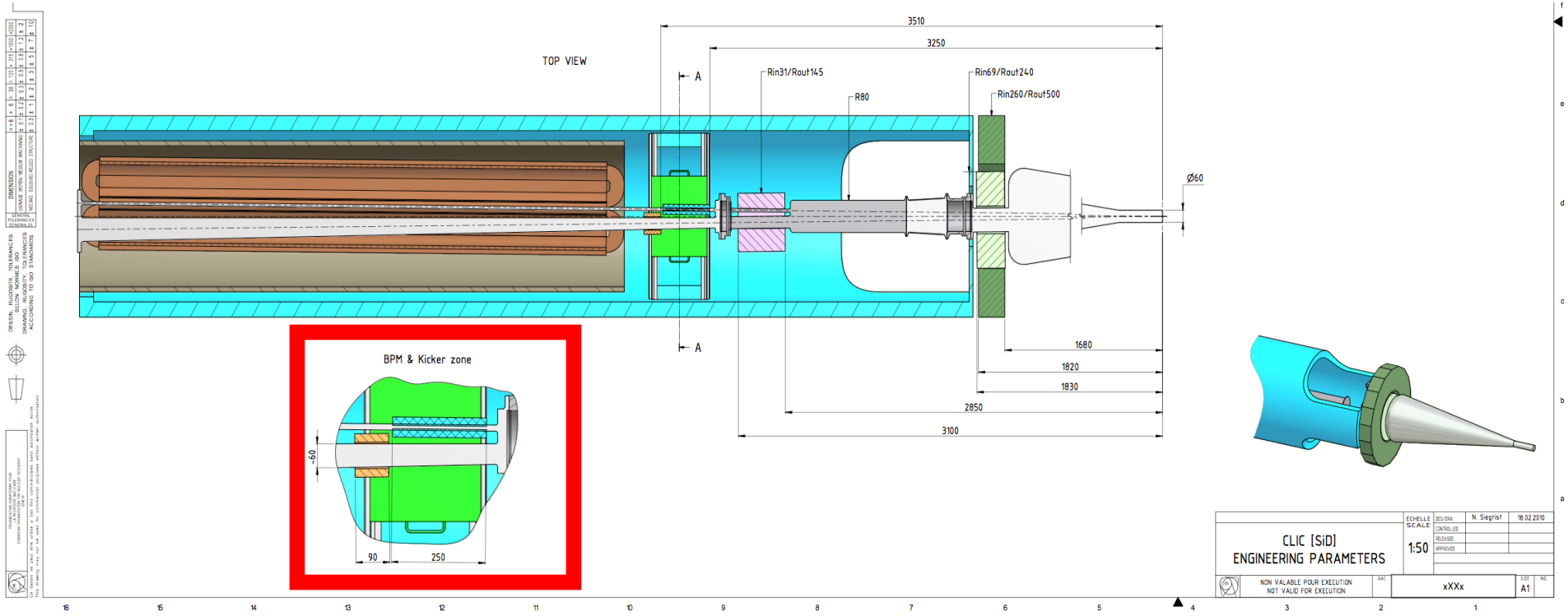




Example: kicker calibration

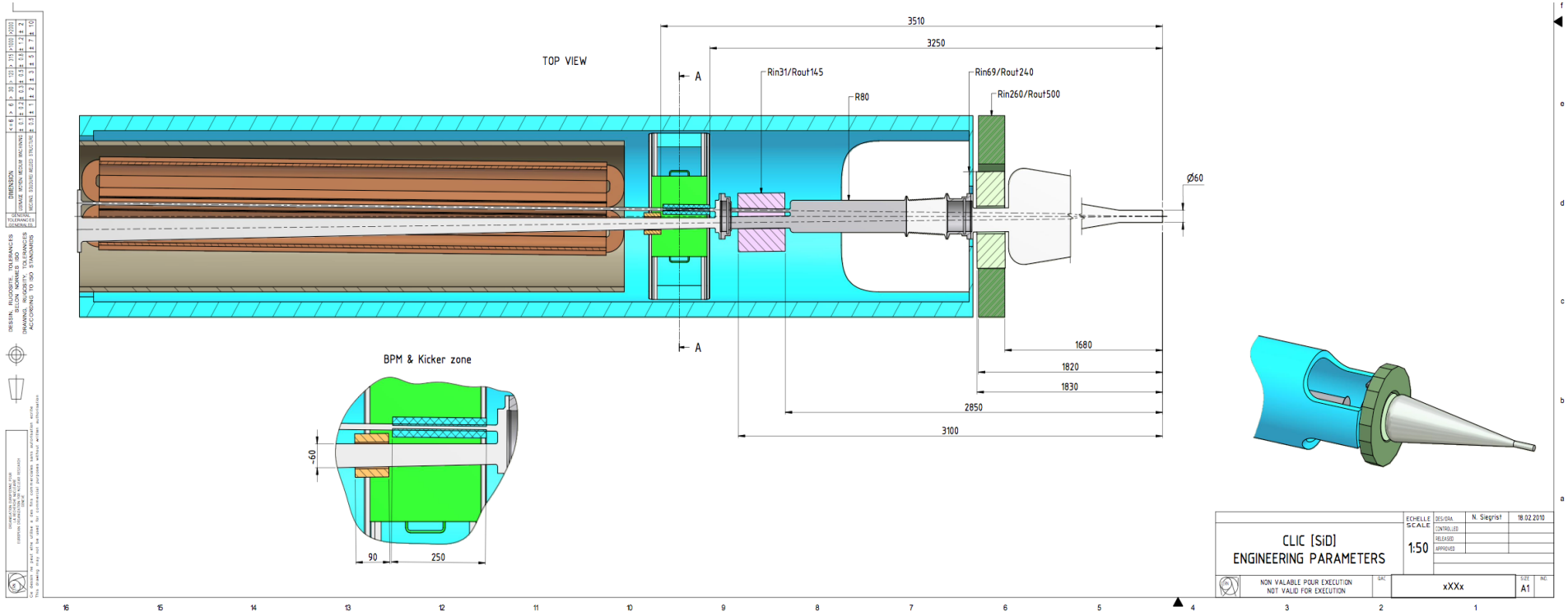


CLIC: zoom-in to QD0



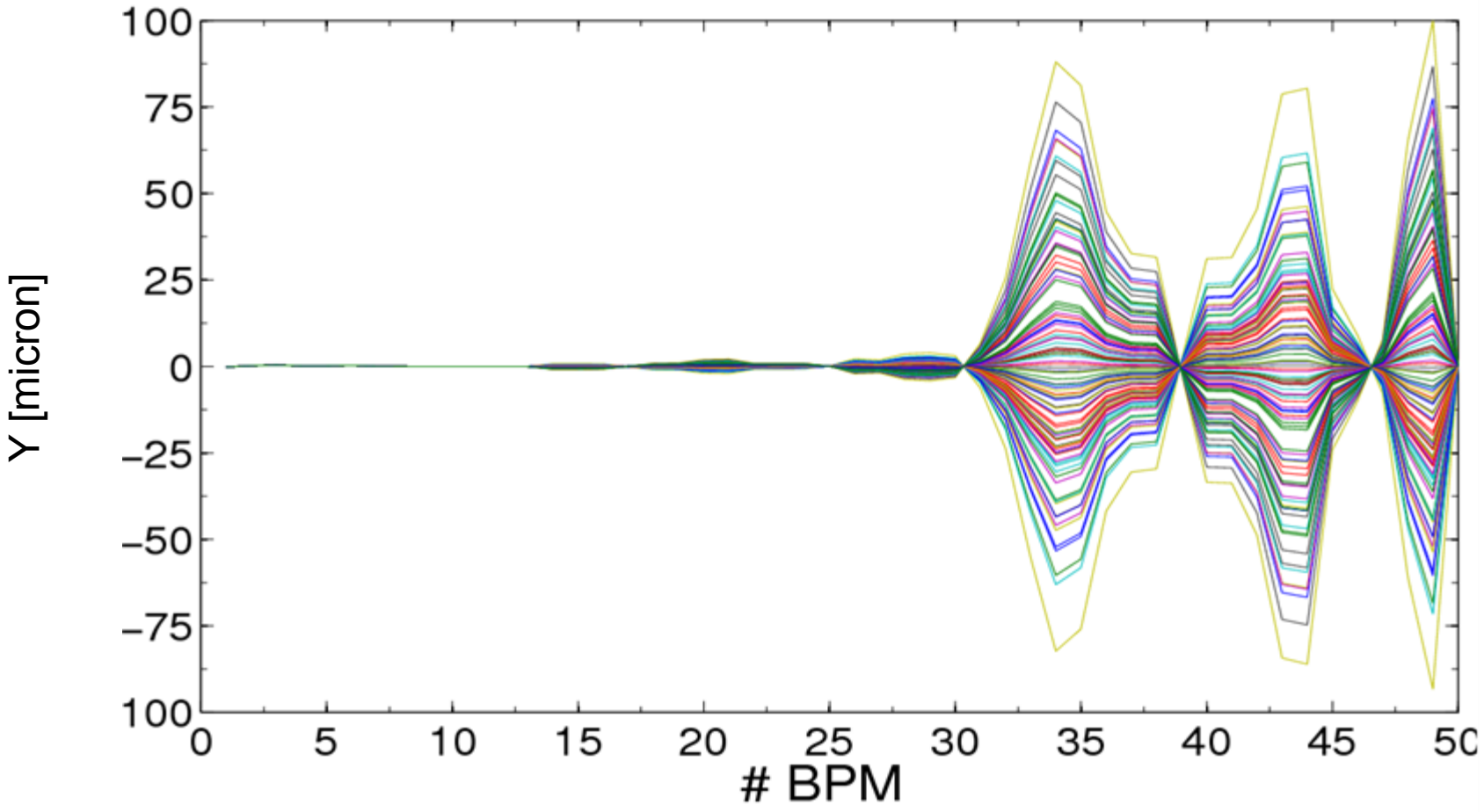
Herve 22/2/10

CLIC: zoom-in to QD0



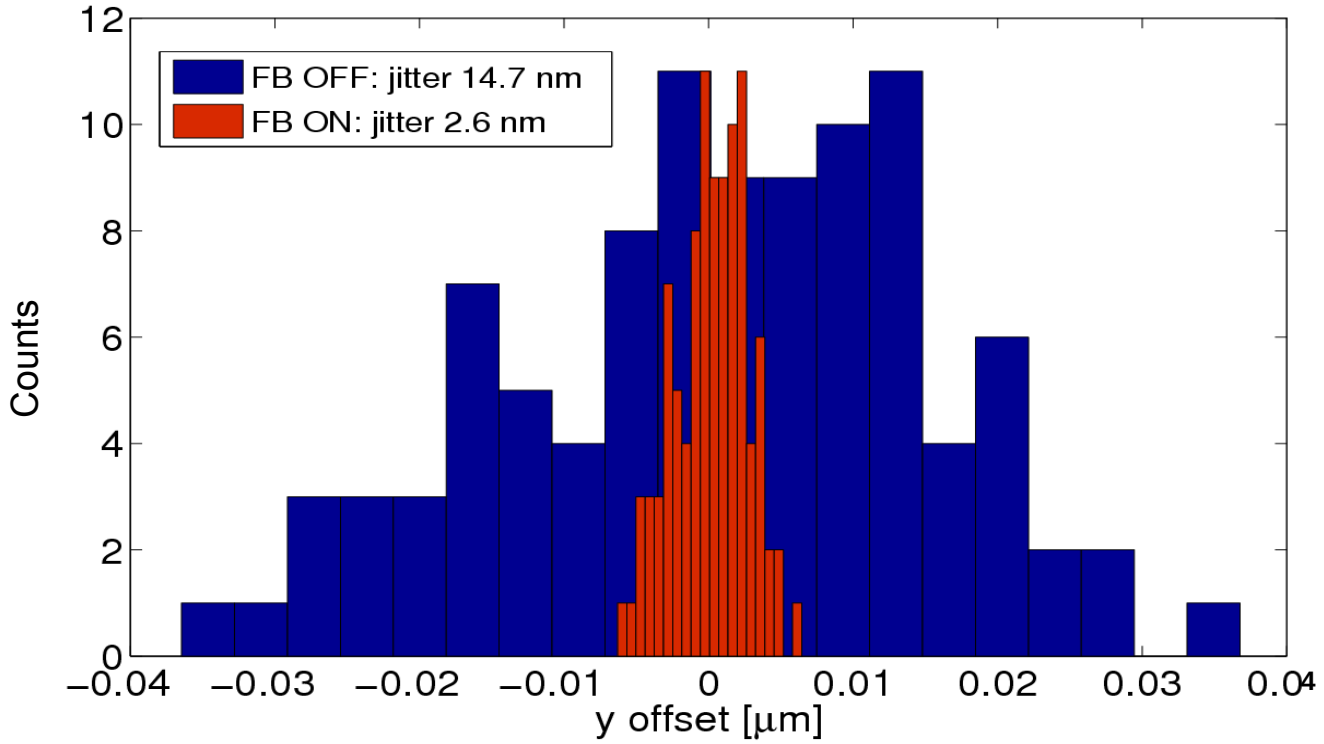
Herve 22/2/10

0.4 micron jitter propagation from P2



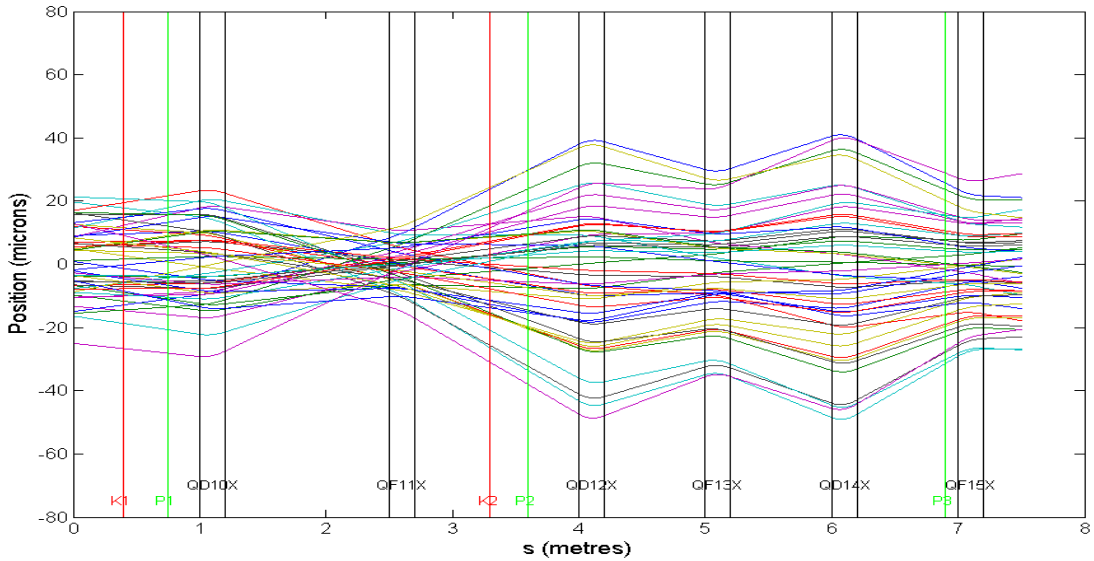
Jitter comparison at IP

Assuming perfect lattice, no further imperfections (!)



FB simulation: P2-K1+P3-K2 coupled

Bunch 1



Bunch 2