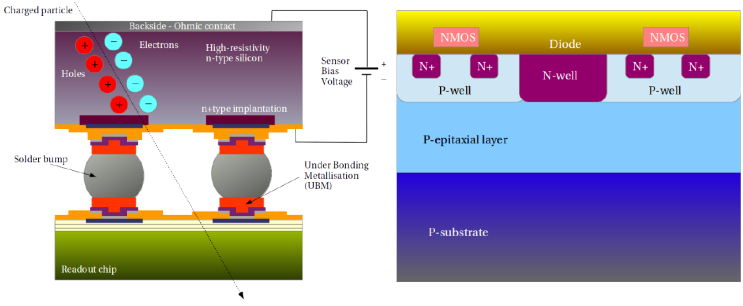
MoTiC: Prototype of a Monolithic Particle Tracking Detector with Timing

Stephan Burkhalter

Motivation

- The PSI High Energy Physics group in collaboration with ETHZ has a generic R&D program for DMAPS since 2019
- Several technologies are being evaluated
- Goal: radiation hard detectors featuring timing
- Aiming for
  - Spatial resolution of O(10 µm)
  - Sub-nanosecond timing resolution

Depleted Monolithic Active Pixel Sensors (DMAPS)



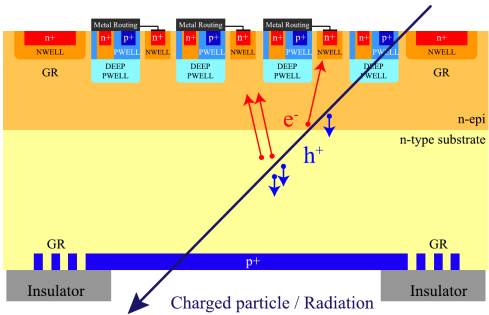
- Left: Hybrid pixel detector (such as the current pixel detector at CMS): More complex, but each piece of silicon can be optimized for its purpose.
- Right: DMAPS: All components are processed on the same wafer.

MoTiC: Monolithic Timing Chip

- Manufactured in a modified 110 nm CMOS process
- Pixel pitch: 50 x 50 μm^2
- 80 columns by 64 rows (5120 pixels)
- Full frame readout
- In-pixel discriminators and TDC shared by 4 pixels
- 7 pixel flavours with different preamplifier designs
- Sister chip with varying sensor geometries and test structures (MoTiC B)

Process Overview: Modified LFoundry 110 nm Process

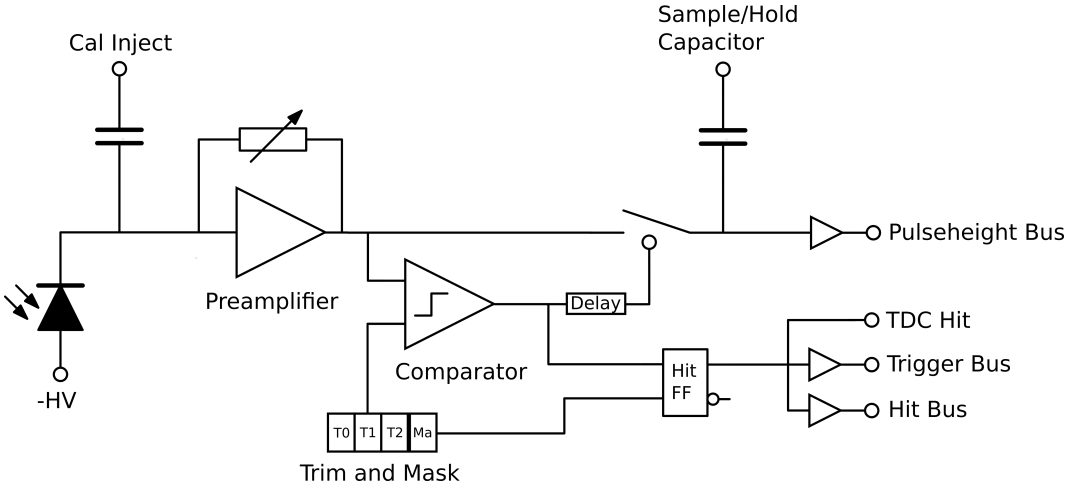
N-type substrate wafers



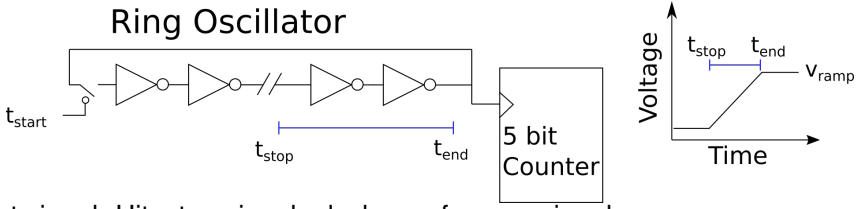
- All sensing structures designed by ARCADIA
- Small electrodes with small capacitance
- The wafers are backside processed to have guard rings and backside metal contact.
- Depletion from the backside
- Active thicknesses of 50, 100, 200 µm

The development of the process modification and sensor nodes has been performed in the framework of the INFN CSN5 Call ARCADIA. Image Source: [1]

Pixel Schematic

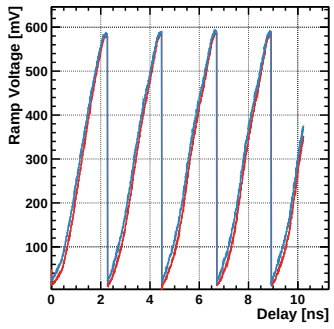


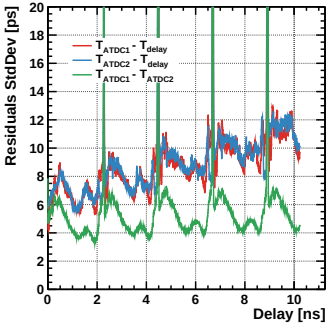
Time to Digital Converter (TDC)



- Start signal: Hit, stop signal: clock or reference signal
- Ring oscillator, adjustable frequency of O(500 MHz to 1 GHz)
- Coarse resolution (O(ns)): number of revolutions counted
- Sub-nanosecond resolution: charging a capacitor to measure time to finish last revolution (analog readout)

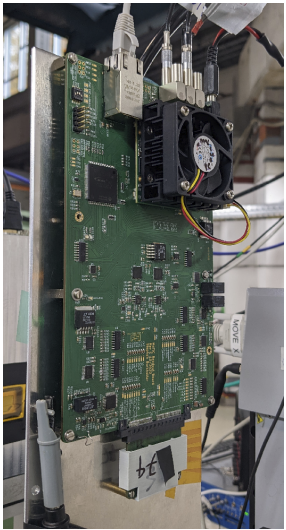
Time to Digital Converter (TDC)





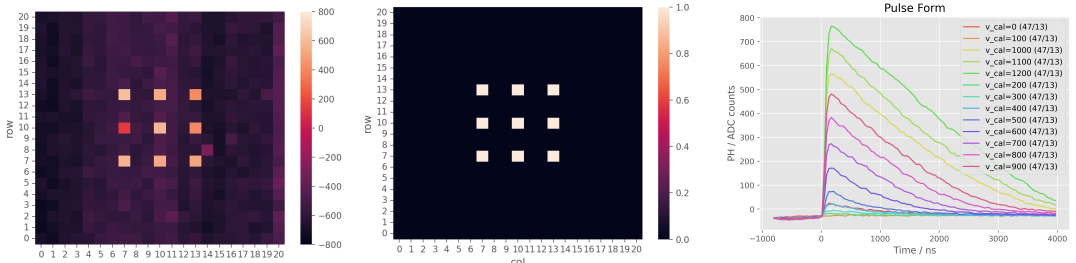
- Left: 2 standalone TDCs, analog response vs. external delay
- Right: residuals of TDCs
- O(10 ps) TDC resolution achieved
- Flat top removed in next submission

DAQ System



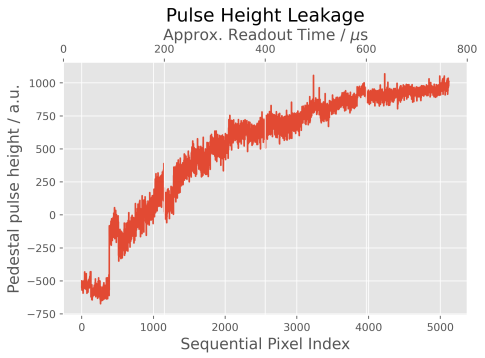
- Regulators for chip power supply
- Two high speed ADCs for pulse heights and TDC ramp
- Two FPGAs
  - Max10 for direct communication with the chip
  - Enclustra SoC (Cyclone V) for readout control
- 48 DAC/ADC channels
- Delay chip to test TDC
- Dedicated DAQ soft- and firmware with integration in EUDAQ2

Calibration Pulses



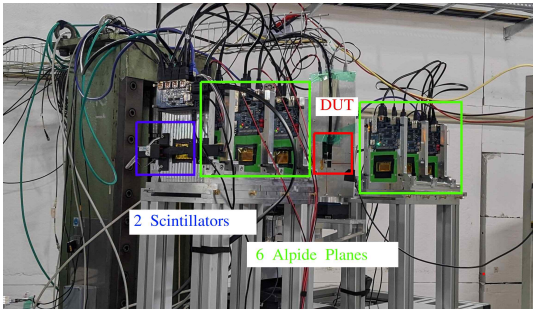
- Basic functionality verified in the lab
- Left and Middle: Inject calibration pulses in pattern resulting pulse height and hit map
- Right: Pulse forms of varying injection charges

Leakage of Sample & Hold Capacitor



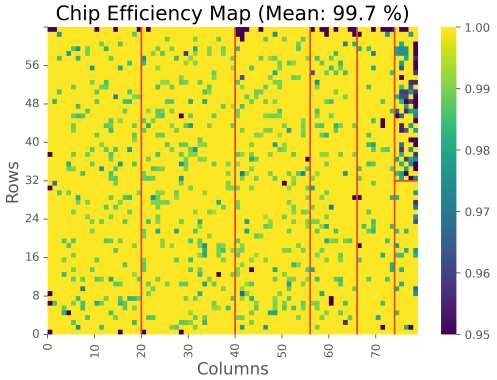
- Read out all pixels sequentially
- Pulse height pedestal as a function of pixel index
- Sample & Hold capacitor (MOSCap) very leaky
- All charge leaking away within $\sim$ 1 ms
- Steps due to variation in the end-of-column amplifiers
- This and other issues fixed in v2 tapeout in June 2022 (received a few weeks ago)

Test Beam at DESY



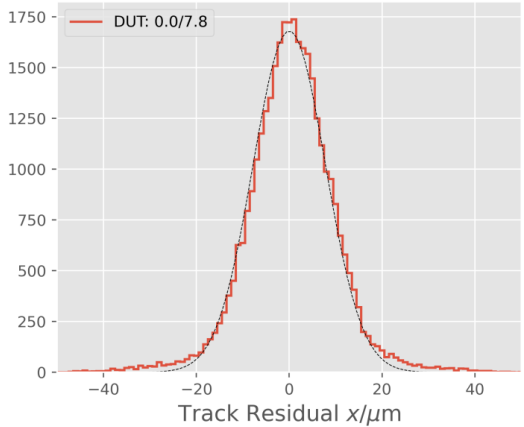
- Took place Nov 21 - Nov 28 2022
- 4-5 GeV/c electrons
- 6 Alpide planes
- $\sim$ 28 x 28 µm^2 pixels
- Tracking resolution $\lesssim$ 5 µm
- Coincidence of scintillators as trigger

Efficiency Map



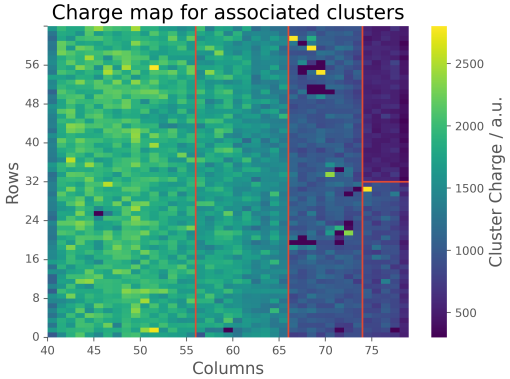
- Efficiency across full matrix.
- Red borders show different preamplifier designs.
- Top right flavour has a larger feedback capacitance leading to a lower gain.

Spatial Resolution at Vertical Incidence



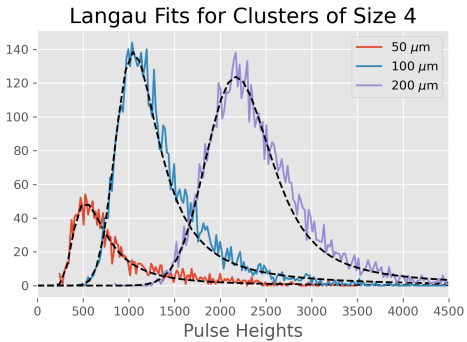
- Resolution: RMS of the distance to the reconstructed track.
- Better than binary resolution ($\sim$ 14.4 µm)
- This is due to significant charge sharing even at vertical incidence.
- Best resolution of 6.5 µm achieved at an incident angle of 10°.

Charge Map of Associated Clusters



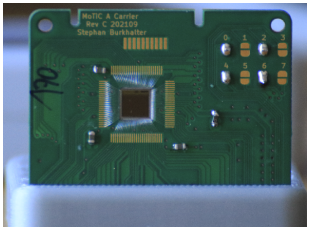
- Only right half of the chip is read out.
- Different preamplifier flavours are visible.
- Top right flavour has a larger feedback capacitance.

Charge Distribution of Associated Clusters



- Charge distribution of associated clusters.
- Samples of 50, 100, 200 µm active thickness.
- MPV of roughly 500, 1000, 2000 ADC counts.
- MPV proportional to active thickness.
- 1 ADC count $\approx 8\ e^-$.

Summary and Outlook



- A new prototype DMAPS chip has been designed in a modified LFoundry 110 nm process.
- High efficiency (99.7 %) and good spatial resolution (6.5-8 µm) measured in test beam
- More analysis on the different preamplifier flavours to be performed
- In-pixel TDC to be tested
- MoTiCv2 received end of April 2023. Leakage is fixed, but other new problems to be understood

References

[1] L. Pancheri et al., “Fully Depleted MAPS in 110-nm CMOS Process With 100-300 um Active Substrate,” *IEEE Transactions on Electron Devices*, vol. 67, no. 6, pp. 2393–2399, 2020.

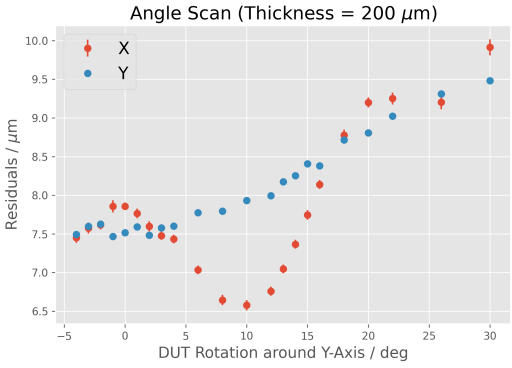
[2] L. Pancheri et al., “A 110 nm CMOS process for fully-depleted pixel sensors,” *Journal of Instrumentation*, vol. 14, pp. C06016–C06016, jun 2019.

[3] C. Neubüser et al., “Sensor design optimization of innovative low-power, large area fd-maps for hep and applied science,” *Frontiers in Physics*, vol. 9, 2021.

[4] R. Diener et al., “The DESY II test beam facility,” *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, vol. 922, pp. 265–286, 2019.

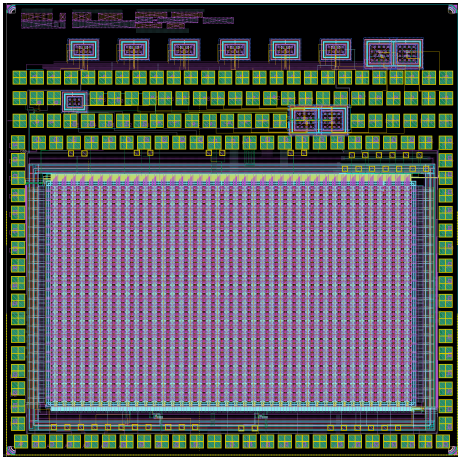
[5] D. Dannheim et al., “Corryvreckan: a modular 4d track reconstruction and analysis software for test beam data,” *Journal of Instrumentation*, vol. 16, p. P03008, mar 2021.

Spatial Resolution



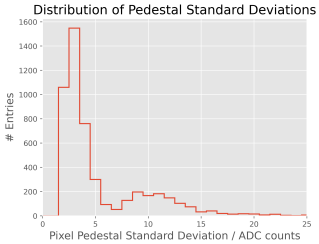
- Particles inducing charge in multiple pixels form clusters (charge sharing).
- Exact hit position is calculated by the center-of-gravity of the pulse heights.
- Resolution: RMS of the distance to the reconstructed track.
- Significantly better than binary resolution ($\sim$ 14.4 µm) even at vertical incidence.
- Optimal charge sharing angle for 200 µm at 10°.

MoTiC B: Sister Chip with Test Structures



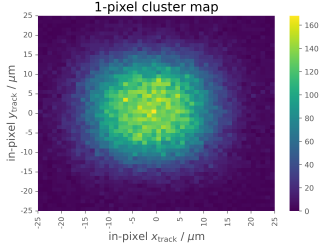
- 4 different sensor geometries designed by ARCADIA
- 1 AC coupled pixel
- Test structures for (edge) TCT measurements

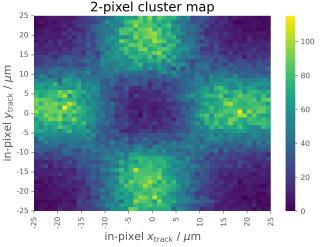
Readout Mode in Test Beam

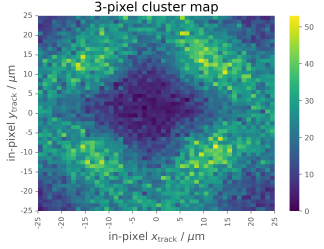


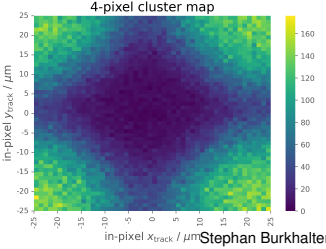
- An external trigger starts the readout sequence with a delay of $\sim$ 200 ns.
- The Sample & Hold circuit is set on hold to store pulse heights on the capacitors.
- All pixels are read out sequentially with shift registers.
- No buffers or digitization on chip, this is handled on the DAQ board.
- Discriminator and TDC not used at present.
- For hit discrimination an offline threshold of 8 times the noise (σ of the pedestal) is used.

N-pixel cluster Maps



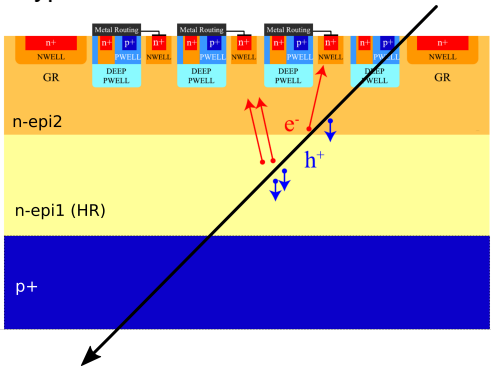






Process Overview: Modified LFoundry 110 nm process (2)

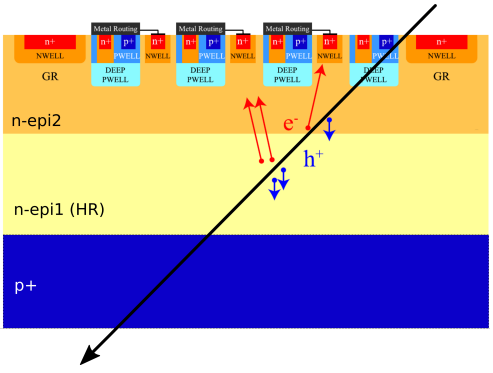
P-type substrate wafers



- All sensing structures designed by ARCADIA[1, 2, 3]
- P-substrate with 2 epitaxial n-layers
- Total thickness of epitaxial layers is 48 µm
- Physical wafer thickness is 300 µm
- Biased via conducting chip edge

The development of the process modification and sensor nodes has been performed in the framework of the INFN CSN5 Call ARCADIA. Image Source: [1]

Depleting the sensors

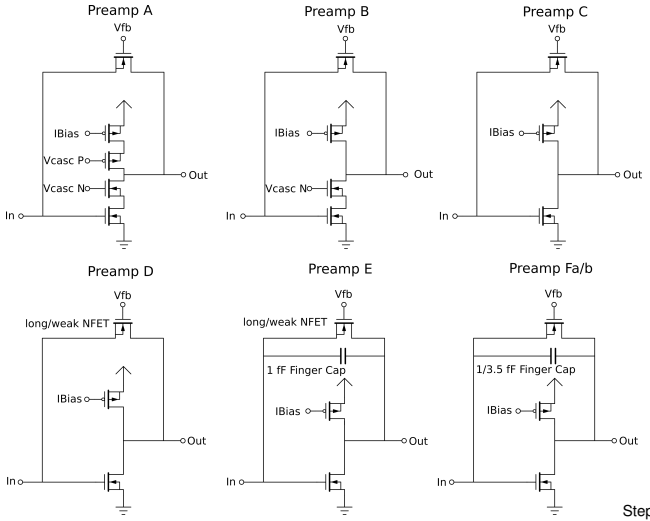


d / µm	Bias	V_D	I_L @ V_D / µA
200	Backside	∼ 50 V	∼ 20-30
100	Chip Edge	∼ 35 V	∼ 500-1000
48	Chip Edge	∼ 35 V	∼ 500-1000

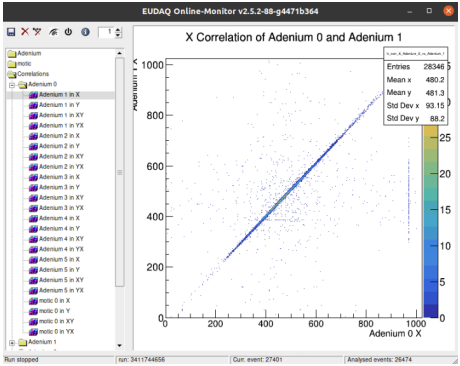
- High leakage caused by the conductive chip edge

- Full depletion is necessary to see signals.
- Leakage current flows into top-side guard ring and not into pixels.

Preamplifier Designs



Telescope at TB24



- Very clean telescope
- Integration time of O(10 µs)
- No need for timing reference plane
- 1 track per event
- Tracking resolution $\lesssim$ 5 µm

Preamplifier Calibration