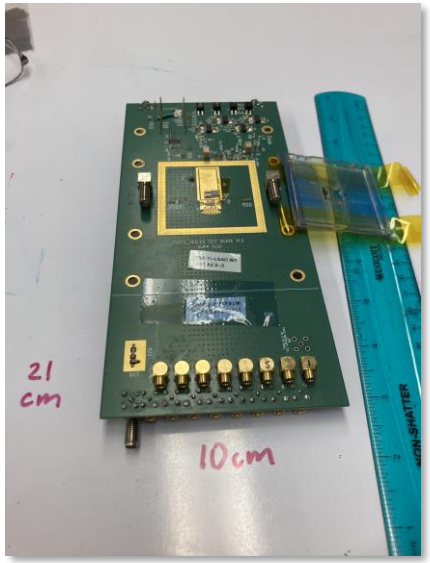
Readout Board and Mechanical Support for Atar

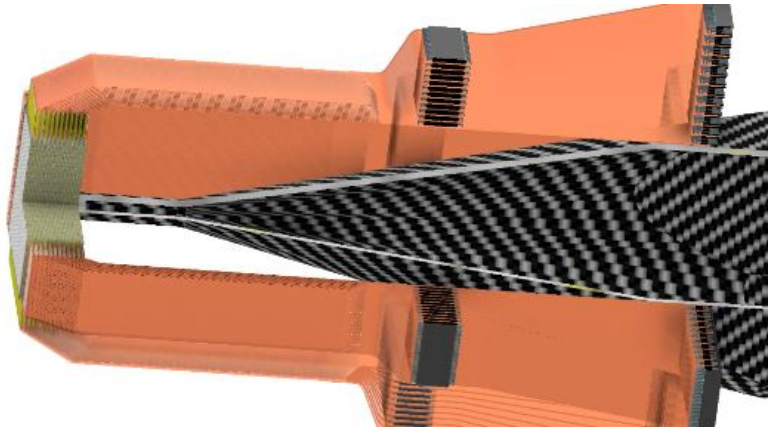
This is planning exercise to stimulate internal discussion

Peter Kammel, Tim van Wechel, David Peterson



16-channel

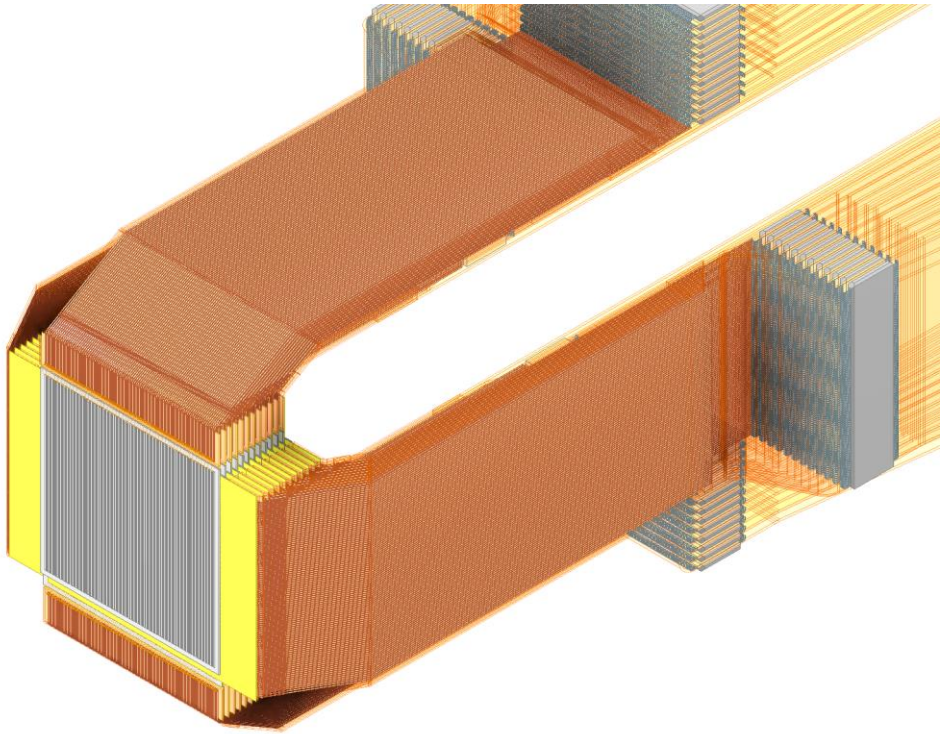
Strategy for development path



5000 channels

Sensor “packaging” options: LGAD modules

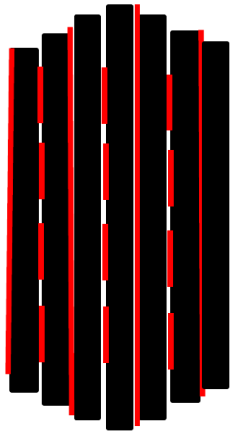
- Proposal
  - 20 x 20 x 5.76 mm
  - 48 sensor layers with 120 µm thickness
  - 12 flex cables to each side



- Doug: Pacman

- BNL

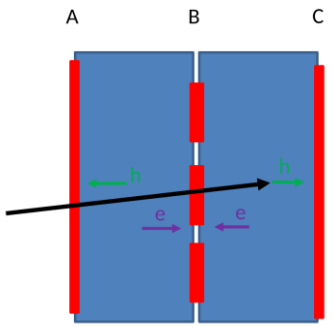
  Two adjacent layers shared the same readout strips
  (N --anode or P -- cathode)
  - 48 layers □ 49 x 100 channels (100 channels more than default)
  - 2-sided readout for each layer



Bulk (120 um)
Readout strip (200 um pitch, 100 width)

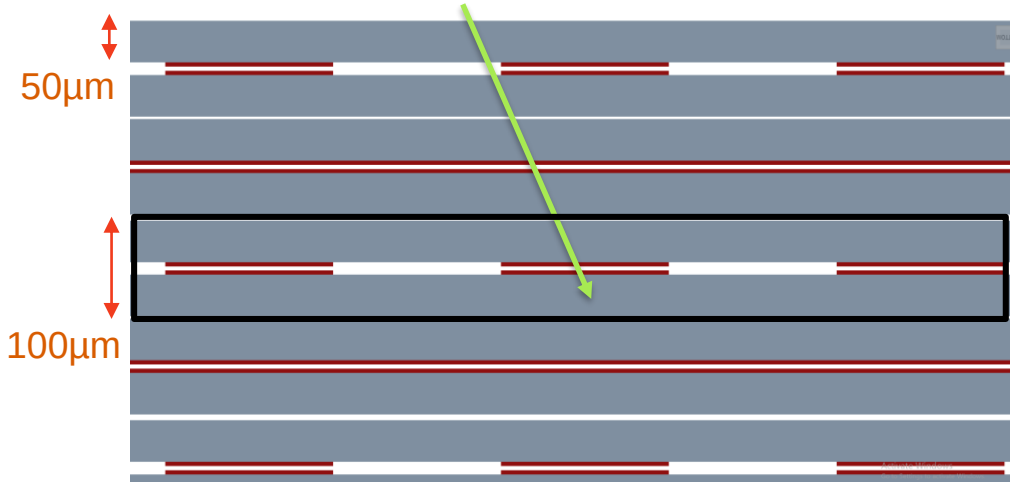
Layers are gradually increased/decreased, so that we can readout from the sides

Xin



Sensor “packaging” options impact design

- Peter



50 µm sensors connected on strip, HV plane

Smaller pi/mu ΔE seen by each gain layer

- Simone: combine several sensors to module with TSV

- Double LGAD, F. Carnesecchi et al.

reported. This is currently just a proof of concept, but the natural next step would be a better integration of such a concept either in the board containing the electronics or in the detector itself (in a truly d-LGAD or e.g. using Through-Silicon Via, TSV, technique).
In the proposed scheme, given by the sum of two LGADs each with a certain

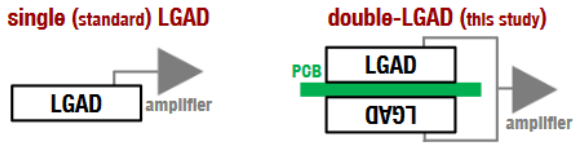
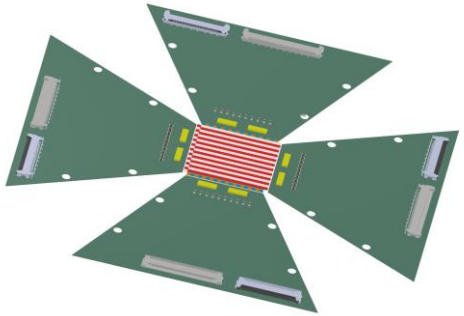


Fig. 1 Schematic of the single (standard) and double LGAD concept

Strategy



UCSC board and FAST2 chip

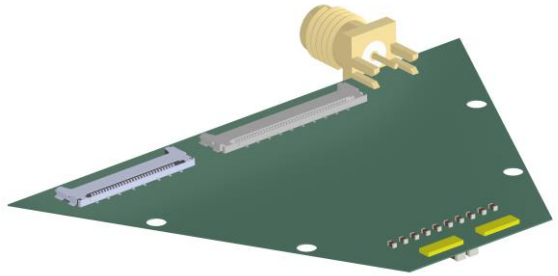
pFEB with minimal board spacing. Few mm gaps between pFEBs and sensor modules.

FEB0, Rigid-flex board with minimal thickness retracked behind ATAR.

Start | Step1 | Step2 | Step3 | Step4

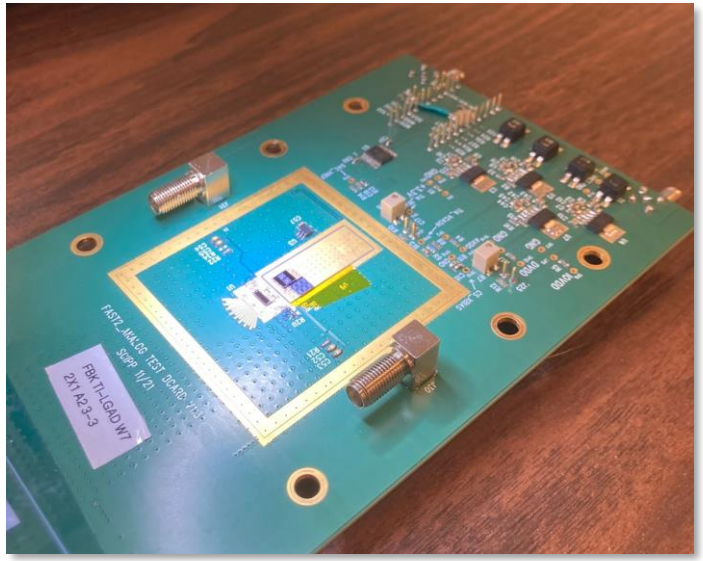
Flat proto frontend board pFEB, UW

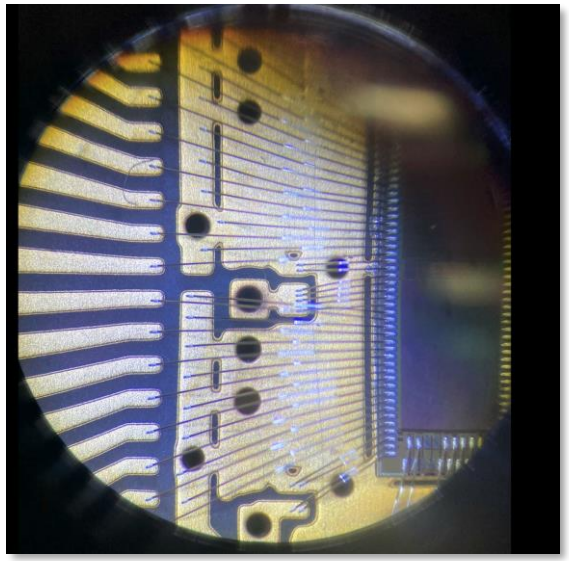
pFEB with flex between sensor and amplifier. No gaps.

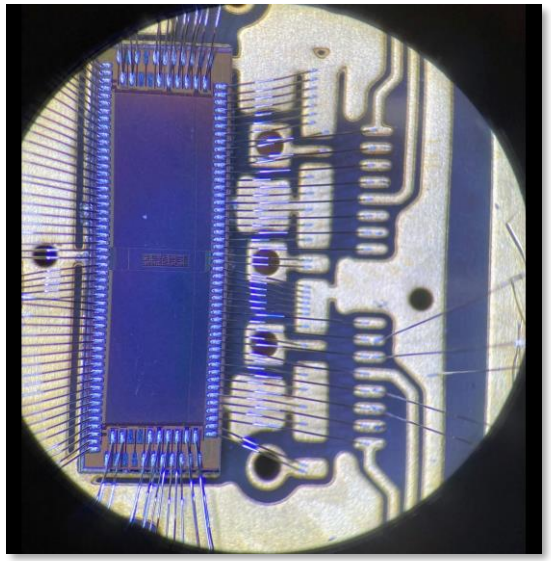


Start: UCSC board and FAST2/3

- Hardware

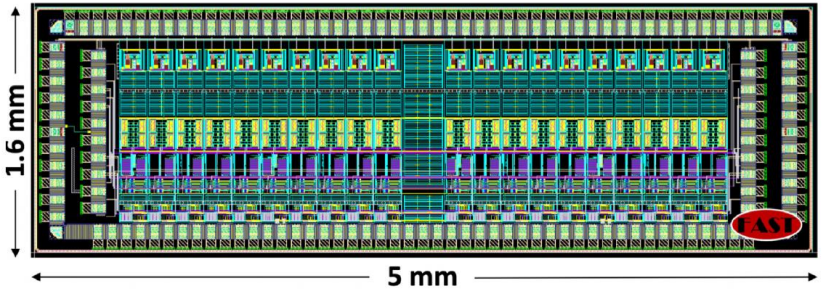






- Specs (Tim's talk)
  - Dynamic range limited FAST2/FAST3
  - Other ASICs in future
    - Anadyne
    - Nalu

ASIC Designers: J. Olave, F. Fausti



Design goal:
30 ps time resolution FAST+UFSD with MPV (8fC)

Channels number	~~20~~ 16
FAST flavors	Regular, EVO1, EVO2
Operation Voltage	1.2 V
Size	1.6 × 5 mm^2
Sensor Cap	2-6 pF
$\overline{SNR}$	60
RMS Noise	~ 0.7 mV
Power consumption	4mV
Time Walk correction	ToA, Tot
MPV input signal	8fC
Nominal input dynamic range	1 fC - 60 fC

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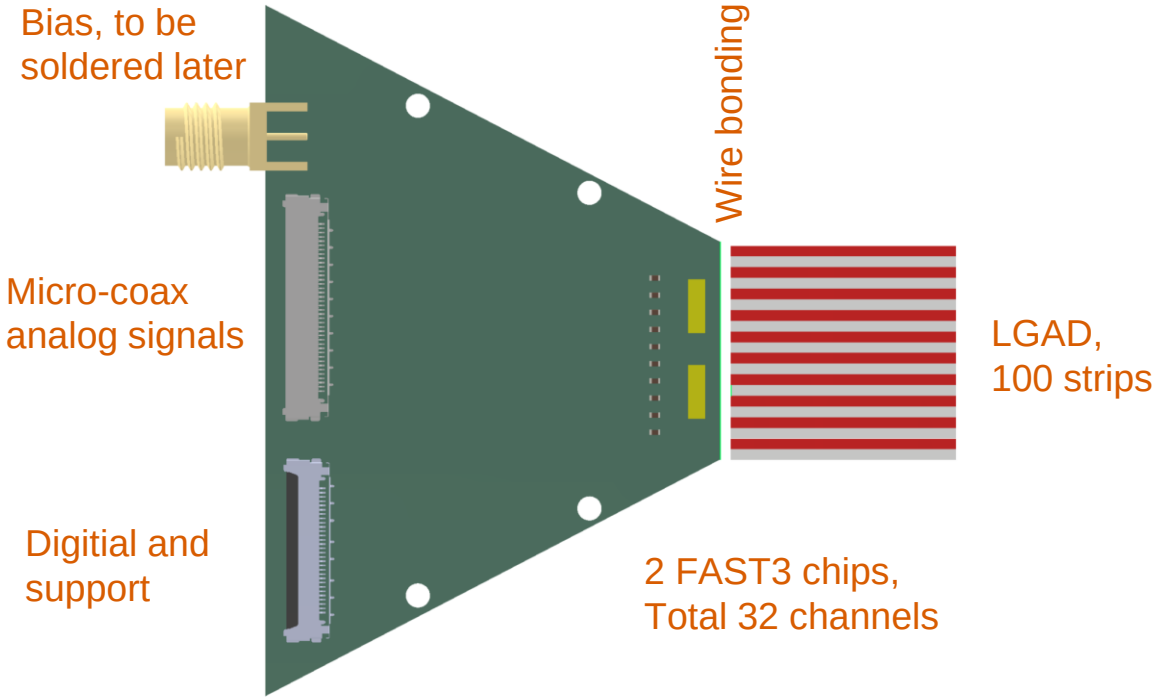
Via Pietro Giuria 1, Turin, Italy

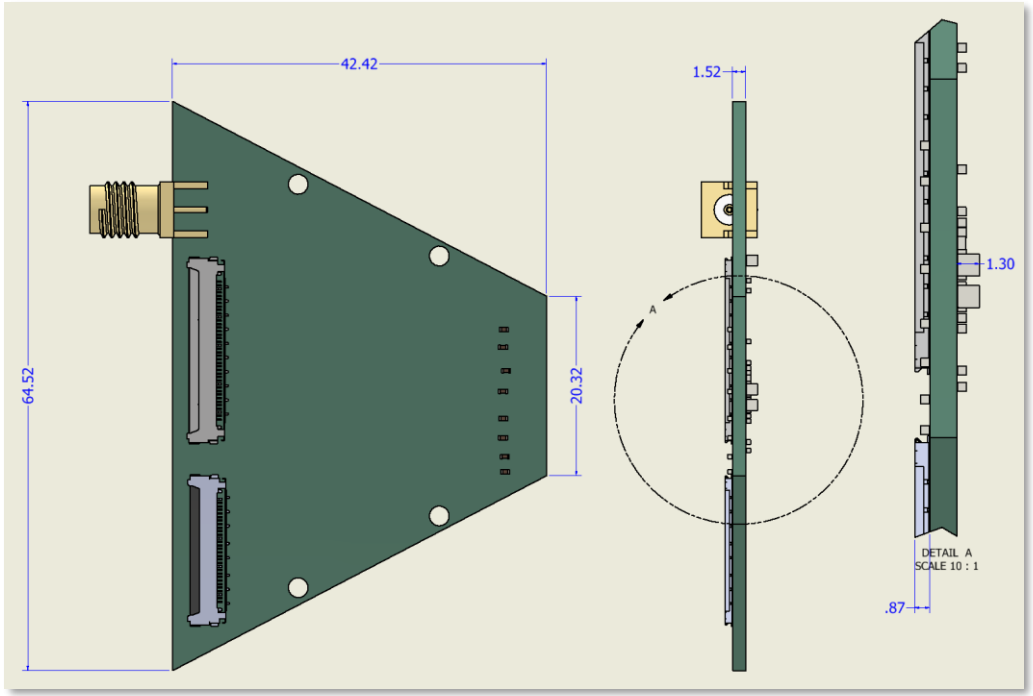
Step1: Flat pFEB, Quadrant

- Layout



- Geometry

Board height 1.5mm



Micro coax connector 1 mm

Status

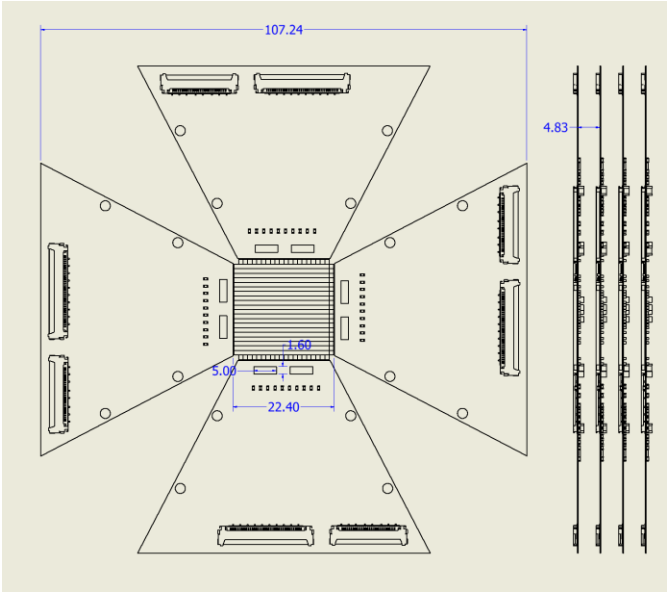
Design done

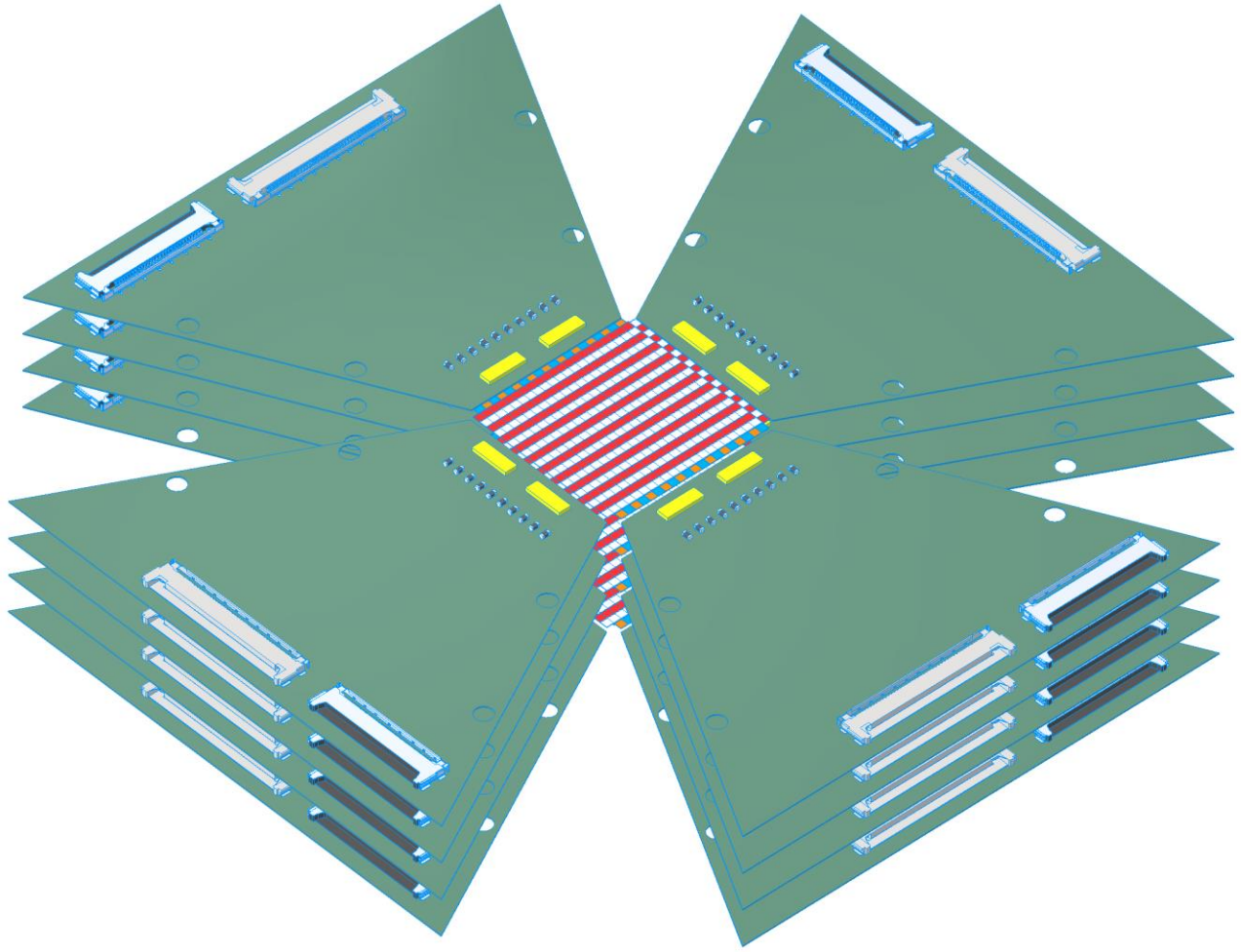
Routing in progress, review this week

Step2: Complete Flat pFEB

4 boards= 1/3 ATAR, 1/6 electronics

- Goal of pFEB:
  - 4 sensors,
  - 32 channels/sensor, 128 total
    (need LGAD,FAST3 production funding)
  - Full particle transmission
  - Mechanics
  - Test run with pi/mu in 2026
- Not a tight stack
  - mm gaps between 4 sensor modules



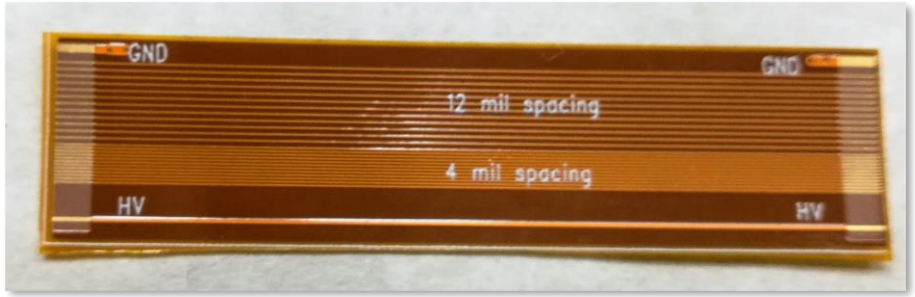


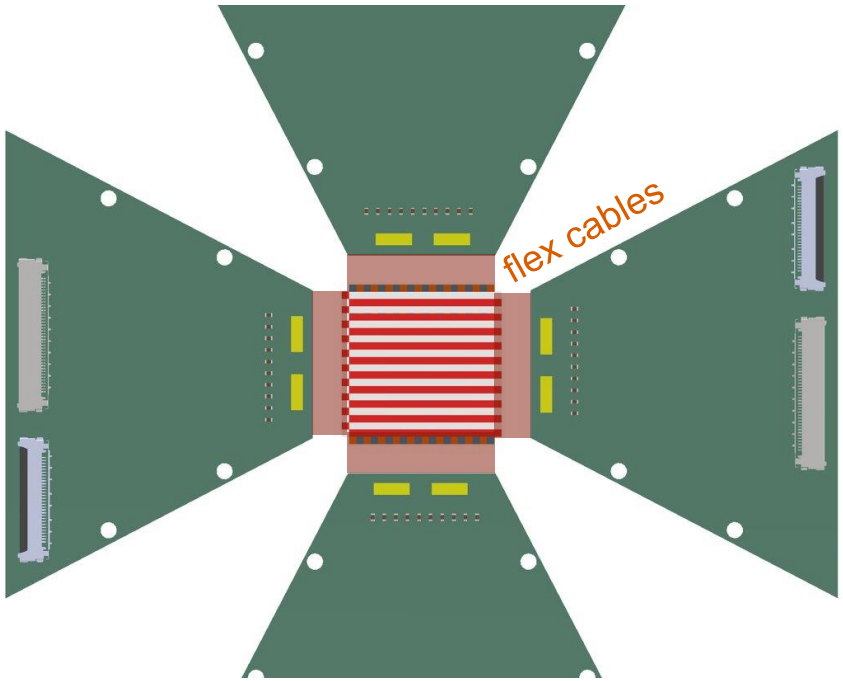
FEB stack will be mounted on mother board

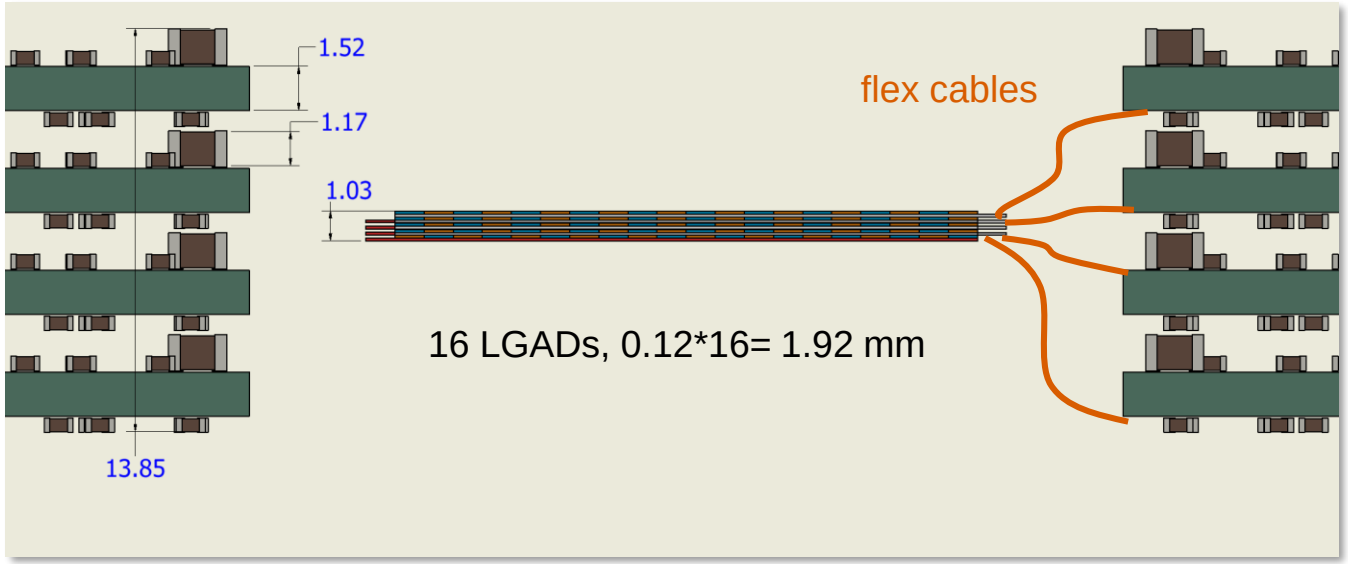
Step3: pFEB with flex and tight sensor stack

- Need to design working flex cables LGAD – FAST chip
  (or FAST close to LGAD?)

- Increase board opening and connect to tight stack



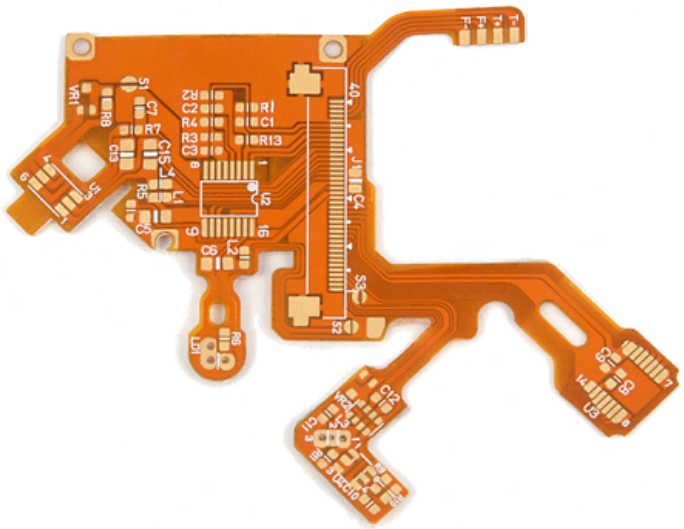




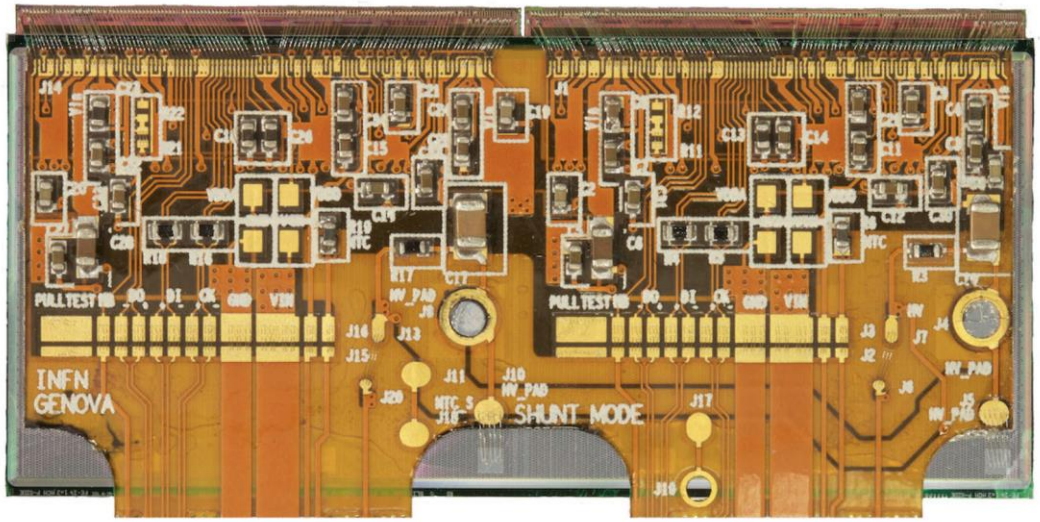
Step4: Rigid-to-flex board with minimal thickness

- Tilt boards relative to LGAD stack
  - Rigid-to-flex construction
  - 4-8 board modules with TSV big advantage
    - wire bonds in planes separated by 0.5-1 mm
    - Bias on same plane for all LGADs in module
    - All modules identical wire bonding and cabling
  - Mounting structure which supports flex cables

1 LGAD and flex per FEB.0 quadrant

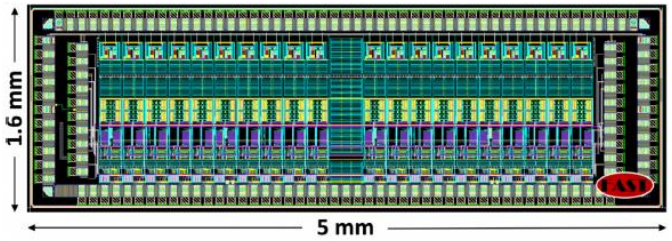


ATLAS



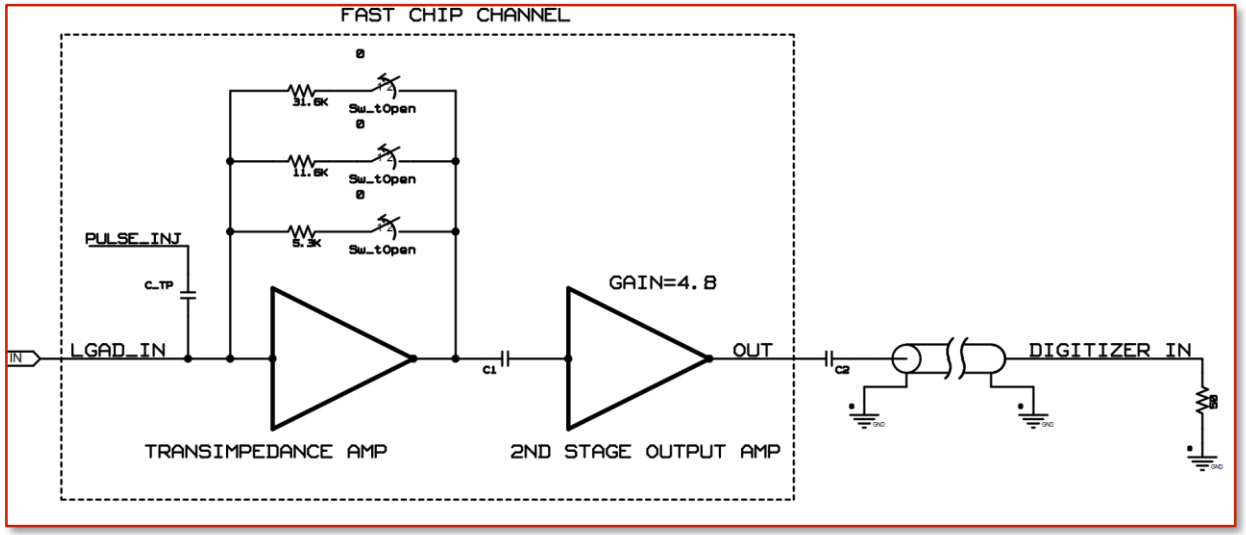
Front-end Amplifiers for Silicon detectors in Timing

ASIC Designers: J. Olave, F. Fausti



Each chip
- two groups of 8 channels, 16 channels total

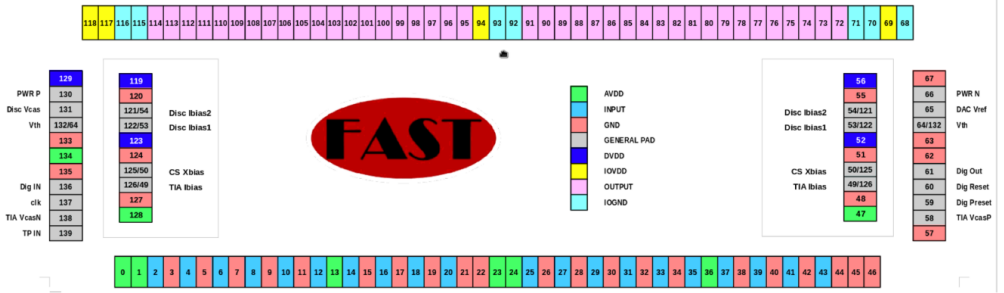
Each channel has two gain stages
- variable gain transimpedance amplifier (TIA)
- second stage output amplifier with ac coupling between stages and gain ~4.8.



Each transimpedance amplifier:
- three software selectable feedback resistors, 5.3, 11.6 (nominal), 31.6 kΩ.
- Nominal gain
  - TIA stage is11.6 kV/A
  - at the output is ~ 55 kV/A.
  - The bandwidth at the nominal gain setting is 550 kHz to 470 MHz.

Noise: At the nominal gain setting the noise voltage
- at the TIA output was simulated to be 770 uV RMS
- and 2.7 mV RMS at the output.

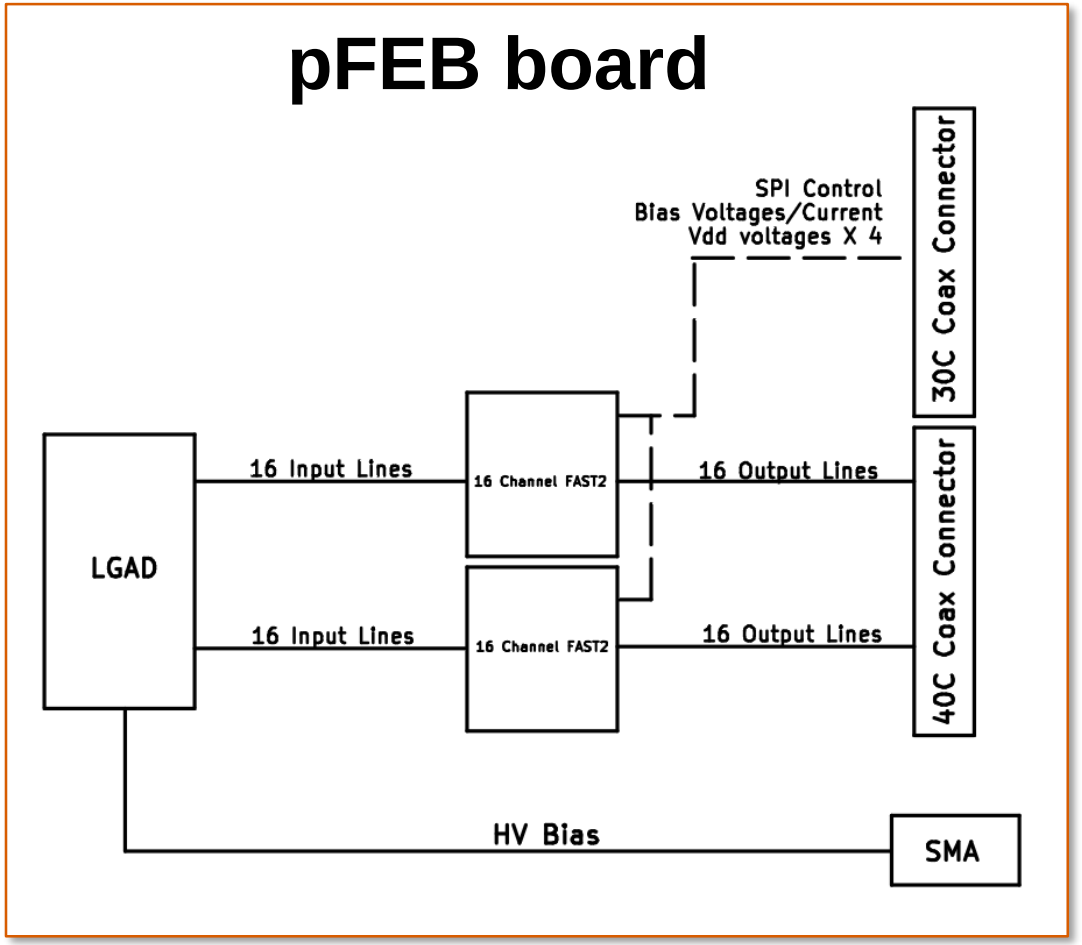
FAST2_EVO1 and EVO2



Design consideration and implementation I

collaboration UW-UCSC

- pFEB has two FAST2/3 chips, 32 channels, UCSC demo board single FAST2 chip
- The design was split into two boards (trying to minimize electronic close to LGAD)
  - the triangle shaped front end board (pFEB)
  - Motherboard with most of the support
- Boards connected by two CABLINE-CA multi conductor Micro-Coaxial cable assemblies
  - 40 position cable for the output and test pulse signals
  - 30 position cable for the power, control and bias signals

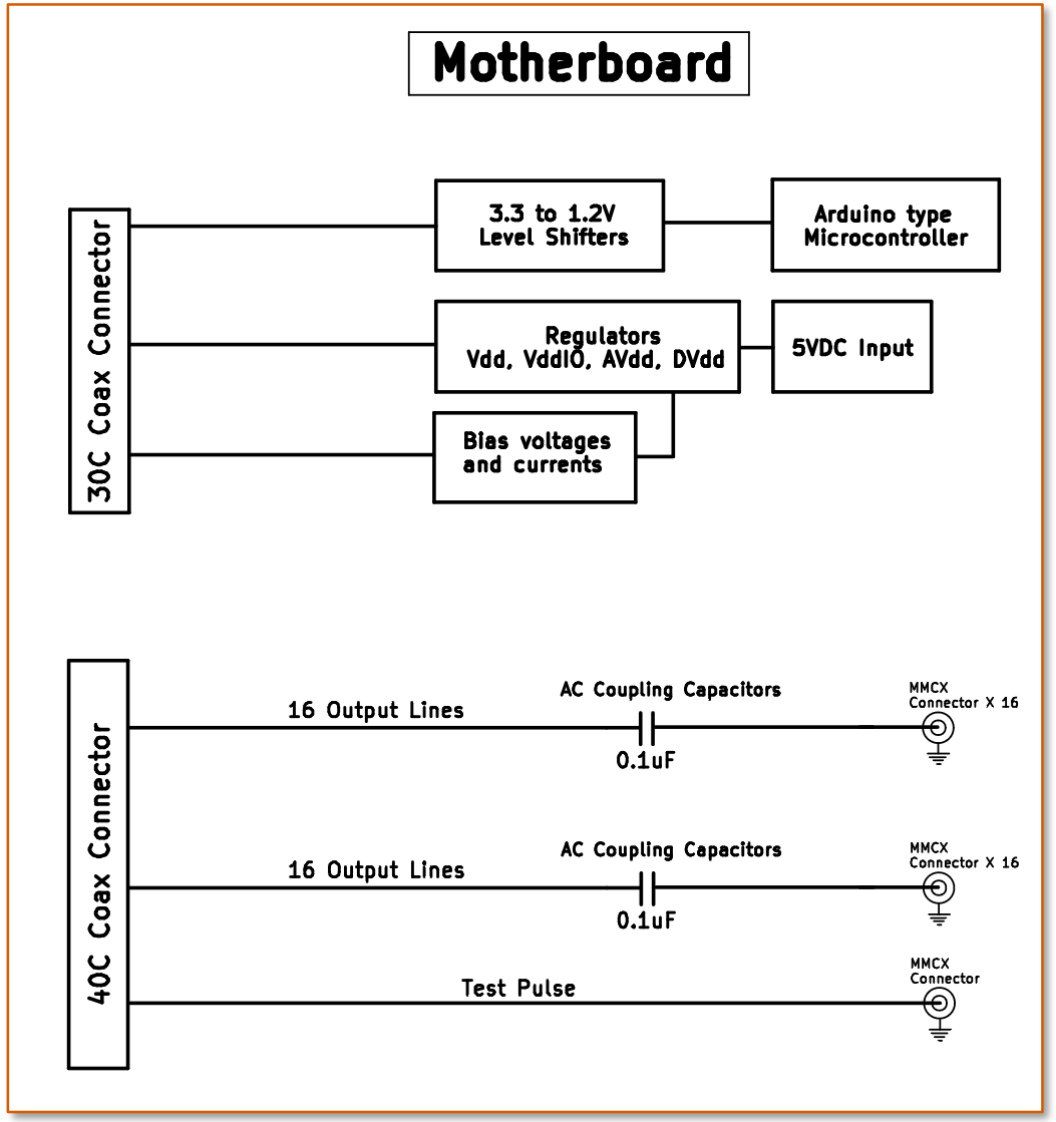


Design consideration and implementation II

collaboration UW-UCSC

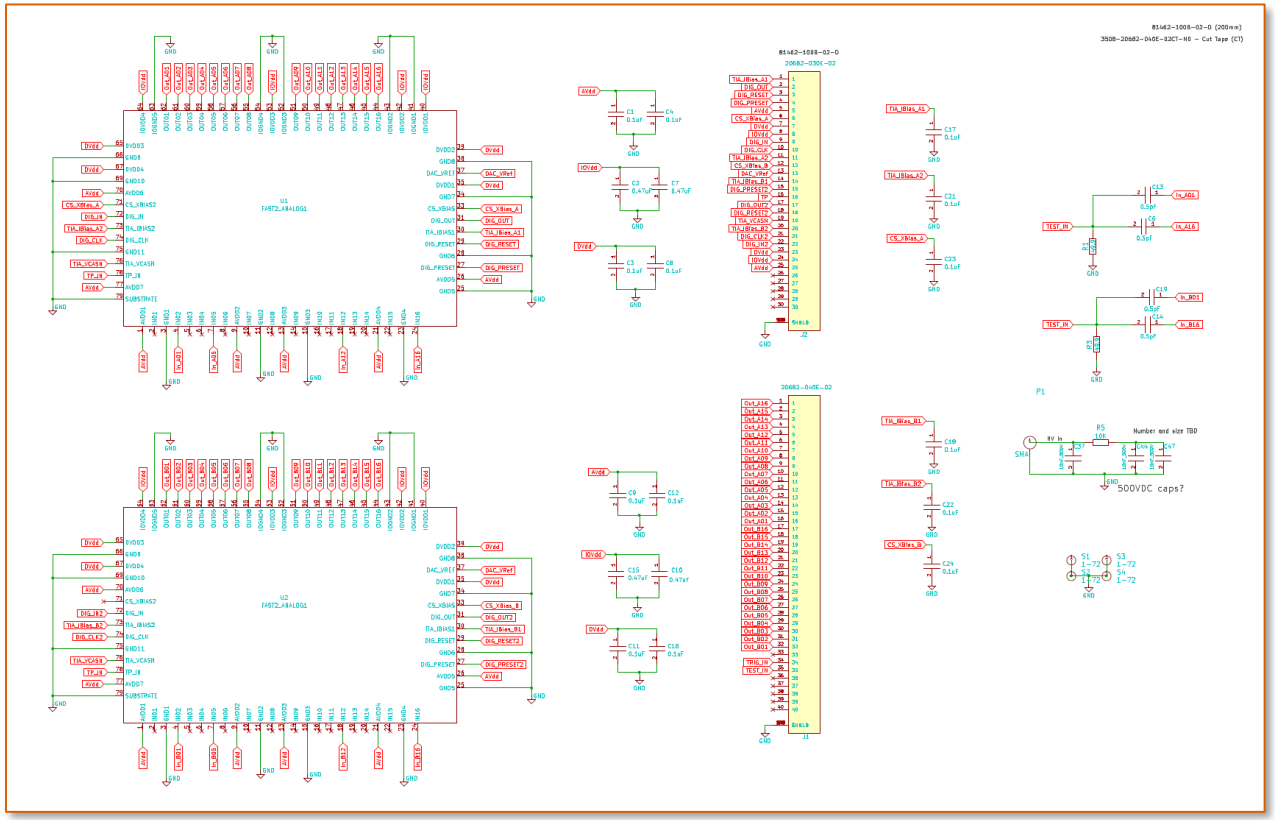
- Motherboard/Breakout board
  - ac coupling capacitor
  - MMCX connector output channel to digitizers.
  - FAST2/3 outputs are ac coupled due to ~700 mV dc bias on the output signals.

- Separate TIA Ibias current for each section of eight channels
  Original board had the TIA Ibias inputs of both sections connected together so not well defined how current splits between the two sections.

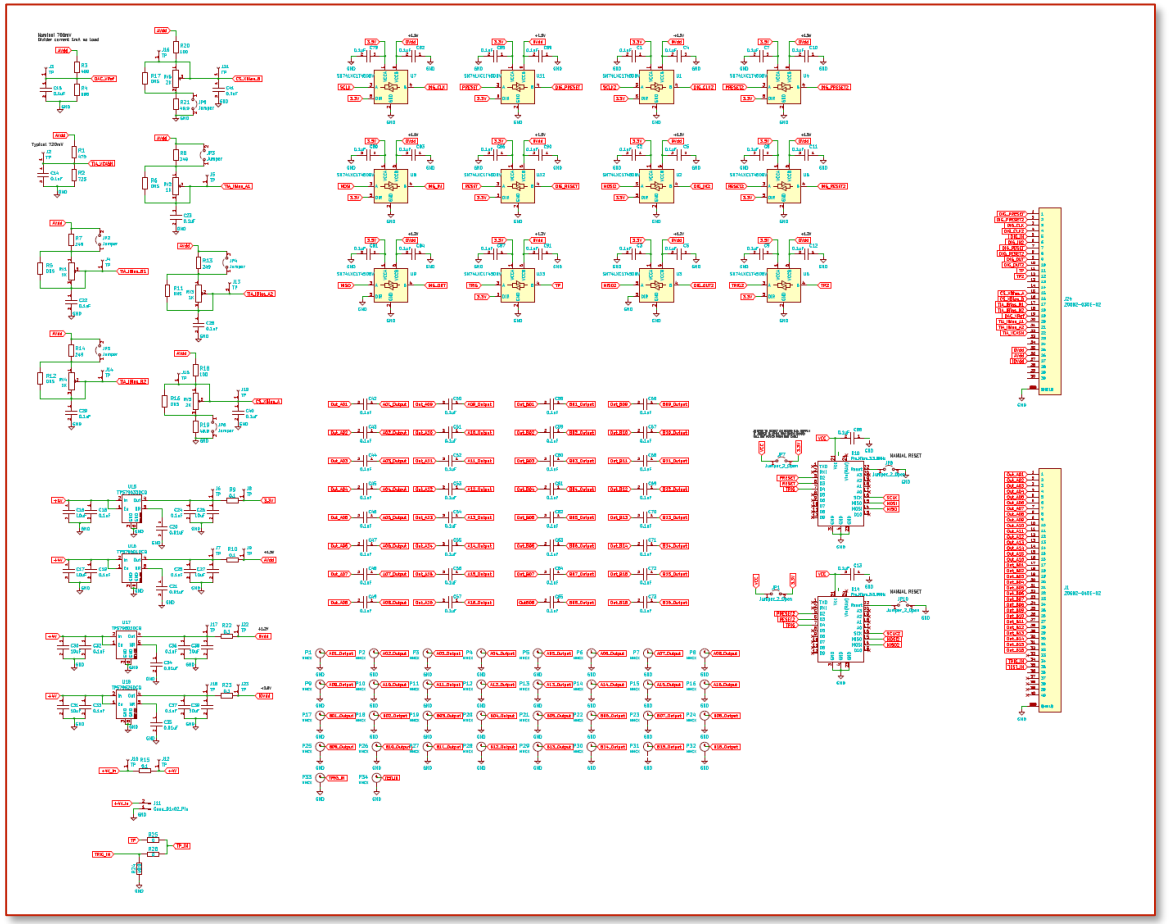


Schematics

pFEB

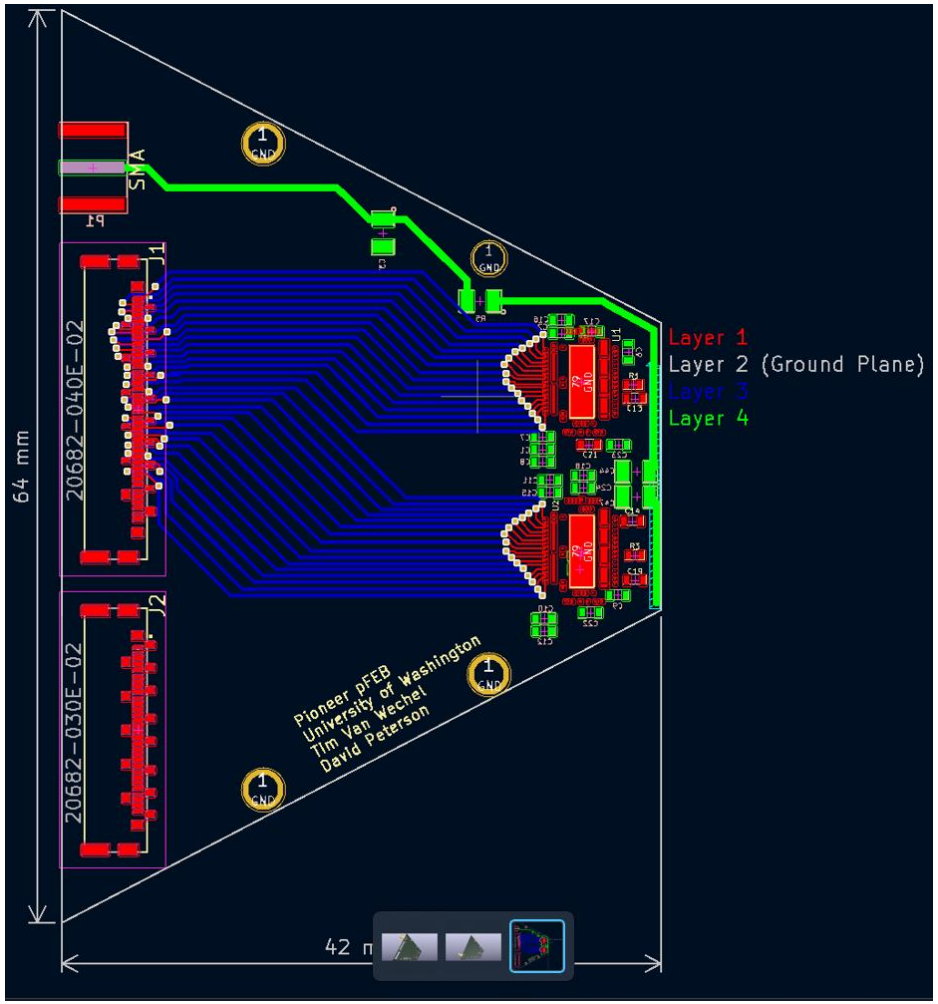


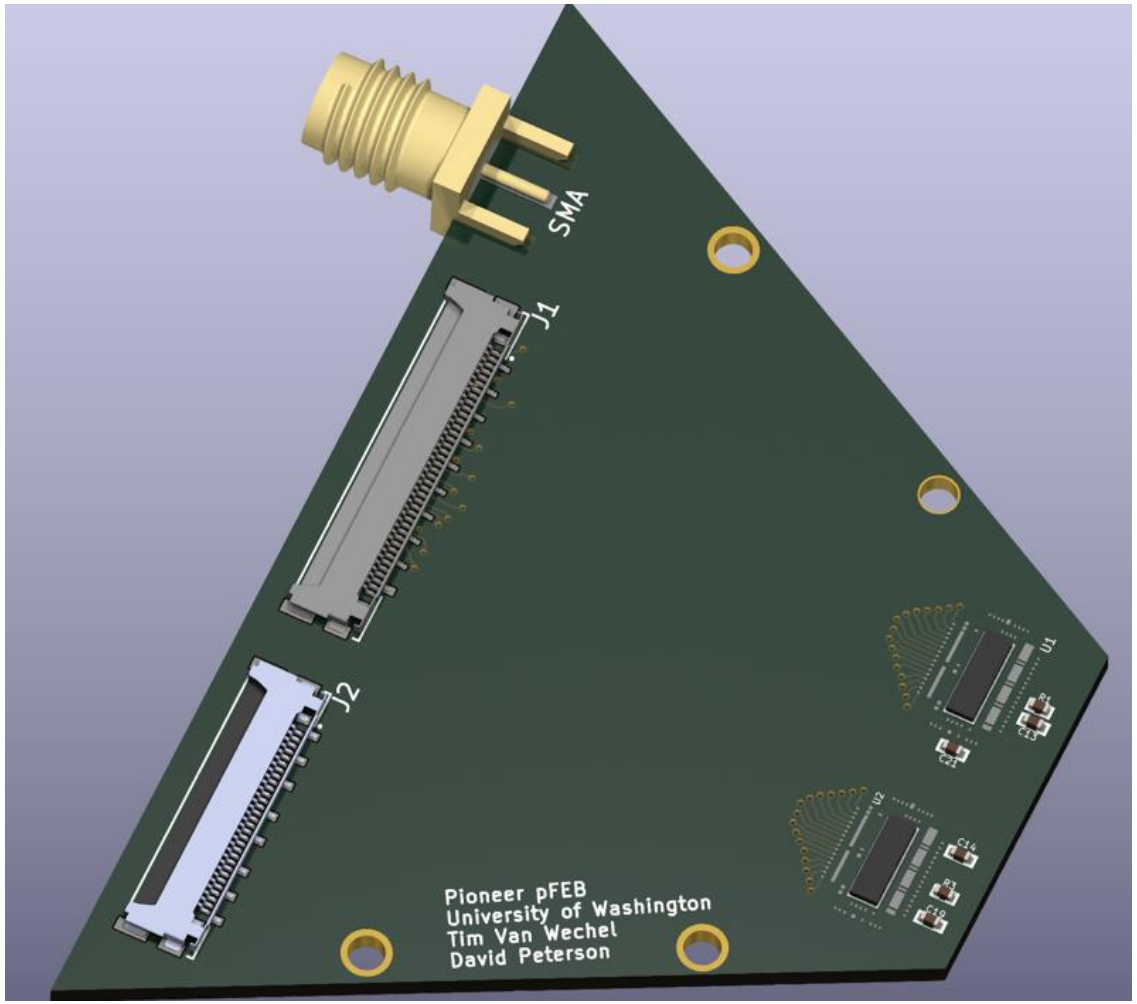
Motherboard



Very preliminary layout

to be reviewed this week





Backup

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