ATAR Geometry in Simulation Adam Molnar

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ATAR Geometry and Motivation

- Nominal ATAR has been put into the simulation sans mechanics (See Peter's talk and further discussions)
- ATAR parametrized to allow for simulation building of different geometries
- Additionally, nominal example .json files
- Attempted to include our best guess for the dead material given our current understanding of the experiment
- This talk will go through the motivation for a lot of the different elements of the ATAR simulation and why the values are what they are

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ATAR Active Region Basics

- PIONEER's nominal ATAR will consist of 48 layers of LGAD silicon sensors
- The bulk thickness of the sensors are 120µm
- Each layer will have 100 strips per layer each of these are considered as independent active volumes in the simulation
- At this point of time there is no nominal LGAD choice, but TI-LGADs and AC-LGADs are being investigated

Why the Nominal*Values

Asterisk, as these parameters are the initial stab at a design but will likely change as our ATAR simulation campaign begins

• The simulation is organized into meta objects known as sensors and sandwich layers

- A sandwich layer consists of the items in between the green dotted lines, 2 sensors and 1 high voltage region
- The sensors correspond to the red dashed lines, which include the aluminum strips and a backing region

ATAR Inactive Regions: High Voltage Layer

- What I call the HV layer is a model of what will be a more complex object for the final ATAR
- These LGAD sensors need high volage biasing and a mechanical object to support the sensors
- In the simulation this HV layer is a Kapton model of a nominal thickness of 10µm
- Furthermore, we envision that four rods would go through the corners of this region to provide support for the ATAR, unsure exact "overflow"

ATAR Inactive Regions: Sensor Metallization

- On every sensor there are two regions of aluminum metallization
- On the front side are the electrodes that read out the signals from the bulk of the sensor
- For the simulation assumed 100µm wide electrodes
- In the simulation electrodes sit on top of the strips, which are the active region
- On the backside is what we call the backing layer this is also metallized and will be giving the sensor it's high voltage bias
- Made the assumption that the electrodes and backing layer will always be the same thickness nominally 2µm

ATAR Inactive Regions: Guard Ring

- Around the active portion of the strips silicon sensors have an inactive region that in the simulation we call the guard ring, which is one element of that inactive region
- In the simulation this is nominally a 200µm frame and is also made of silicon
- There have been discussions of the fact that there is further dead material outside of the guard ring that could increase this area of dead region even up to 500µm

ATAR Inactive Regions: Passivation Layer

- Recently added to the simulation one can add a passivation layer to the sensors
- The passivation layer is a small region of inactive material deposited below the electrodes to stabilize the semiconductor chemically and electrically

ATAR Sensor Staggering

Sensors staggered for readout. Each layer has 2 sensors. Each layer will oscillate but only the "front" and "back" sensors. For example layer 1 sensor 1 will be read out on the right and layer 1 sensor 2 the bottom. Then layer 2 sensor 1 will be read out left and layer 2 sensor 2 top. Staggering by 300 μ m total 200

Working on developing AC-LGAD smearing. Have developed a triple Gaussian model, but have yet to incorporate it into the simulation framework.

Have implanted the TI-LGADs into the simulation as an inactive region. Technically the regions would produce signal, but have no gain.

ATAR Services

- Desire from the collaboration to include ATAR services in the simulation geometry
- Since moving to Pacman geometry there is no nominal services and must be determined (Peter's Talk)
- Once again if someone has expertise in viewing and manipulating GDML files in a cad viewer please let us know ASIC |

Conclusions and Future Work

- Much of the baseline ATAR is in the simulation and ready to begin a simulation campaign
- We need to determine a nominal design for the services and then coming up with a model to code into the geometry
- Melding the ATAR simulation effort back into the larger simulation framework effort
- Build in more accurate detector response
	- AC-LGAD charge sharing
	- Gain suppression

Double Sided Readout – Overview

- Double Sided Readout Motivation
- ATAR Assembly Concept
- Structure of physical sensors
- Implementation into geometry

Brief Motivation

- Background rejection capability for μDIF
	- Need to achieve at least 1% of π ev tail
	- To identify energy deposit of 0.1 -0.2 MIP $>$ must be able to see muon travelling $1 - 2 \mu m$
- Large angle with respect to strips
- Need to minimize dead material and intersensor gaps!
	- Nominal geometry utilizes 25 μm layer gap
		- High chance of missing muon decay
		- Additional benefit of improved S/N
			- Reduced crosstalk and input capacitances -> lower ENC

V1 Double Sided Assembly Concept

- Stacks of sensors with both sides instrumented for readout
	- V1 keeps each sensor the same dimensions
	- V2 will implement "pyramid scheme"
- Neighboring Si layers share readout
	- Orthogonal electrodes for x-y coverage
	- Mixed signal can be deconstructed
	- Known "cross talk"
- Gap between active regions defined by electrode thickness

Geometry Implementation

- Si Bulk
	- 2 cm x 2 cm
	- 120 μm thickness

2 cm

Geometry Implementation 2 cm 200 μm 2 μm • Si Bulk • 2 cm x 2 cm 120 μm ╰V 100 μm • 120 μm thickness • 100 Electrodes each side • 2 μm thickness • 100 μm width \cdot 200 μ m pitch Si

Side cross section Top down 5

Geometry Implementation 2 cm 200 μm 2 μm • Si Bulk • 2 cm x 2 cm 120 μm ╰Ѵ 100 μm • 120 μm thickness • 100 Electrodes each side • 2 μm thickness • 100 μm width Si • 200 μm pitch • Guard Ring • For geometry purposes just a wall of Si • 500 μm width Motivated by current ∧ sensors produced by 500 um Gabriele! **Example 1998** Side cross section Top down

Geometry Implementation

- Si Bulk
	- $2 \text{ cm} \times 2 \text{ cm}$
	- 120 μm thickness
- 100 Electrodes each side
	- 2 μm thickness
	- 100 μm width
	- 200 μm pitch
- Guard Ring
	- For geometry purposes just a wall of Si
	- 500 μm width
- Dead Material
	- Representative of oxide and passivation
	- Also just Si
	- \cdot 1-2 μ m thickness depending on sensor type

Side cross section

Geometry Implementation 2 cm 200 μ m 2 μ m • Si Bulk • $2 \text{ cm} \times 2 \text{ cm}$ 120 μ m ╰Ѵ • 120 μm thickness 100 μ m • 100 Electrodes each side • 2 μm thickness • 100 μm width • 200 μm pitch Si • Guard Ring • For geometry purposes just a wall of Si • 500 μm width • Dead Material • Representative of oxide and passivation $2 \mu m$ ∧ • Also just Si • 1-2 μm thickness 500 um 8Side cross Top down

Parameters

- "DoubleSided" boolean to use this geometry
	- Allows for single atar.py file with different configs (.json)
- Requires square sensor area
	- Strip width x N_{strips} = strip length
	- Required for proper alignment of electrodes

"target":{ "DoubleSided": true, " $xPos" : 0.0$, "yPos": 0.0, "zPos": 0.0 , "nLayers" $: 48.$ "layerStagger":0, "stripWidth": 0.02, "stripLength": 2.0, "stripThickness":0.012, "nStrips" $: 100.$ "stripMaterial": "Silicon", "electrodeWidth": 0.01, "electrodeMaterial":"Aluminum", "instrumentWithTILGAD":false, "TILGADTrenchWidth":0, "backingAndElectrodeThickness":0.0002, "backingMaterial":"Aluminum", "hvThickness":0, "hvLengthPastSensor":0, "hvMaterial":"Kapton", "makeGuard":true, "guardWidth":0.1, "quardMaterial":"Silicon", "layerBuffer" : 0, "debug": false, "passivationLayer" : true, "passivationThickness": 0.0002

Next Steps

- Geometry additions
	- V2 "Pyramid Scheme"
	- Readouts/Route in HV
- Framework to handle Double Sided
	- Not implementing strips -> use
		- voxelization/segmentation
			- Needs to be figured out (Guidance appreciated)

Next Steps

- 1. First demonstrate readout capability
- 2. Overall improvement on background rejection compared to nominal
- 3. Effectiveness of gap reduction
	- 25 -> 4 μ m (2x electrode thickness)
- 4. Performance over different Si bulk thicknesses
	- Challenges in producing 120 μm wafers at BNL
	- How much can we afford to increase?

Backup

BNL Sensors

