Hardware progress from BNL

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PIONEER collaboration meeting October 16-18, 2023, Seattle, WA

Contents

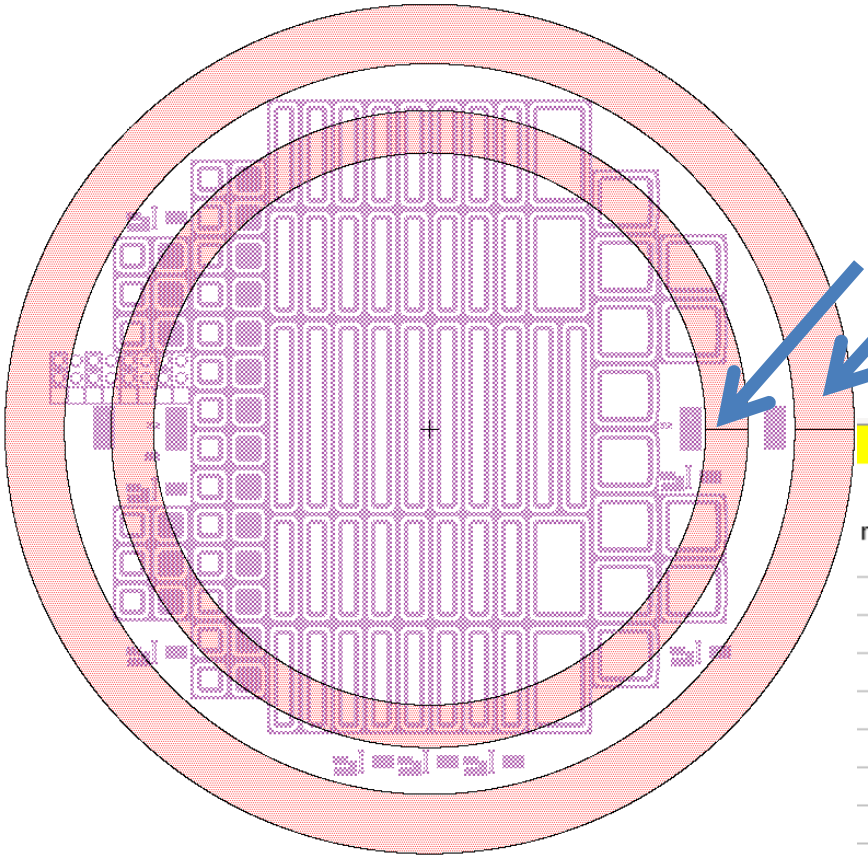
- Small sensor prototype development and production for ATAR
- Frontend electronics development prospects
- Characterization of VMM chip – Siddhant Mehrotra

Small sensor prototype fabrication

- 2yrs LDRD awarded in 2022, second year started October 1st, 2023
- Wafers ordering – July 2022
- Dicing and characterization started September 2023
- Goal: produce small prototypes of 120-um-thick LGAD sensors for PIONEER. Prove their handling with standard clean-room tools at BNL. Take characterization measurements with the sensors.

Layout of the wafers

Gabriele Giacomini



5x3” wafer: 120um thick (one-sided device); update: damaged 2 wafers during mfg.
3x4” wafer: 200um thick

Using same mask set for 3” and 4” wafers to minimize the total cost.

DC strips				
multiplicity in 4" wafer	multiplicity in 3" wafer		Width (um)	Pitch (um)
20x	9x	2mmx2mm	single channel	
8x	4x	1cm x 1mm	100	200
8x	4x	1cm x 1mm	50	200
2x	2x	2cm x 2mm	50	200
3x	3x	2cm x 2mm	100	200
2x	1x	1cm x 0.5cm	200	500
2x	0	0.5cm x 0.5cm	100	500
2x	1x	0.5cm x 0.5cm	200	500
1x	0	0.5cm x 0.5cm	300	500
1x	1x	0.5cm x 0.5cm	100	200

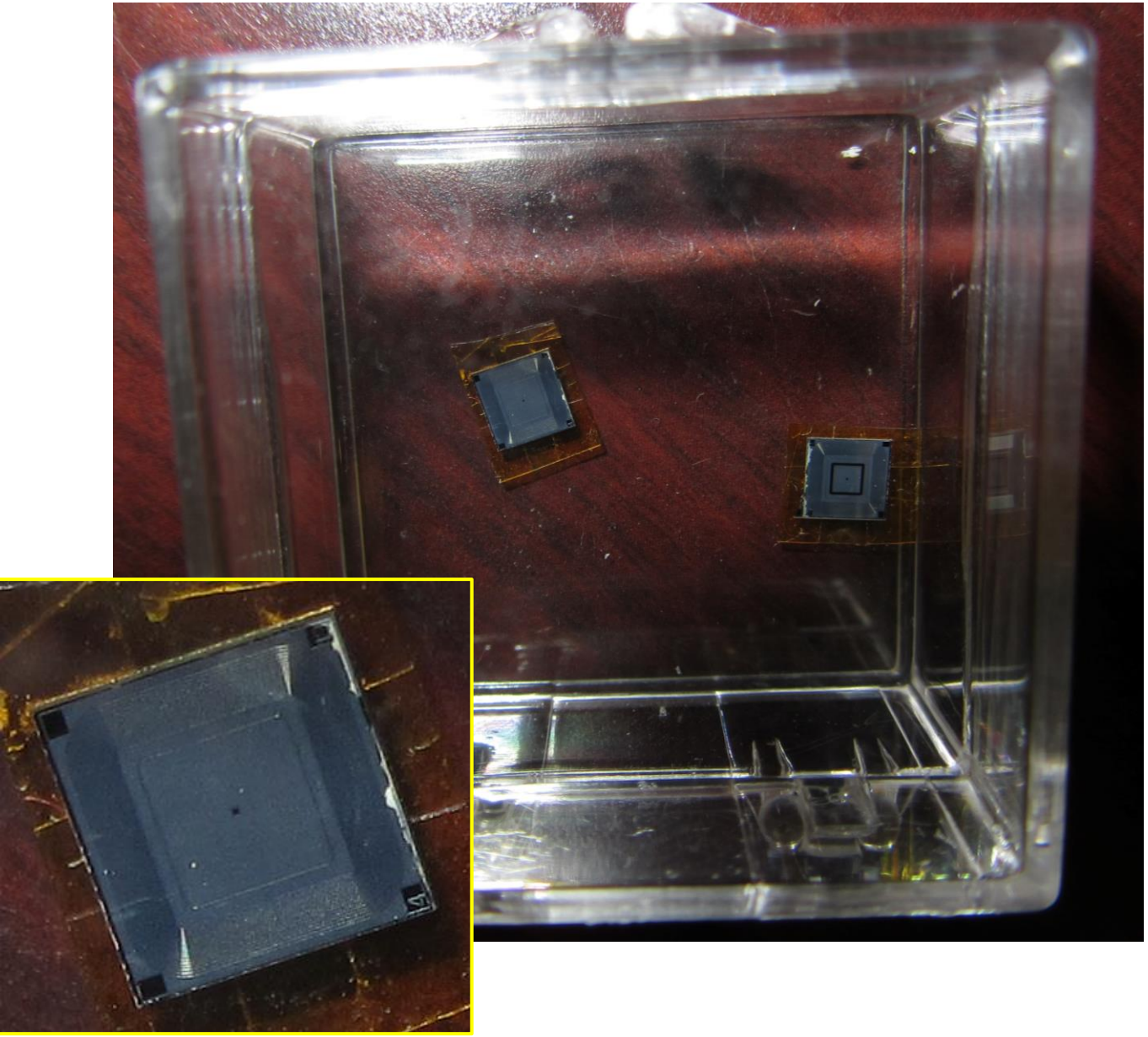
AC-LGAD				
multiplicity in 4" wafer	multiplicity in 3" wafer		Width (um)	Pitch (um)
20x	9x	2mmx2mm	single channel	
4x	2x	1cm x 1mm	80	200
8x	4x	1cm x 1mm	100	200
4x	2x	1cm x 1mm	150	200
1x	1x	2cm x 1mm	80	200
3x	3x	2cm x 1mm	100	200
1x	1x	2cm x 1mm	150	200
1x	0	1cm x 0.5cm	200	500
1x	1x	1cm x 0.5cm	100	500
2x	0	0.5cm x 0.5cm	100	500
2x	1x	0.5cm x 0.5cm	200	500
1x	1x	0.5cm x 0.5cm	300	500
1x	0	0.5cm x 0.5cm	400	500

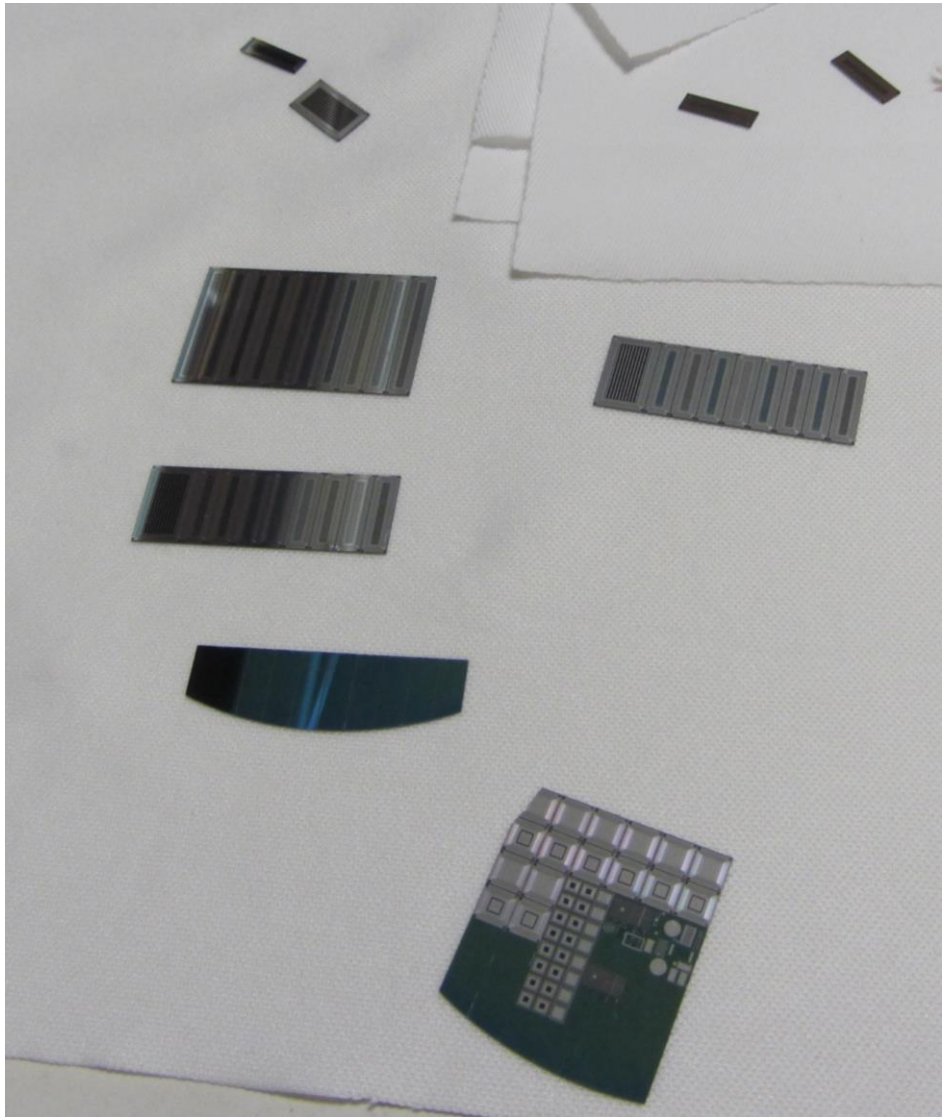
Back: p+ DC-coupled strips
4 lithographies and 1 implant: p+ implant, contacts, passivation opening

n-side: 6 lithographies and 3implants: deep n+ implant (or Junction Termination Edge, JTE), resistive implant (AC-LGAD devices), gain layer (AC-LGAD devices), contacts, metal and passivation opening.

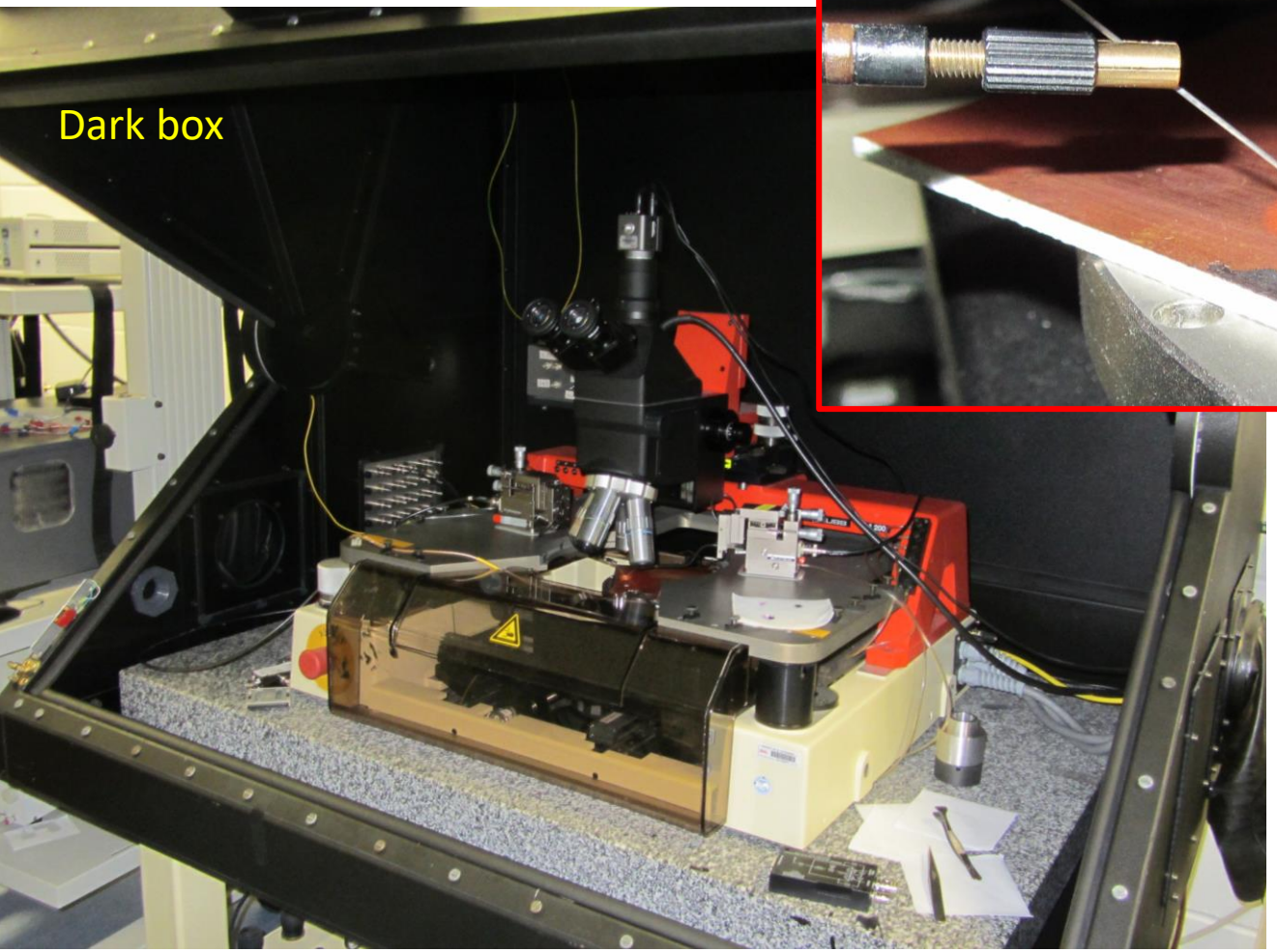
Resistive layer dose: 1, 1.5, 2 x 10^{13} cm^{-2} on different wafers

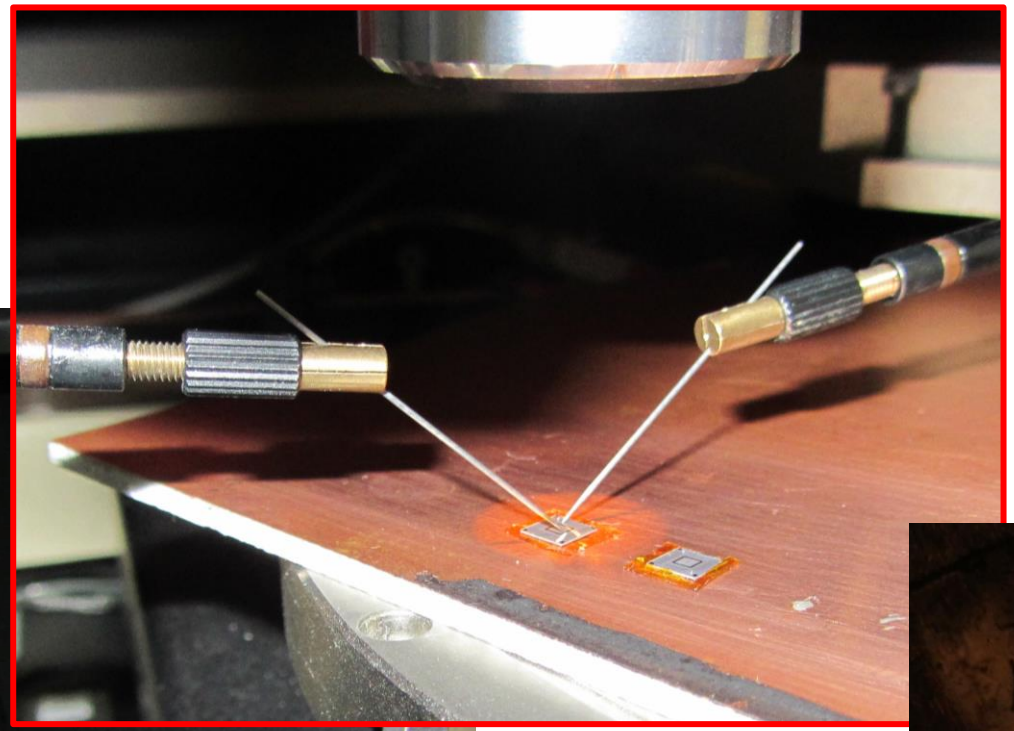
200 um sensors – dicing one 4” wafer

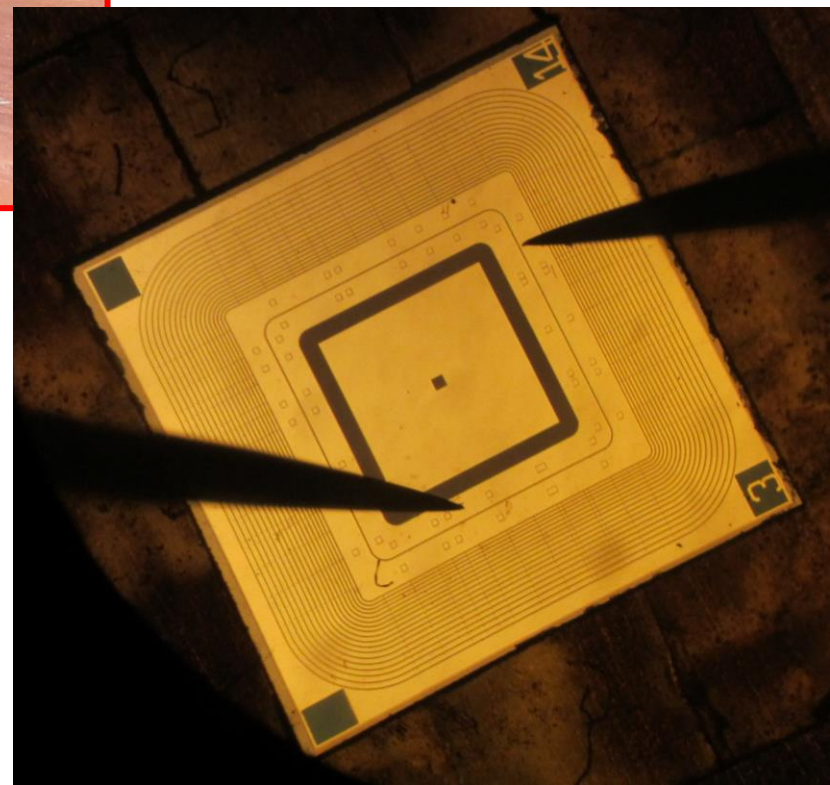




200 um sensors – basic checkup setup

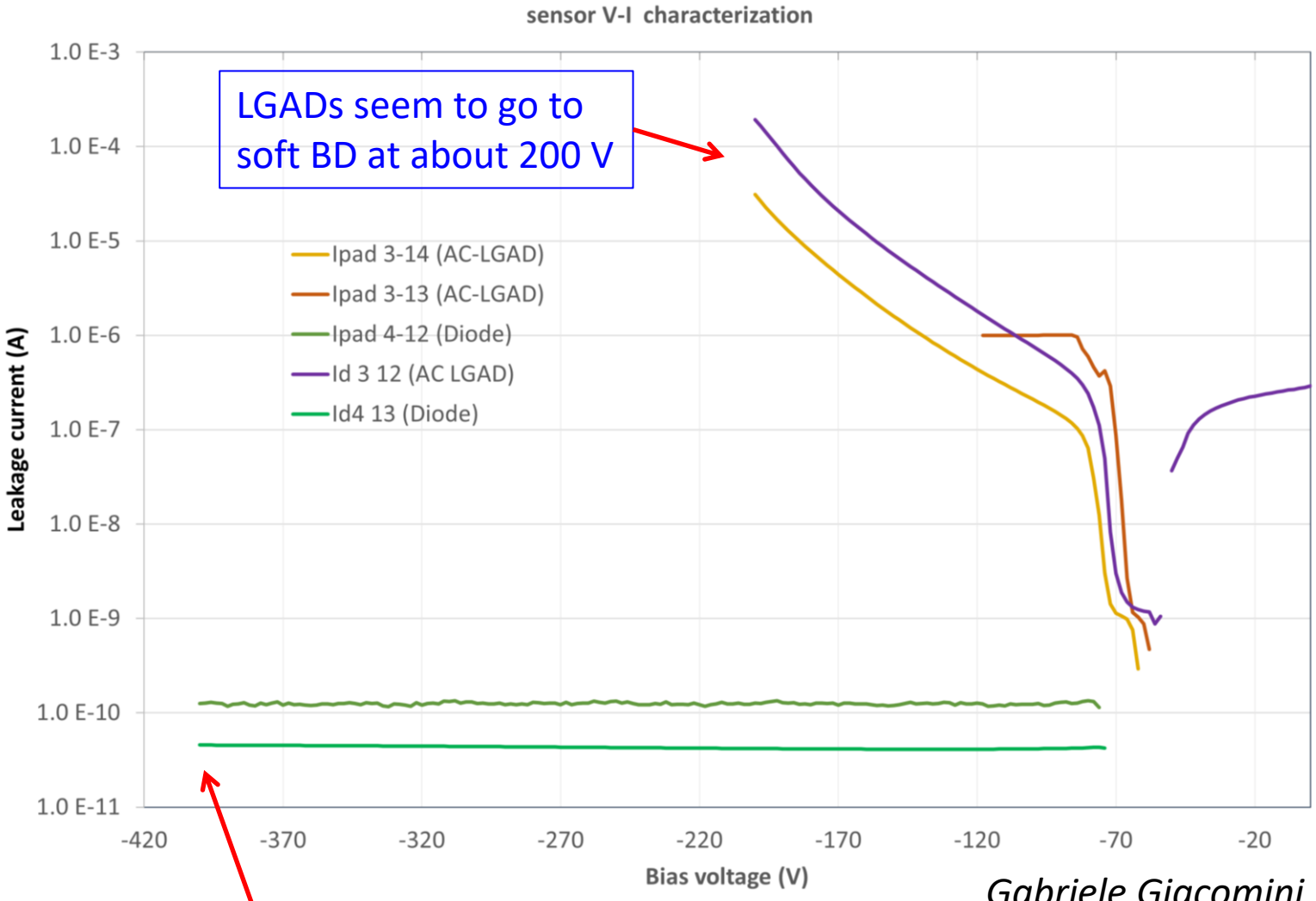






200 um sensors characterization – in progress

Single channel devices from one 200um-thick wafer, not passivated.

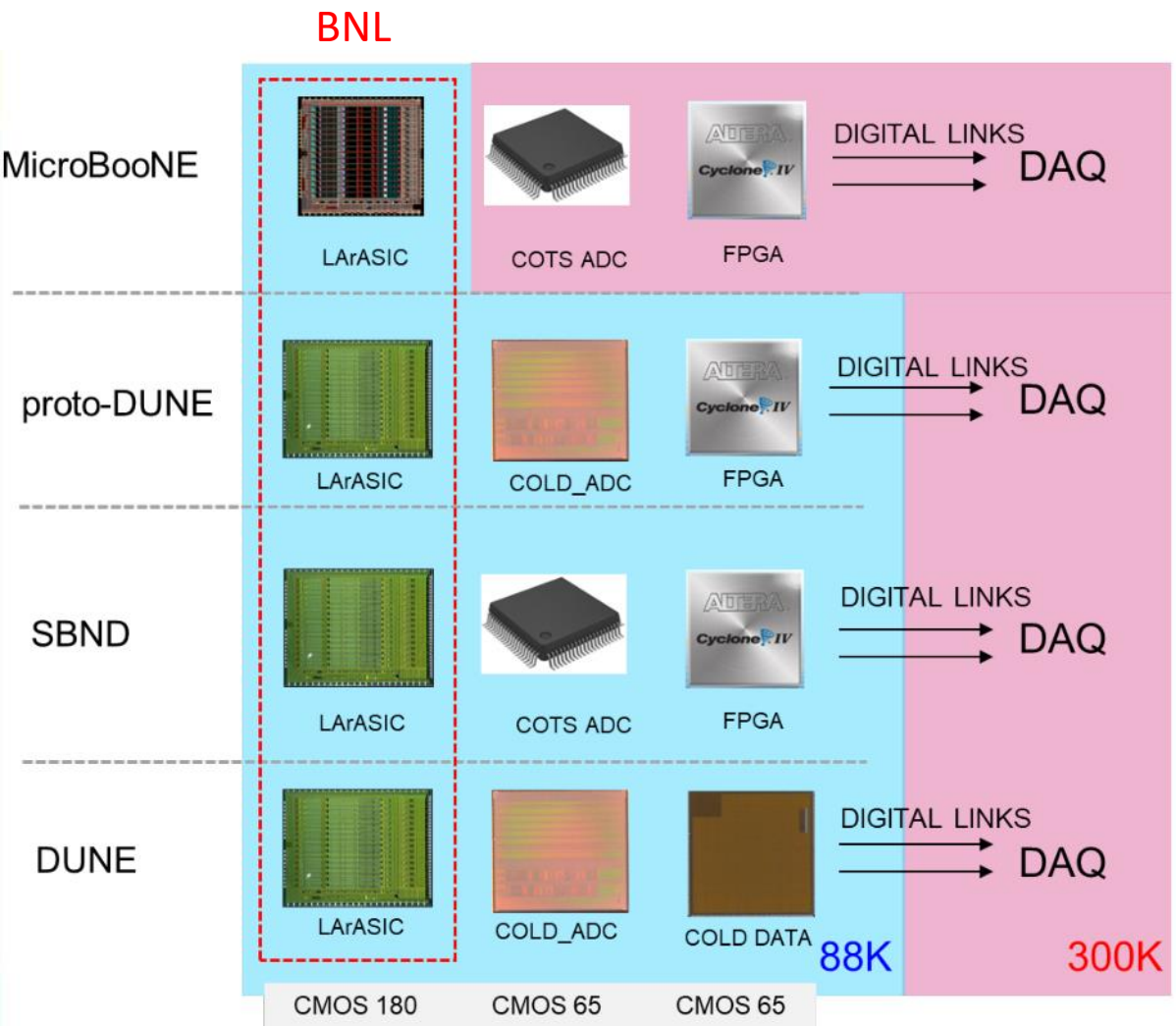


- Basic characterization of produced sensors started.
- Provided several sensors to UCSC for independent characterization. More sensors requested, will be provided soon.
- The analysis of the observed features is in progress.
- Sensors from other wafers will be tested soon.

Gabriele Giacomini

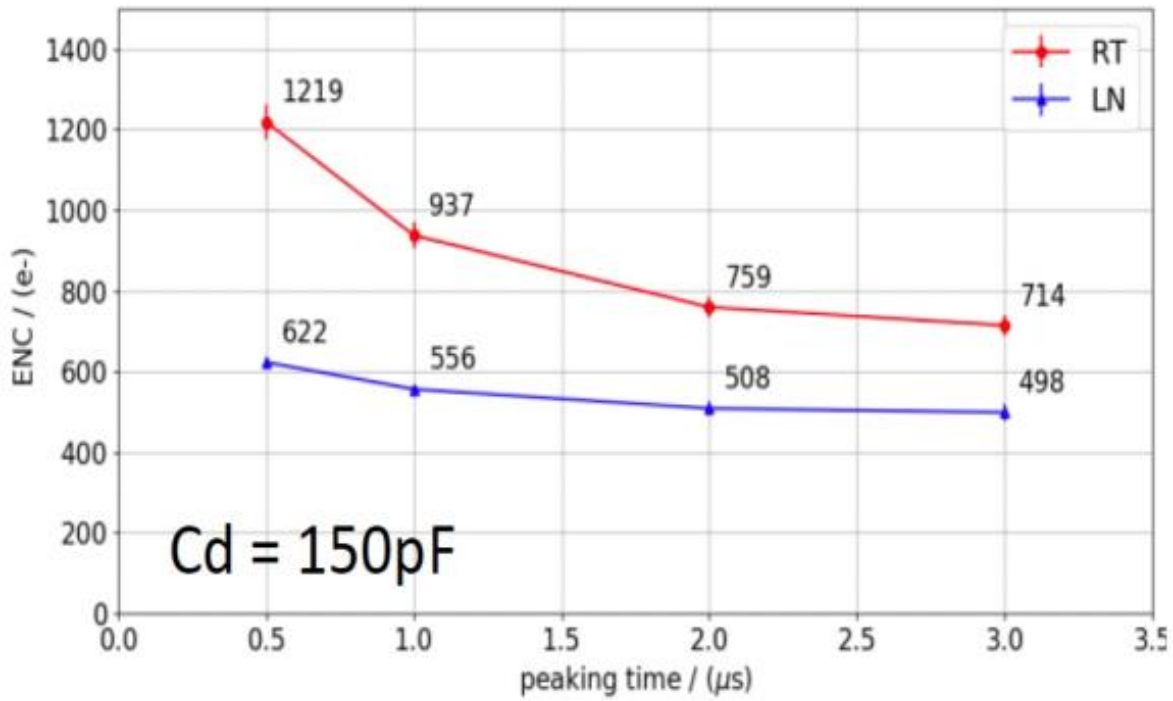
Development of frontend ASICs at BNL

Prashansa Mukim, LIDINE 2023



All three ASICS (FE+ADC+serializer) share same FrontEnd MotherBoard PCB.

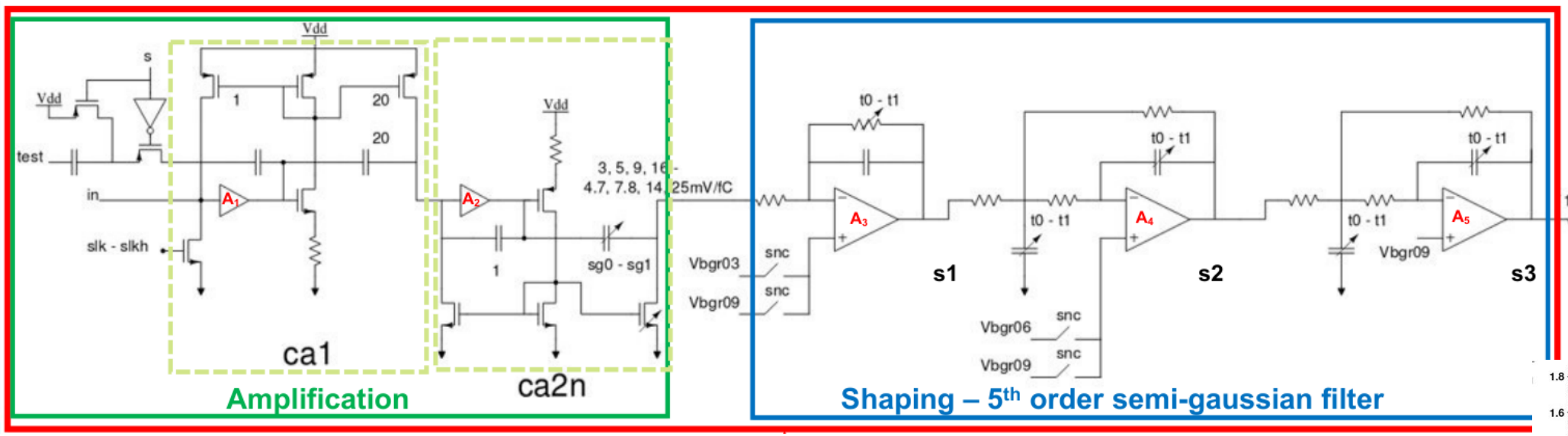
LArASIC frontend chip for DUNE



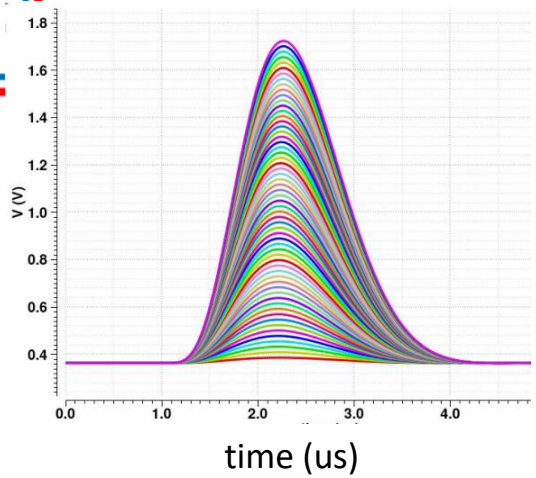
Design currently being translated to 65 nm CMOS.
Opportunity for PIONEER for frontend chip design
Customization for shorter shaping times (~20 ns, Cd.~20 pF).

LArASIC 180 → 65 nm translation status

Prashansa Mukim, LIDINE 2023



Design in 65 nm competed with 3 mW power consumption



- Charge amplifiers use current-mirror based adaptive continuous reset
- A1 and A2 are 3-stage amplifiers (> 100 dB gain)
- Input stage transistor for A1 implemented using thick oxide (2.5V) devices in 65 nm to limit leakage current and associated shot noise. Input stage transistor sized to have Cg~40 pF, optimal choice for minimizing noise with Cd~150 pF with given power budget.
- Pole zero cancellation ensures fast current pulse and prevents baseline drift.
- Implemented shaper is 5th order semi-gaussian filter with complex conjugate poles.
- (Nearly) equal rise and fall times maximize the output signal and amplitude for a given pulse duration

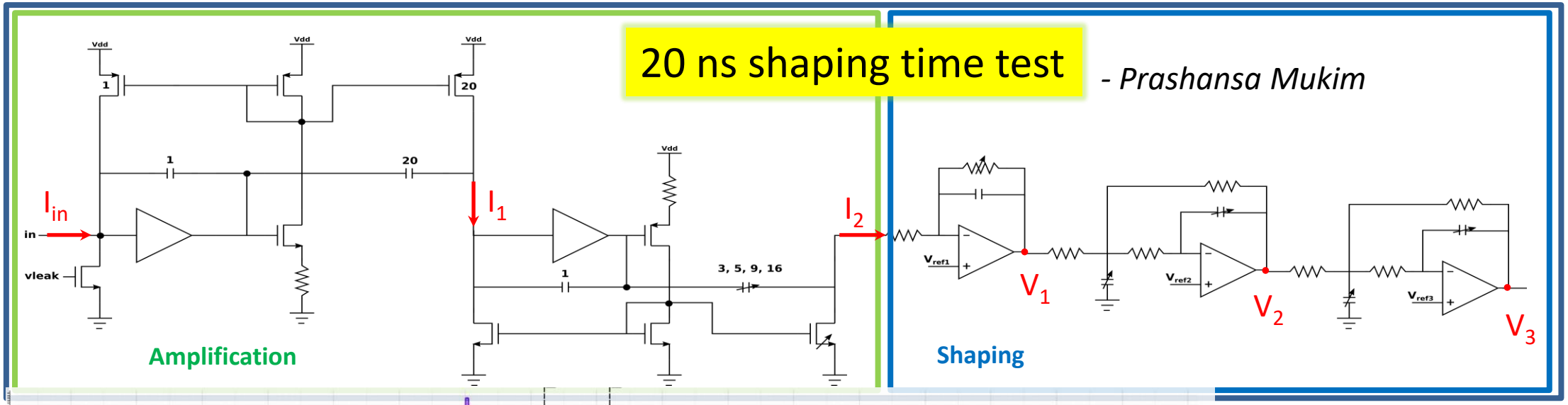
LArASIC 180 → 65 nm translation status

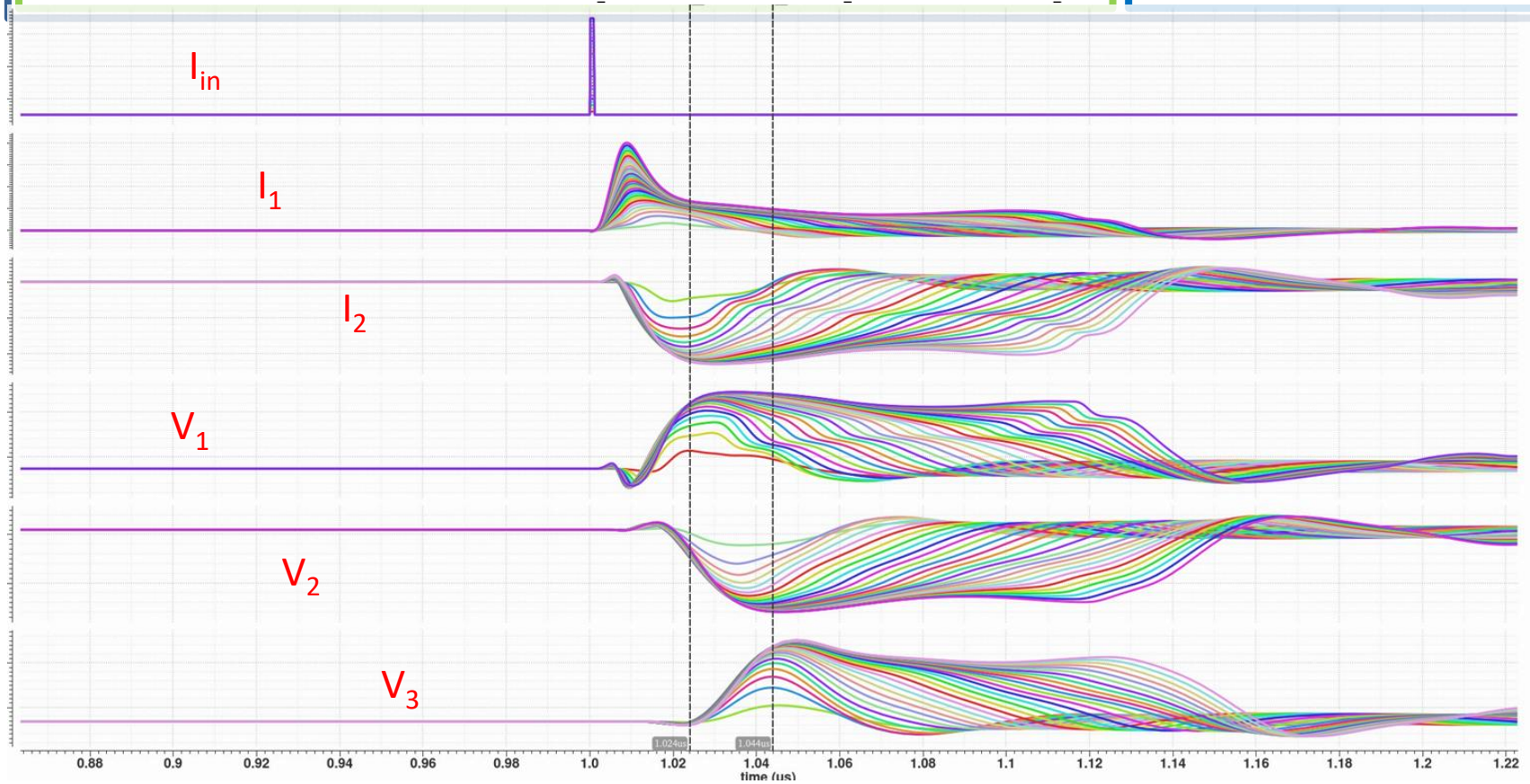
Prashansa Mukim, LIDINE 2023

Technology	180 nm CMOS – 1-poly, 6-metal, MiM cap, sil blk resistors				65 nm CMOS: 1-poly, 9-metal
Supply Voltage	1.8 V				✓
Temperature Range	77 – 300 K (-196 – 27 °C) optimized for 87k (-186 °C)				✓
Number of Channels	16				✓
Max Single-Ended Output Swing	1.4 V peak to peak (0.2 – 1.6 V)				✓
Gain Selection (mV/fC)	4.7	7.8	14	25	✓
Full-Scale Input Charge (fC)	300	180	100	56	✓
Baseline selection	200 mV (collection mode)		900 mV (induction mode)		✓
Charge Preamplifier Polarity	Negative (collection mode)		Bipolar (induction mode)		✓
Adaptive-Reset Current Selection (nA)	0.1	0.5	1	5	✓
Shaper Peaking Time Selection (µs)	0.5	1	2	3	✓
Output Coupling	AC (100 µs HPF time-constant)		DC		✓
Output Selection	Shaper	SE buffer	SEDC buffer		✓
Total Channel Settings	1024				
Integrated Test Capacitor	200 fF				
Temperature Sensor	0.8728 V @ 25°C + 2.868 mV/°C				
Integrated Pulse Generator	6-bit DAC based				
Configuration Control	SPI interface with 144 register bits				I²C interface

20 ns shaping time test

- Prashansa Mukim



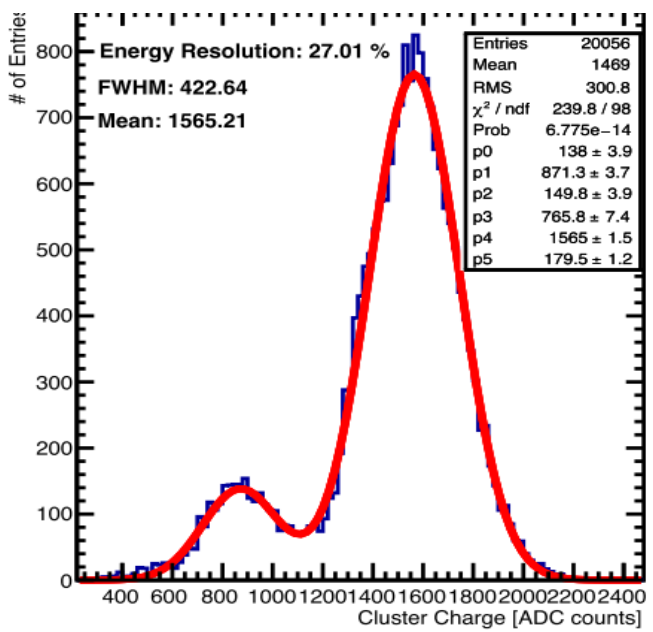


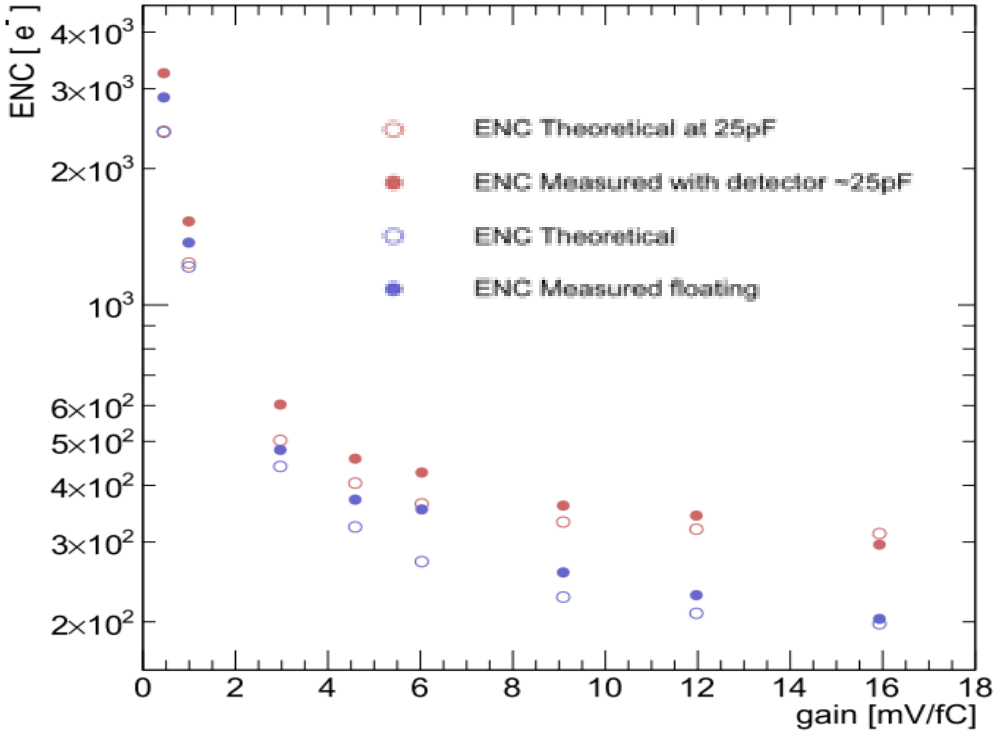
- The shaping circuit performs reasonably well.
- The amplification circuit requires modifications. Not surprising since it was optimized for (slower) TPC signals.
- No obvious showstoppers for conversion to ~20ns shaping time.
- Resources are needed to support the design work.

VMM3a – Why?

- Prototype ATAR readout for PIN
- Low noise
  - DDF architecture -> low C_{in}
- Fast shaping time (25 ns)
  - Cannot separate peaks within 5 ns but enough for first try
  - T_0 timing resolution of 0.4 ns can be achieved
- Immediate shortcomings
  - 10-bit ADC w/7.5 ENOB
    - Limt dynamic range
- Measurement capabilities
  - Even with ENOB can reach 20 MIP
  - Higher if require less S/N

Measurement of Fe55 demonstrates VMM's capabilities



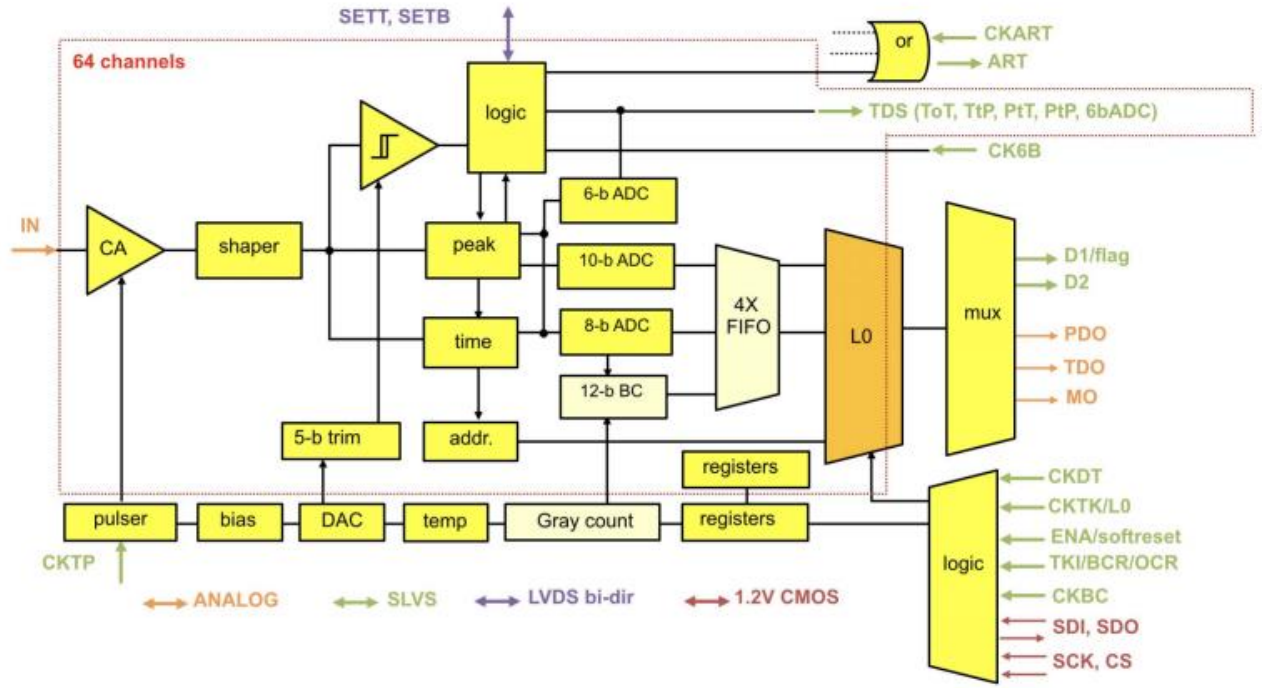


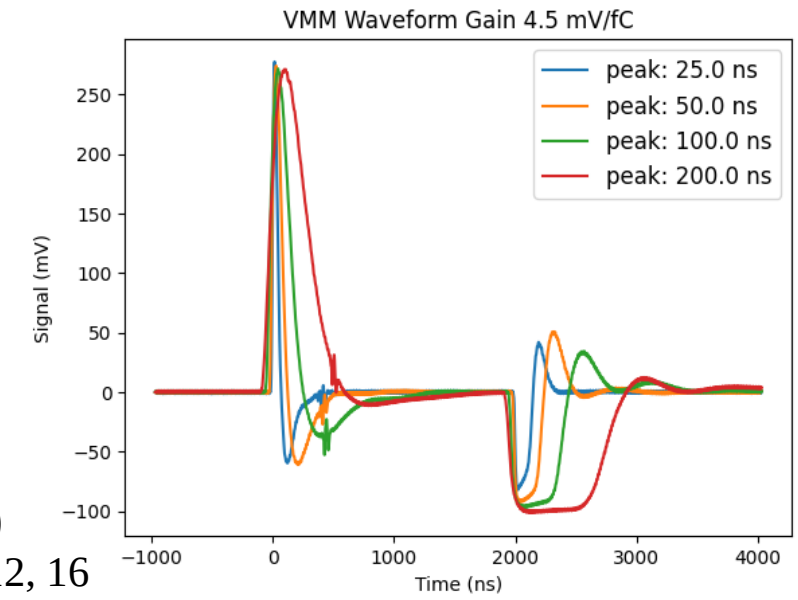
ENC for range of VMM gain settings

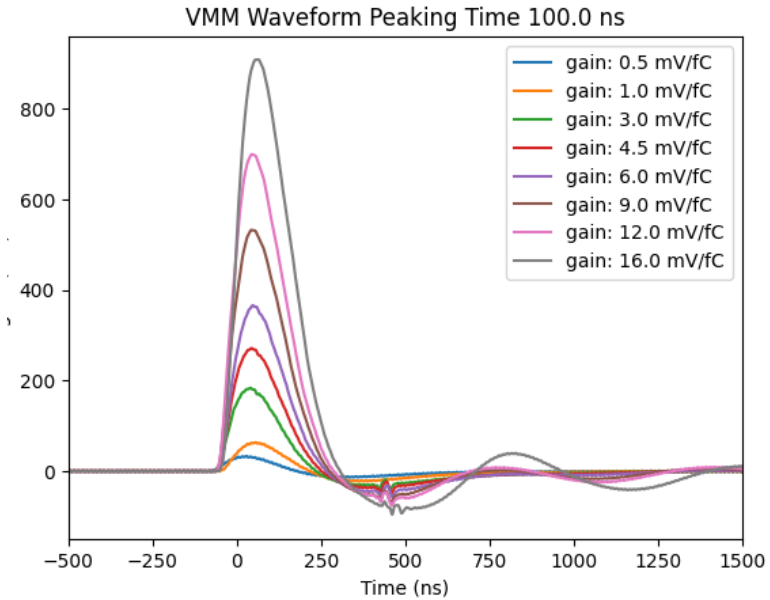
De Geronimo. (2022). The vmm3a asic. *IEEE Transactions on Nuclear Science*, *69*(4), 976-985.

VMM3a –ATLAS ASIC

- 64 front end channels
- 3 stage low noise charge amp
  - Programmable input polarity
  - Test capacitor
- 3rd order shaper
  - Delayed Dissipative Feedback
- Mixed Signal Output
  - Discrimination
    - 20 mV hysteresis
  - PDO, TDO



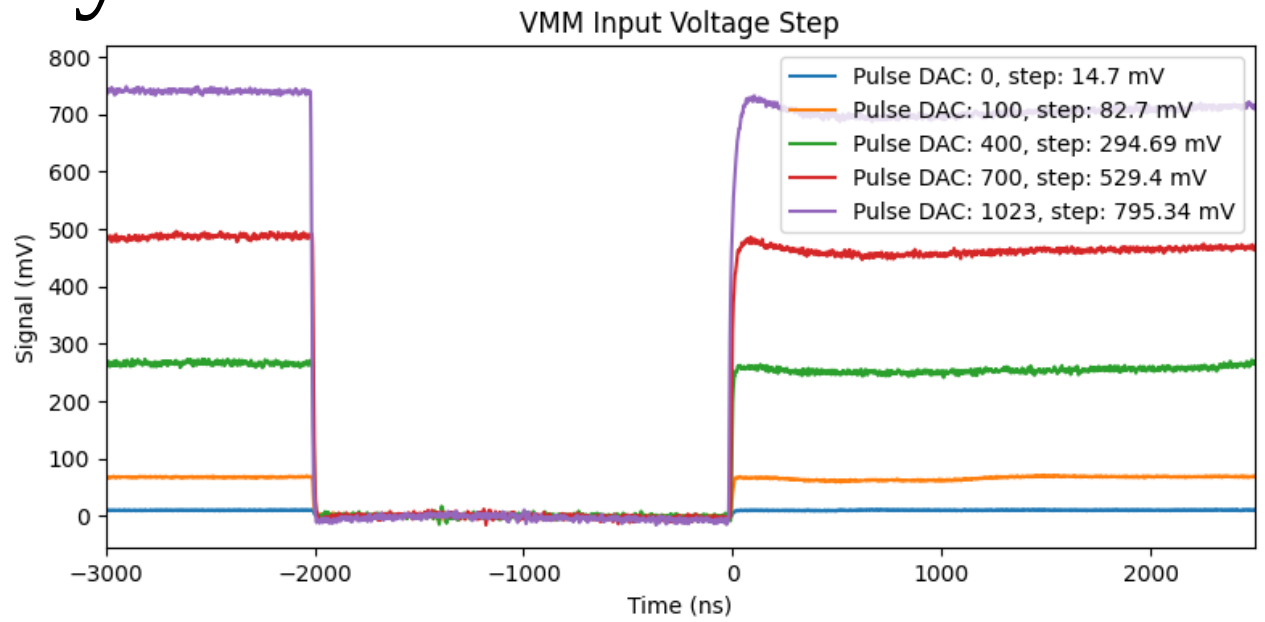


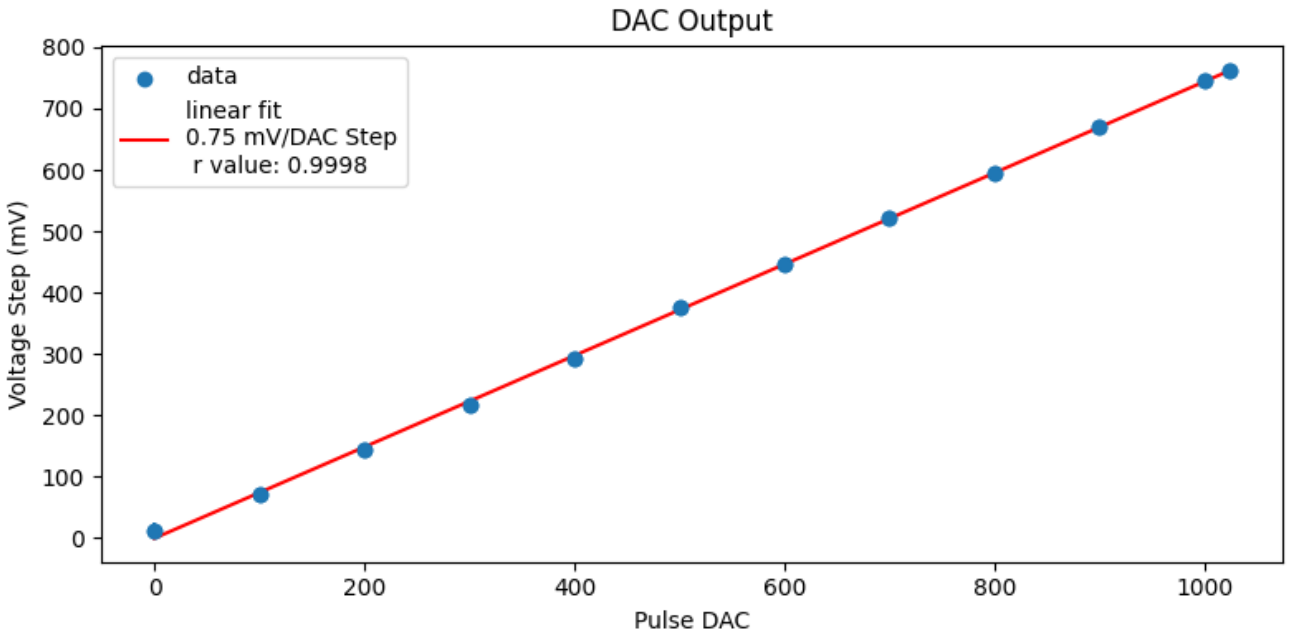


Adjustable Peaking Time
25, 50, 100, 200 ns
Adjustable Gain (mV/fC)
0.5, 1, 3, 4.5, 6, 9, 12, 16

Characterization – Linearity

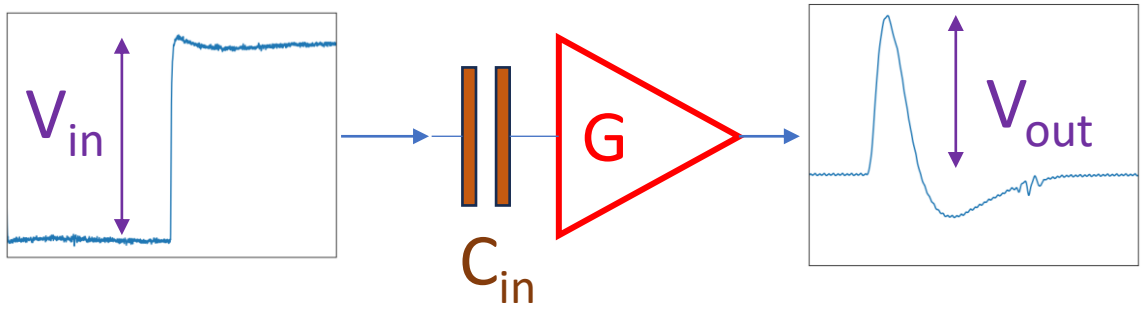
- Measured output of pulser DAC directly
- Fitted output against configured DAC input
  - **0.75 mV/DAC step**
  - Use to test gain accuracy
- Expected Dynamic Range ~180
  - ENOB: ~7.5 -> $2^{7.5}$
- **Measured Dynamic Range ~205 (46 dB)**





Characterization – Gain Accuracy

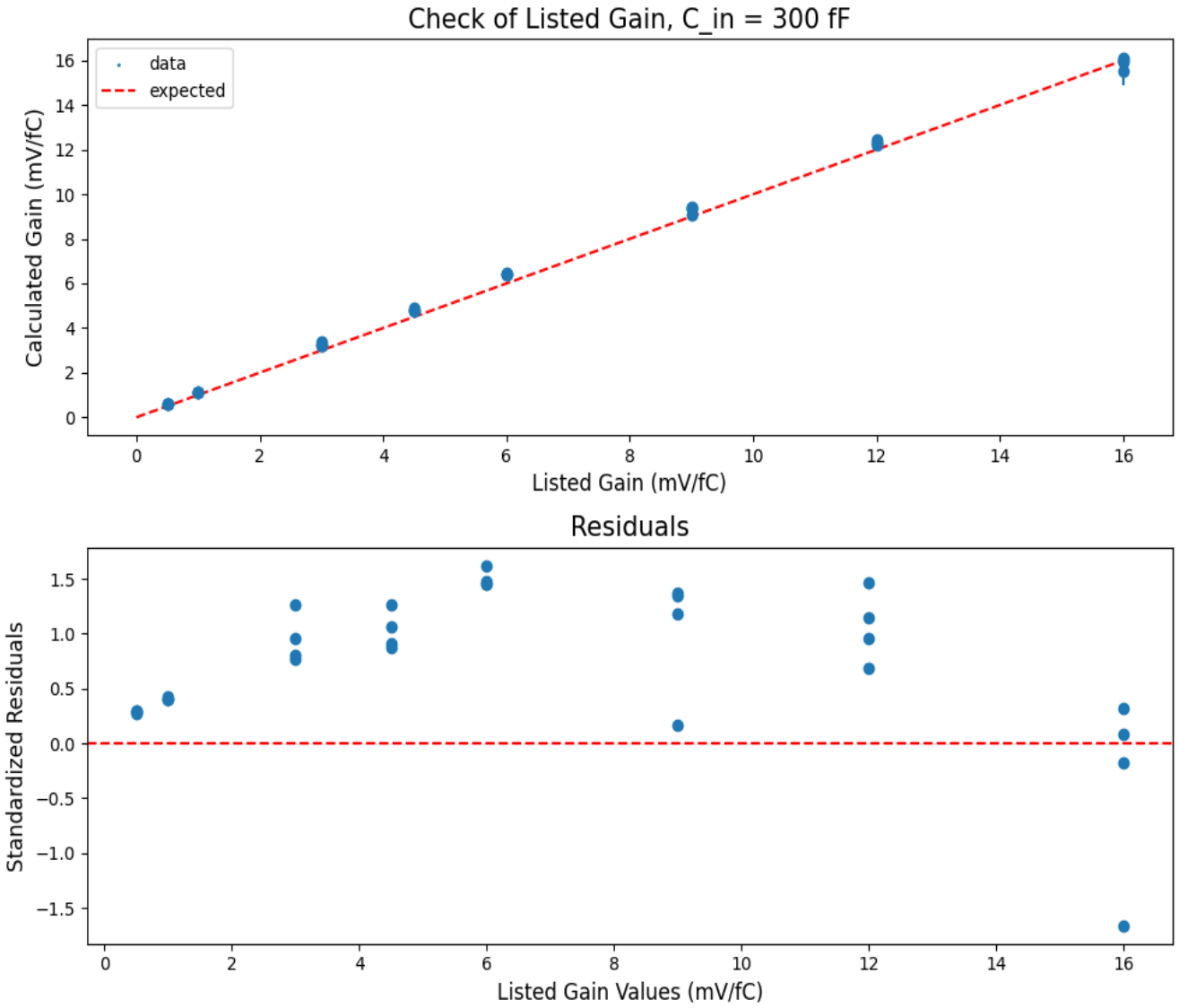
- Compared direct DAC output with shaped waveforms to test listed gain accuracy
- Adjustable C_{in} (300, 3000 fF)



$$V_{in} = 0.75 \frac{mV}{count} * DAC\ count$$

$$V_{out} = QG = (C_{in}V_{in})G$$

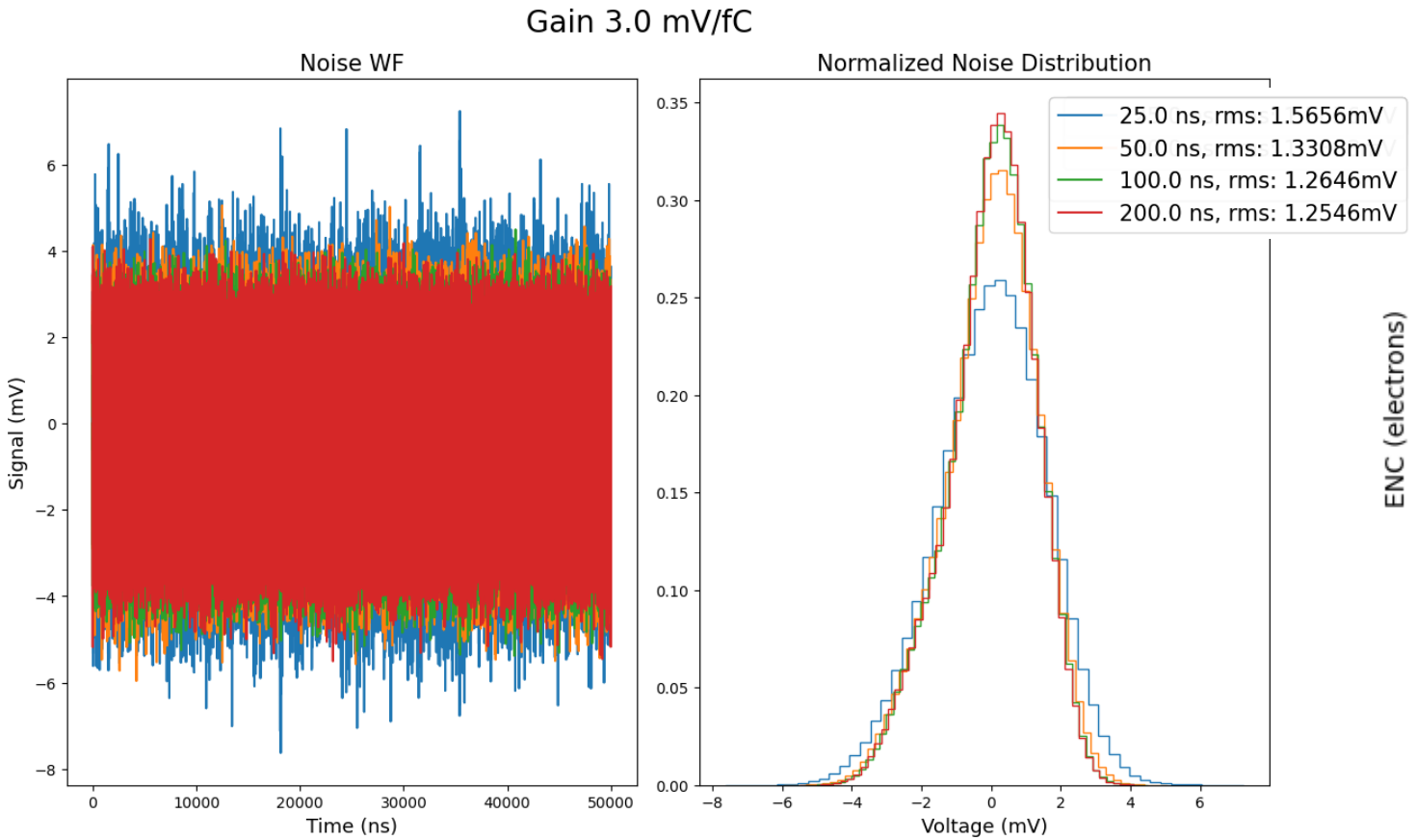
$$\rightarrow G = \frac{V_{out}}{C_{in}V_{in}}$$

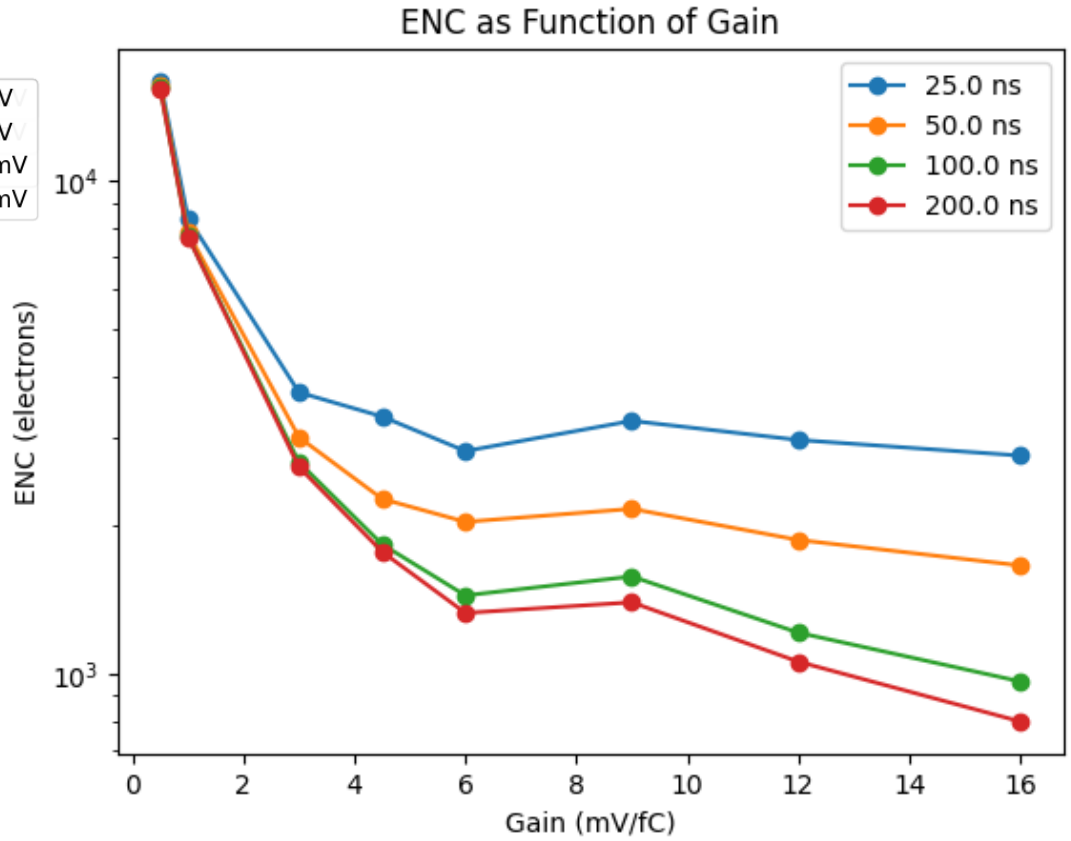


Characterization – Noise

- ENC Measurement via noise signal RMS
- Interested in relationship with Gain at different Peaking Times

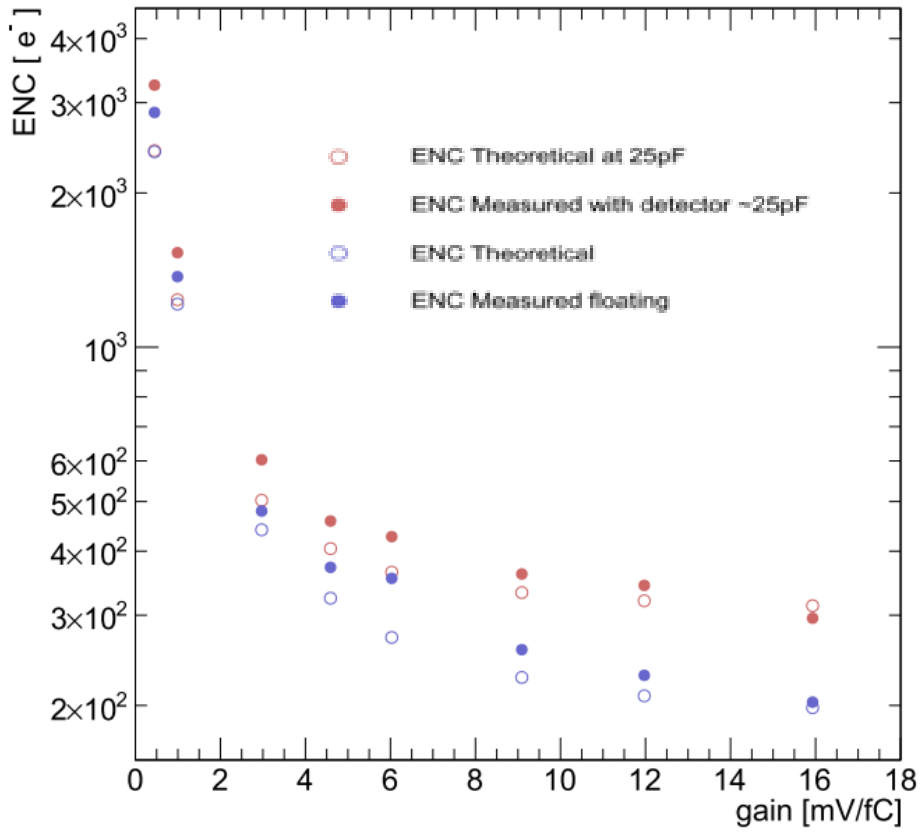
$$ENC = \frac{V_{rms}}{Gain}$$

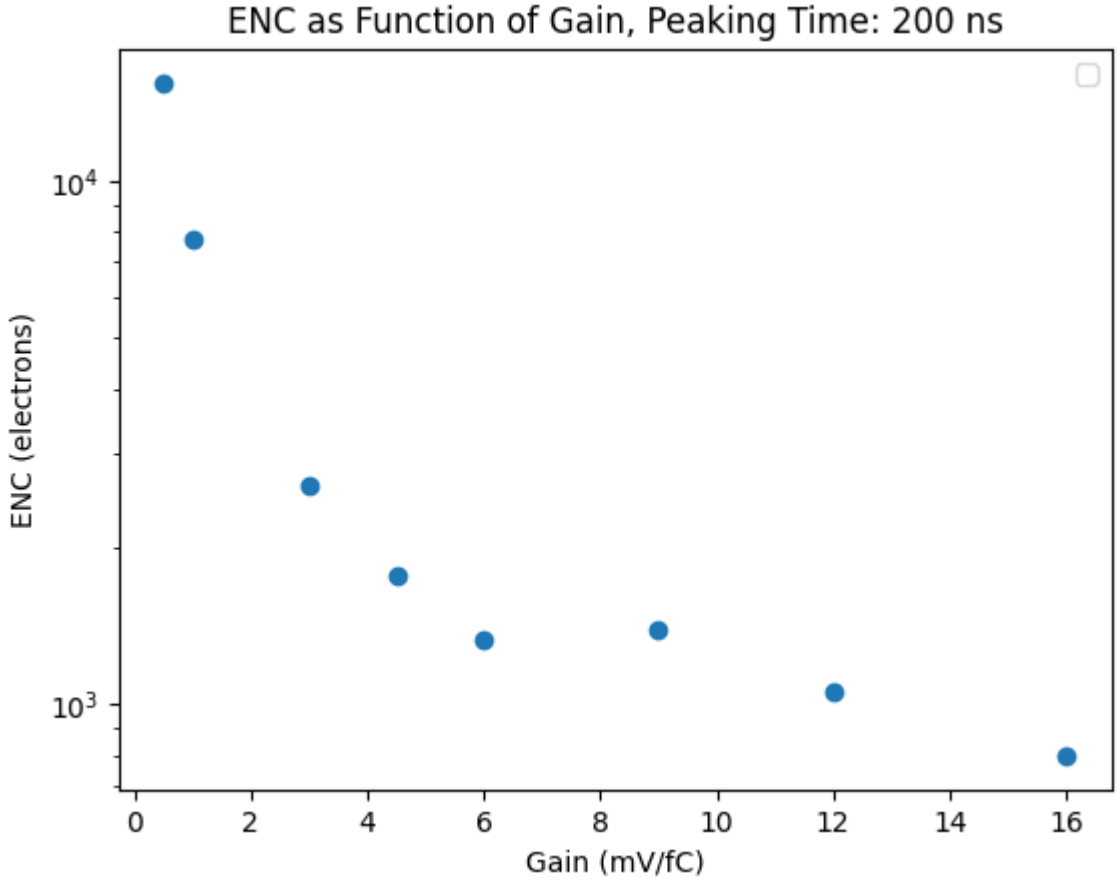




Characterization – Noise

- Disagreement with expected performance -> lowest noise observed ~750 electrons (gain 16)
- Attributed to:
  - Additional capacitances in this board vs ideal chip setup
  - Power/Grounding noise sources (George)





Key Takeaways

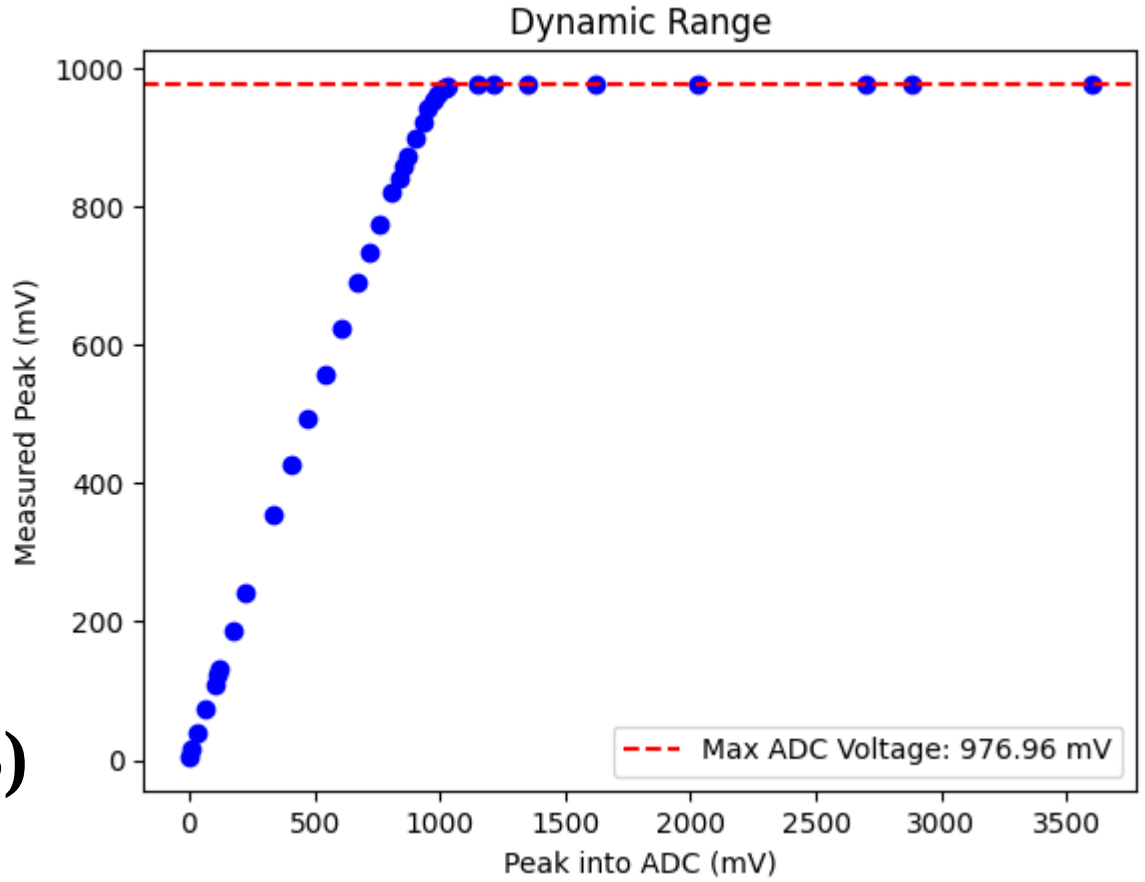
- Currently unable to demonstrate all listed performance levels
  - Need to understand ENC issue better
- Process provides framework for future electronics characterization
- Standardize the characterization of all (current and future) proposed electronics for ATAR
  - ENC relationship with configurable settings (Gain, Peaking Time)
  - Dynamic Range, Linearity, etc.
  - Accuracy of configurable settings

Backup

Characterization – Dynamic Range

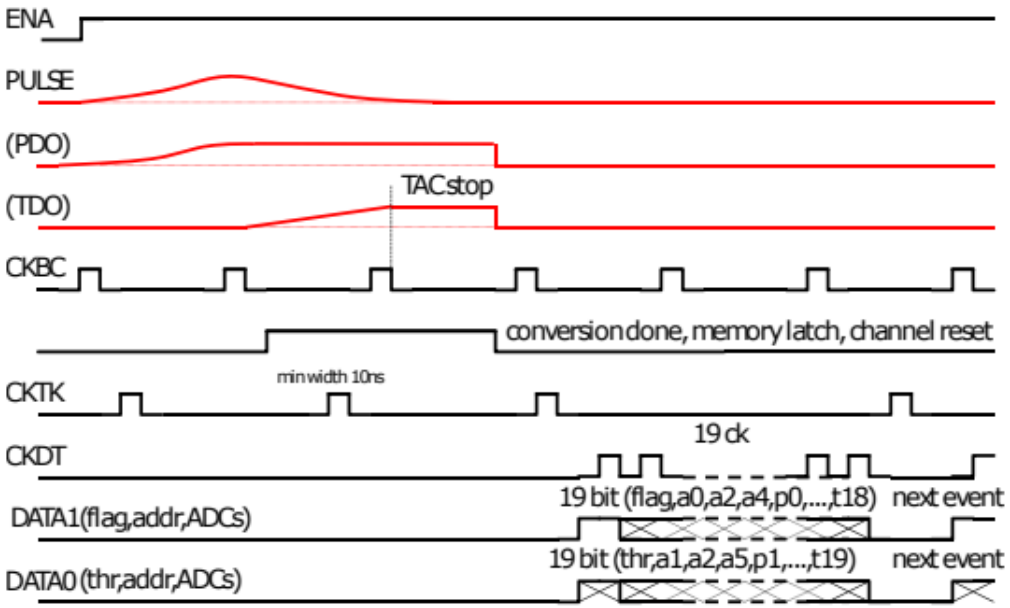
- Compared known input with measured output of ADC
- Maximum measurable signal ~977 mV

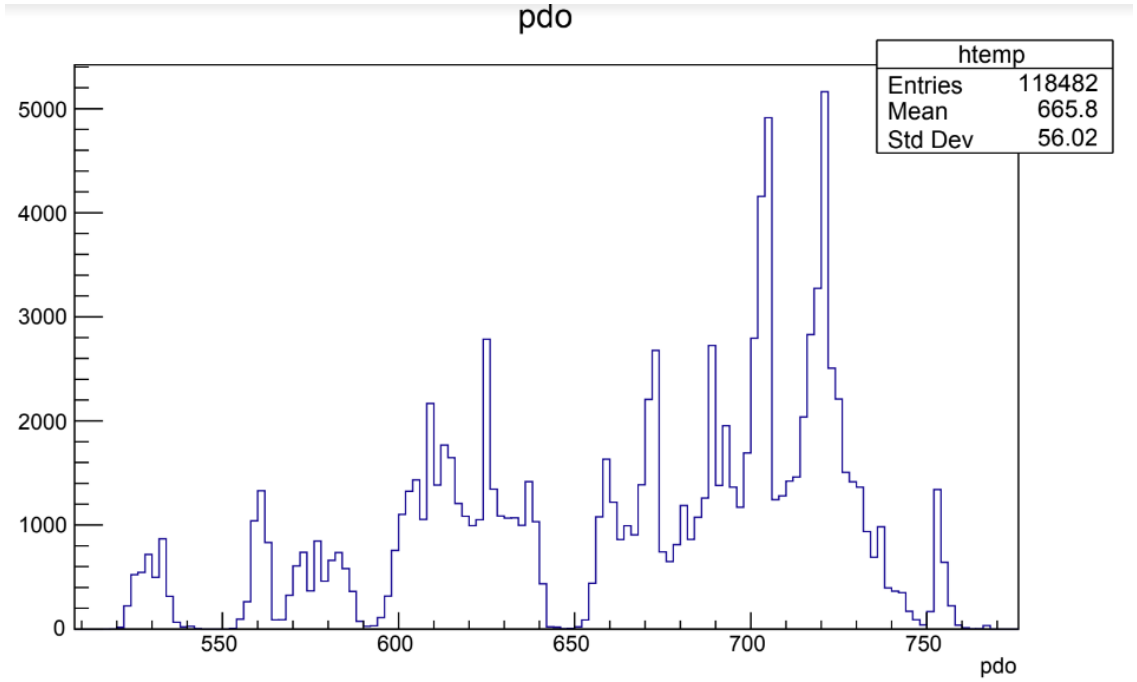
- Expected Dynamic Range ~180
  - ENOB: ~7.5 -> $2^{7.5}$
- **Measured Dynamic Range ~205 (46 dB)**

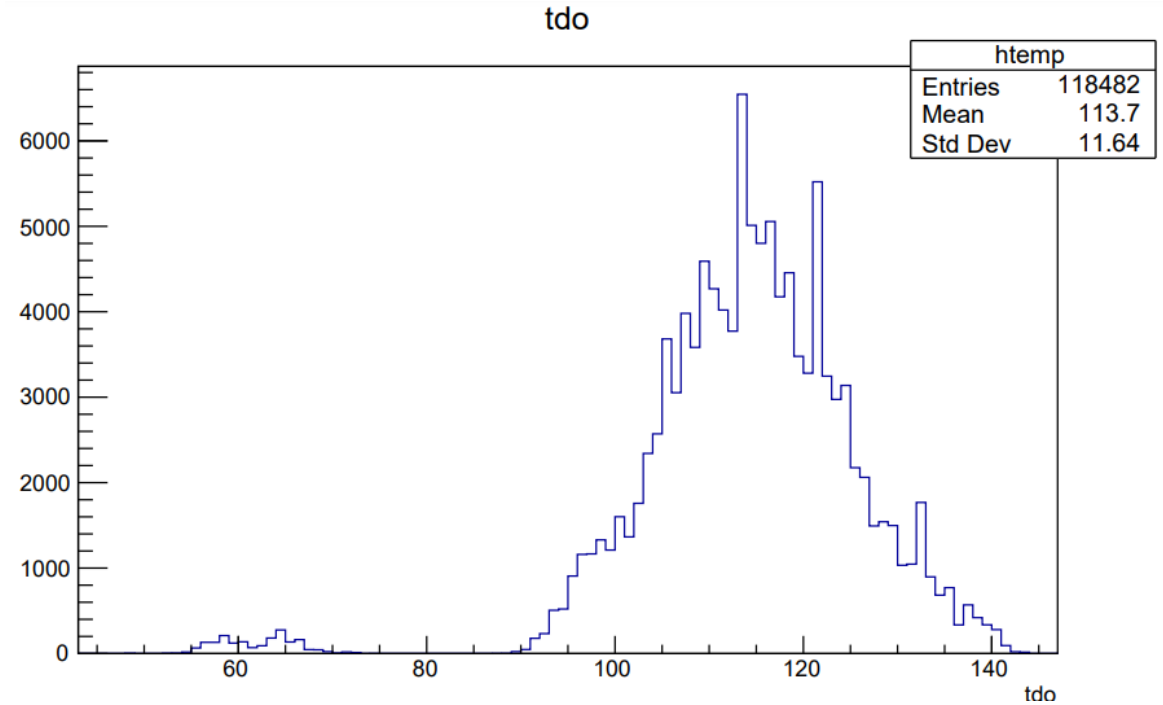


PDO & TDO

- PDO - Peak Detector Output
- TDO - Timing Detector Output
  - Time to Amplitude Converter (TAC)
  - Voltage ramp at threshold or peak and stops at cycle of Bunch Crossing Clock (CKBC)

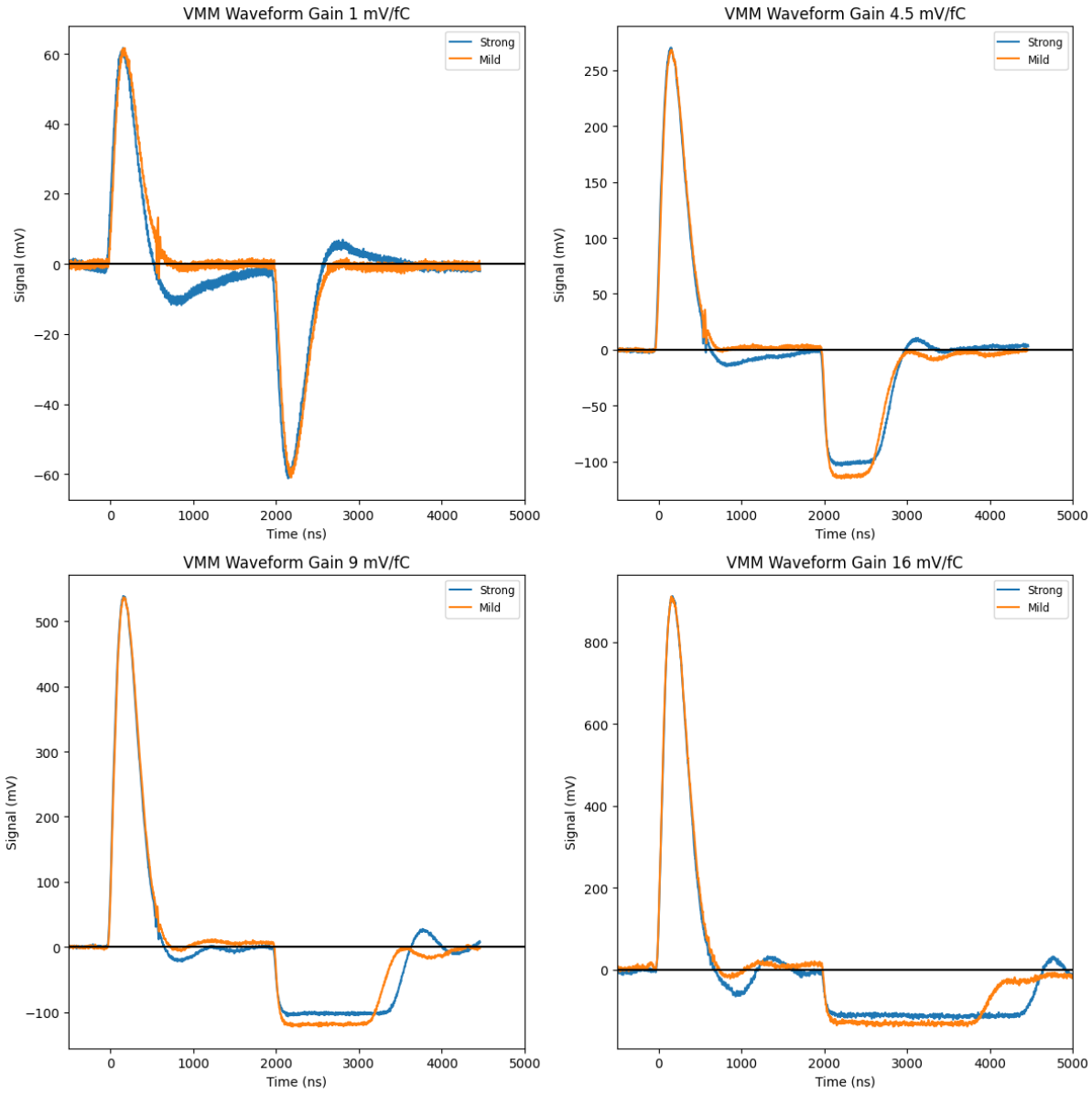






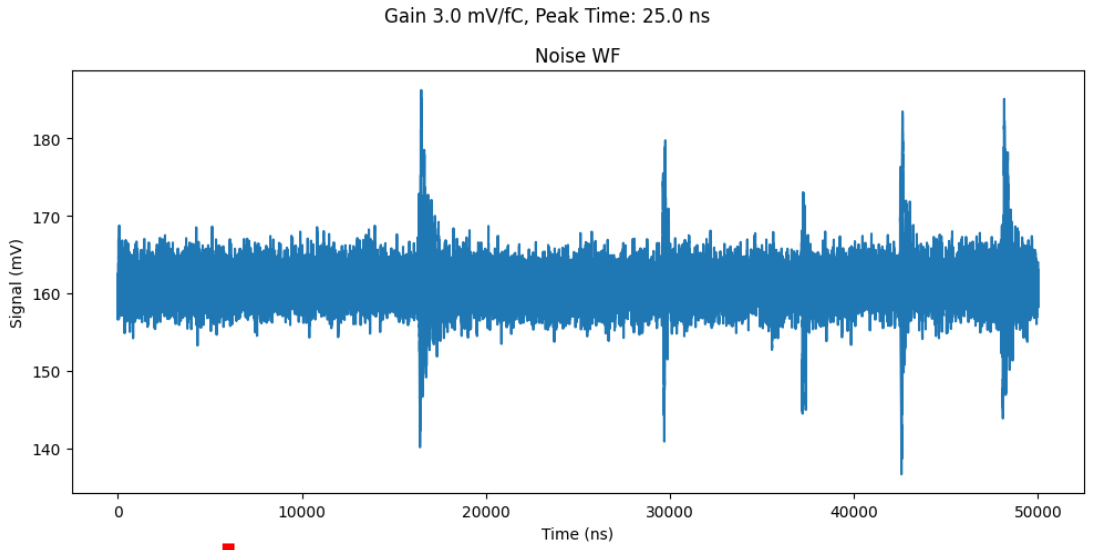
Characterization – Pulse Shaping

- Mild vs Strong Bipolar shape
- Configurable via global bits

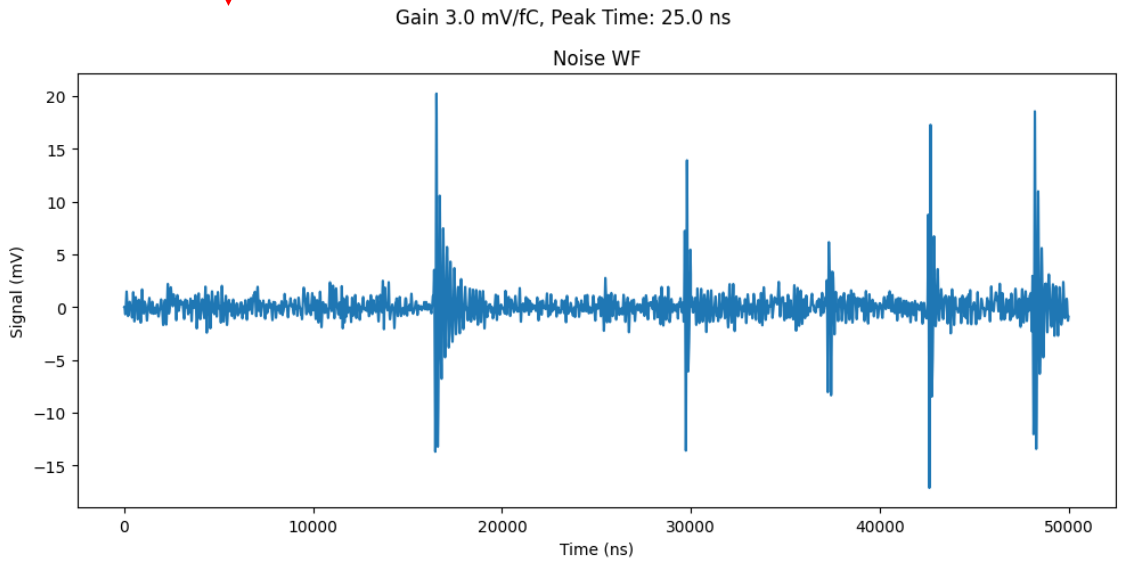


Noise Cleaning

- Noise waveform measurements via Wavepro 7000 scope
  - Sampling frequency: 5 GHz
  - 5000 ns measurement
- Noise waveforms obtained by moving scope selection to time stamps far after test pulser signal
  - Baseline removed for each signal (~160 mV)
  - Low pass filter applied (cutoff freq: $5e^6$ Hz)
- Concatenated numerous noise signals

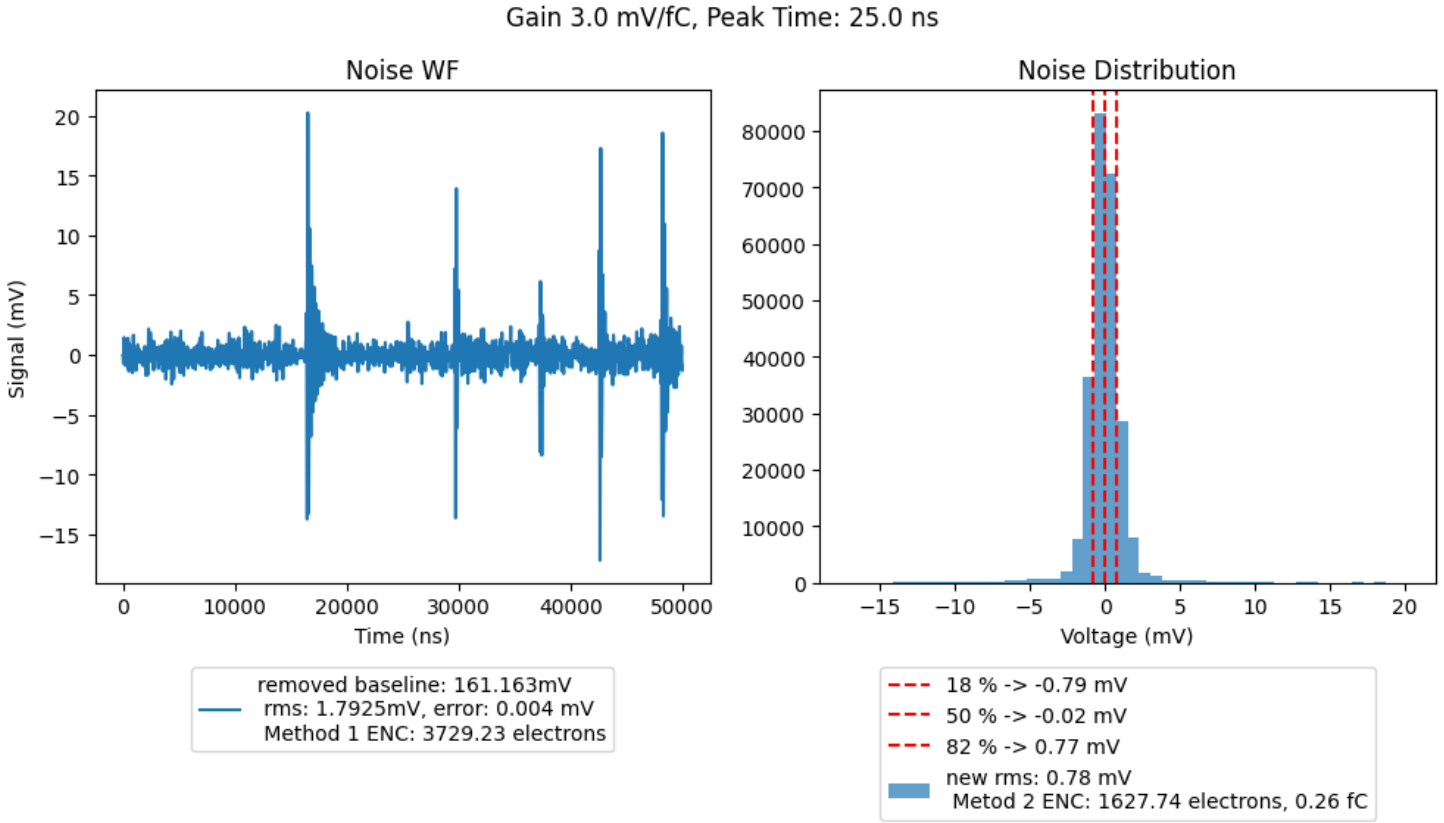


Appy filter and baseline removal



Calculating RMS voltage and ENC

- To calculate ENC we computed RMS of noise first and divided by gain (mV/fC)
- For RMS of voltage we used 2 methods
  - Initially just using normal RMS formula but large spikes (most likely external noise sources) skewed the result
  - Second method allows for removal of outlier voltages



Method 1: RMS formula

- Concatenate squared amplitude of signals and take square root of mean

$$V_{rms} = \sqrt{\frac{\sum_i^n v_i^2}{n}}$$

Method 2: Use 50+/-32% of voltage distribution

- a – 18 %
- b – 50 %
- c – 82%

$$V_{rms} = \sqrt{\frac{(b-a)^2 + (c-b)^2}{2}}$$

$$ENC = \frac{V_{rms}}{Gain}$$