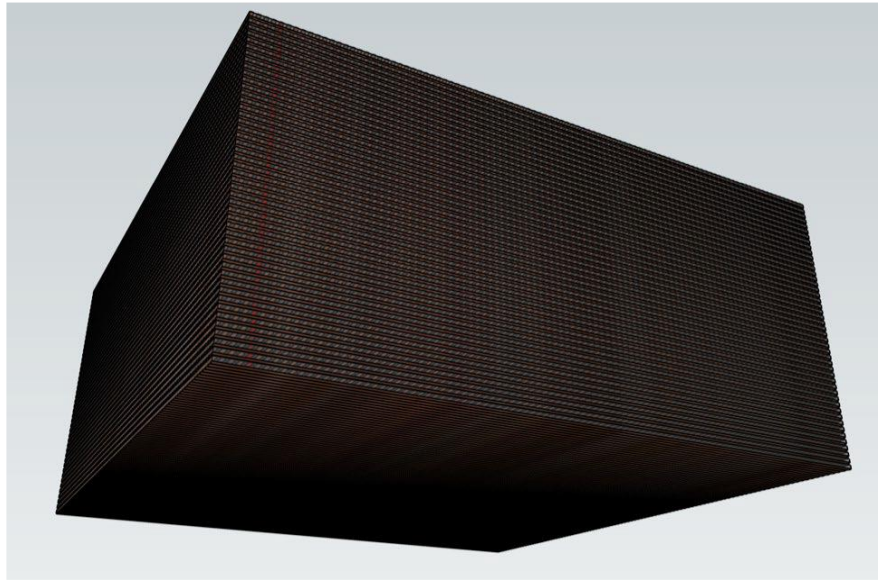
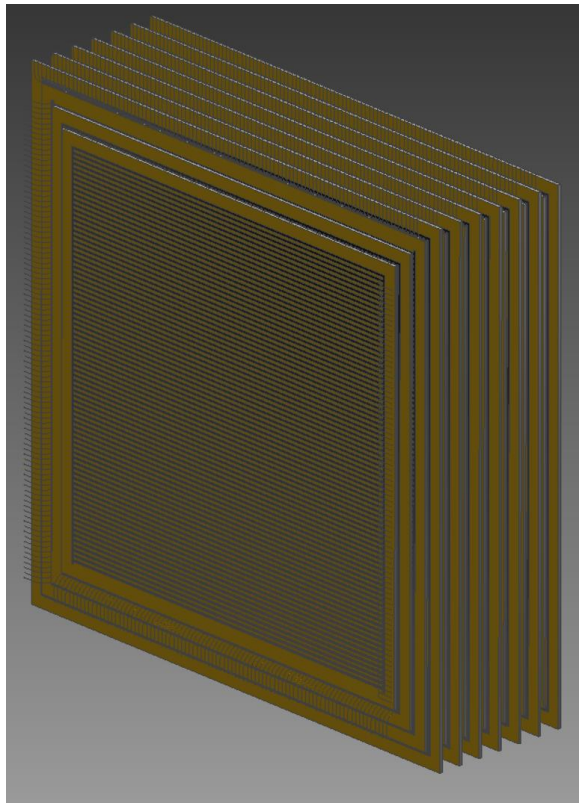
Evolution of Alternative ATAR Design

Xin Qian

BNL

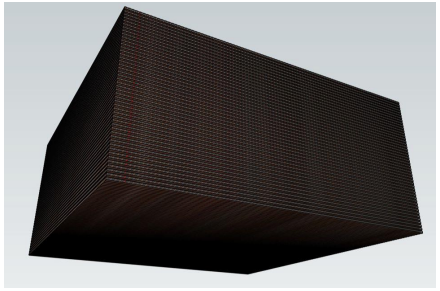




Comparison of Key Parameters

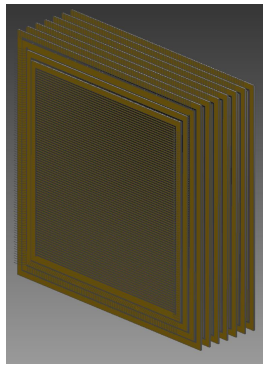
Previous Design

- 120 um layer thickness, 48 layers, 200 um strip pitch, 100 strips per face, **two-sided** X-Y readout
- **PIN technology**
- Separate readout → 9600 channels
- 6 ns shaping time electronics
- Distance between adjacent layers ~25 um
- Rectangular Geometry



New Design

- 120 um layer thickness, 48 layers, 200 um strip pitch, 100 strips per face, **two-sided** X-Y readout
- **PIN technology**
- Shared readout → 4900 channels
- ~20 ns shaping time electronics, cold electronics technology preferred
- Distance between adjacent layers ~ 2 um
- Pyramid Geometry



Considerations of Alternative ATAR Design

- Requirement of in-situ πεν tail measurements for all positron directions
  - Relax requirements on the dead materials that need to be minimized
- Acceptance of πμν and πεν both defined by ATAR only
  - Pion stopping point + positron direction (e.g. 5-hit)
- Trigger scheme of πεν events
  - Coincidence time and position, also energy (not dE/dx) cut based on topology to suppress πμν

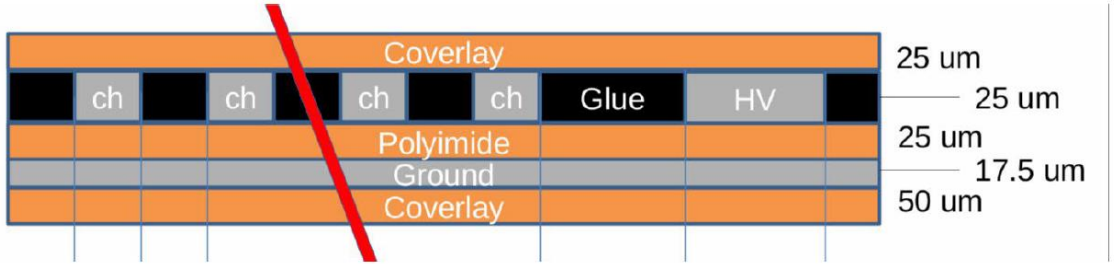
- < 100 um position resolution
- 2D position determination for each layer enabled by 2-sided readout → better dE/**dx**
- O(100) ps track timing resolution
- Good energy resolution to separate π vs. μ and (μ+e) vs. e through dE/dx
  - Suppress μDIF, πDIF, DAR for tail determination
  - No complication of gain
  - Aim for the lowest electronics noise > 9:1 (90:1) S/N for MIP (μ/π)
  - Also important for the trigger design

Detector Capacitance Estimation

Sensor from Gabriele Giacomini

200 um pitch, 100 um width	N-type strip (2 cm)	P-type strip (2 cm)
Interstrip capacitance	0.1 fF/um → 4 pF	0.04 fF/um → 1.6 pF
Back capacitance	0.08 fF/um → 3.2 pF	0.08 fF/um → 3.2 pF
FLEX cable	50-60 pF/m → 2.5 – 3 pF	
Total	~ 10 pF	~ 8 pF

FLEX cable from Simone



	3 cm	5 cm	7 cm
HV-CH (ground)	0.9	1.7	2.85
HV-CH (float)	4.2	6.4	9.1
CH-CH (ground)	0.7	1.2	1.8
CH-CH (float)	3.2	4.8	6.8
HV-ground	12	19.7	27
CH-ground	7	10.8	15.7

- Important for the electronics noise (S/N > 9:1 for MIP >~ 1.25 fC or 7800 electrons)
  - Viability of PIN vs. minimal gain of LGAG

$$ENC \propto C_{in} \cdot \sqrt{\frac{1}{t_{shaping}}}$$

Equivalent **N**oise **C**harge

- 6 e- /pF@ 1 us shaping @ room temperature
  - @ 20 pF, 20 ns shaping time gives us ENC 850 or > 9:1 for MIP w. PIN
  - At LXe temperature (~4 e/pF), ENC ~ 570 or >13:1 for MIP w. PIN
- **Low detector capacitance is preferred**
- **Cold electronics is preferred**

Considerations of (Electronics) Cross Talk

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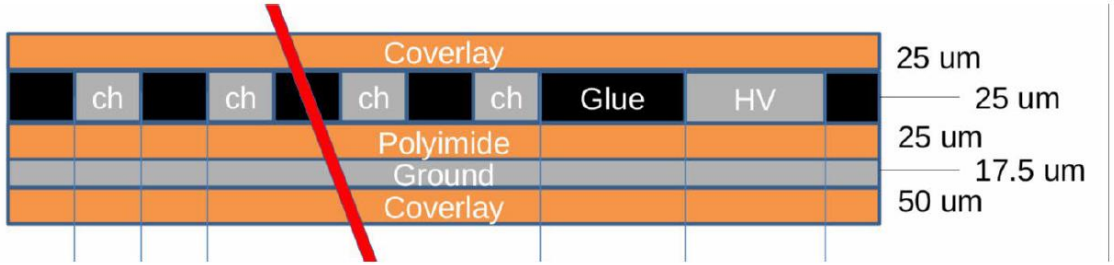

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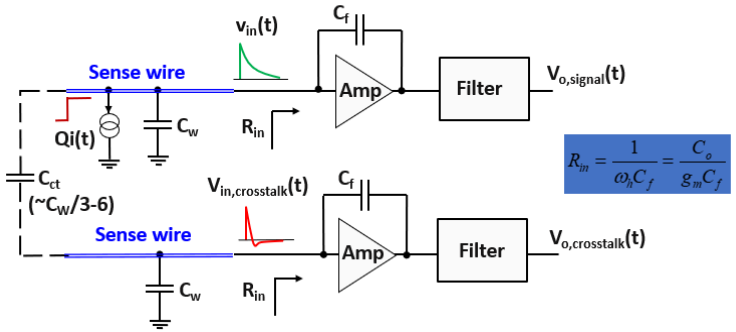
- Cross talk from the readout electronics

$$cross\ talk\ ratio \sim \frac{3}{2}\frac{C_{ct} \cdot R_{in}}{t_p}$$

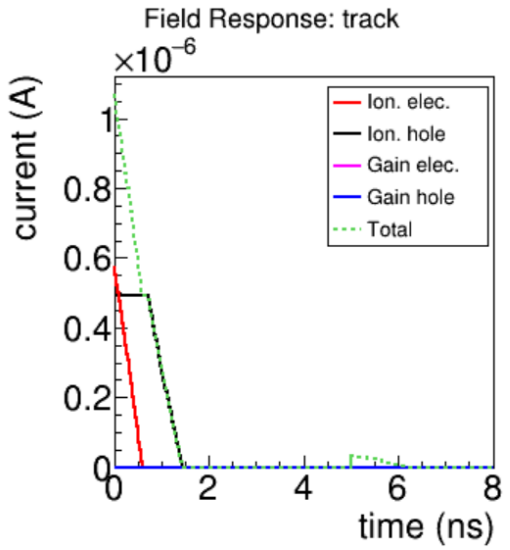
  - C_{ct}: coupling capacitance ~ 3 pF for adjacent chs
  - R_{in}: input inpedence ~ 40 Om
  - t_p: shaping time of electronics

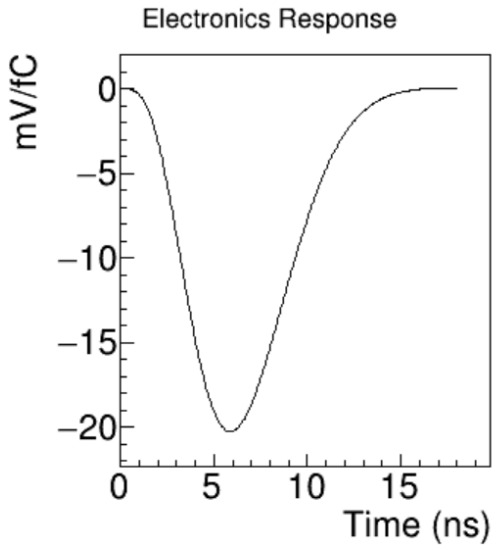


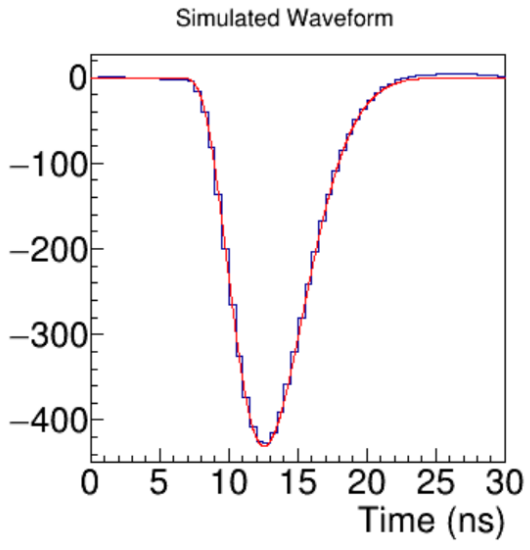
- @ 1 ns t_p, the cross talk will be ~ 20%
  - Also, potential coupling with channels far away
  - Significant effort in calibration is required
- @ 20 ns t_p, the cross talk will be ~1%

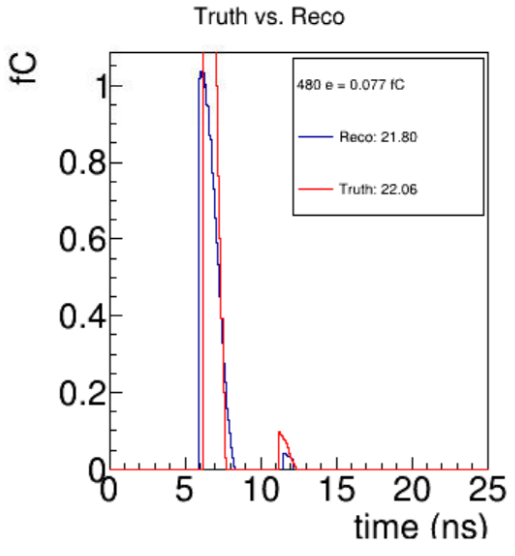
Impact of 20 ns Shaping Time

- Required by small electronics noise level for PIN and minimization of the electronics cross talk
- Difficulties in separating double hits, if time separation << 20 ns
- **Existing studies suggest that we can identify two hits with $t_{\pi\mu} > t_p$**
  - Tail fraction does not depend on $t_{\pi\mu}$!
  - Lower but still sufficient statistics for tail determination [20,78] ns → 41% of pion decays
    Pienu experience [5,35] ns → 56% of pion decays
    Need more than 2% overall efficiency after selection assuming 1% πεν tail fraction

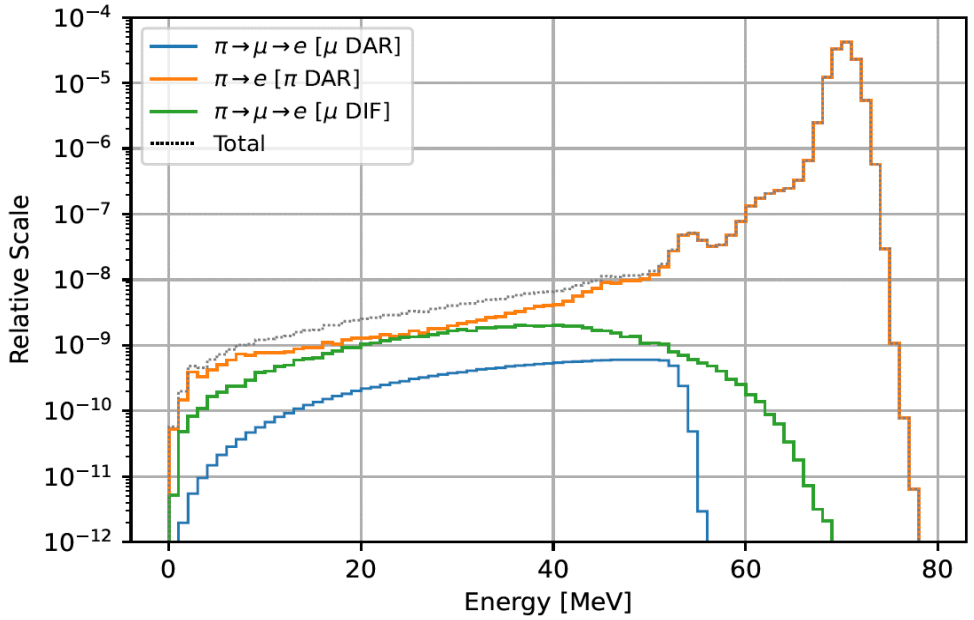








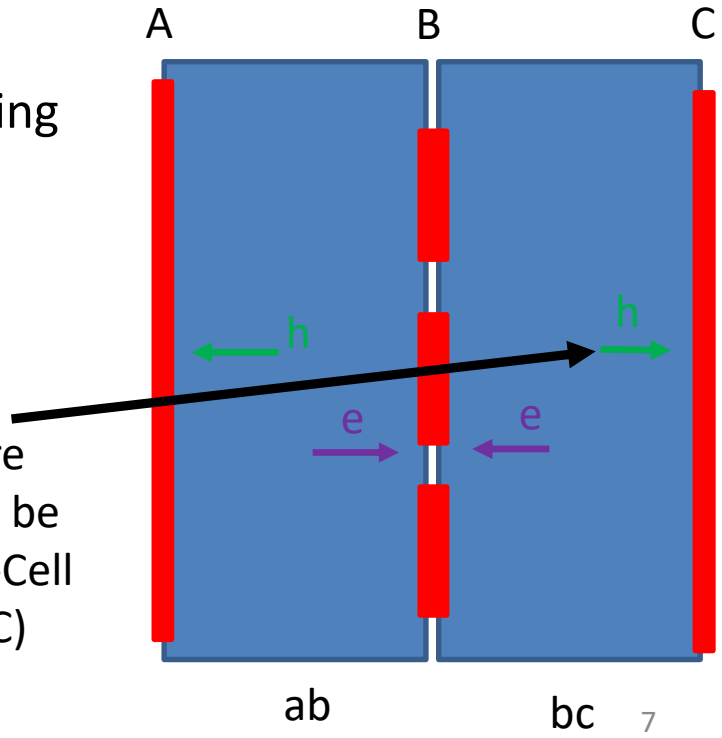
Considerations of Gaps between ATAR layers



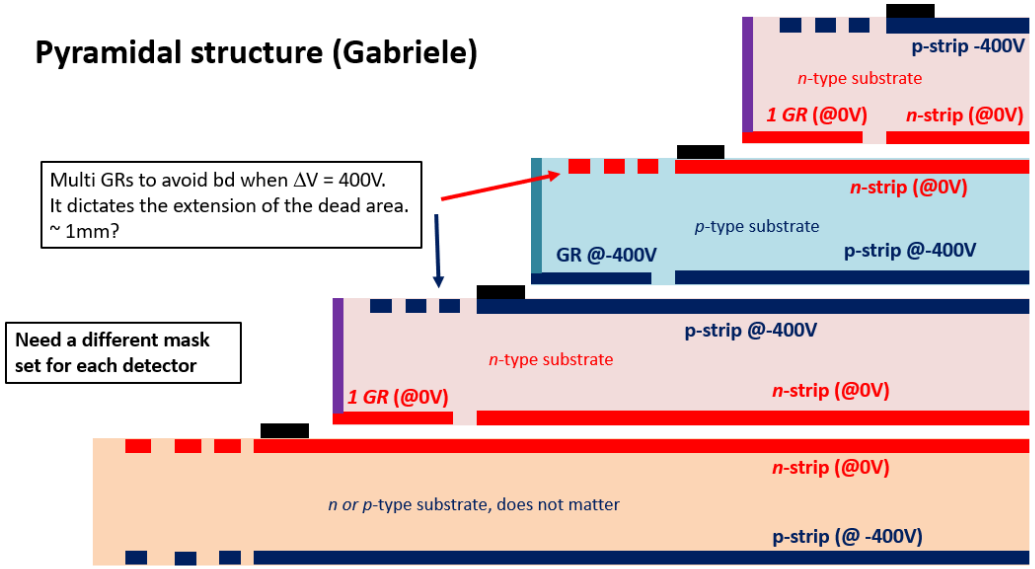
- Existing simulation assumes a very small ~ 1 um gap between adjacent ATAR layers
- Current reference design has 25 um gap
- Existing study suggests that gap would hurt the background rejection (x2-3 worse)
- Minimize the gap in ATAR design

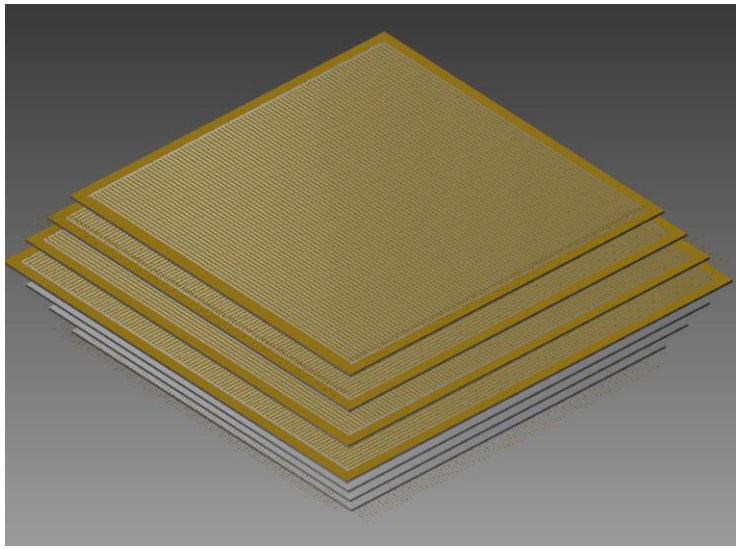
- Also, consideration of detector capacitance
  - For the original 2-sided readout (9600 channels), minimizing the gap between layers will lead to significant increase of the detector capacitance → PIN option is no longer viable
  - Shared readout concept (4900 channels)

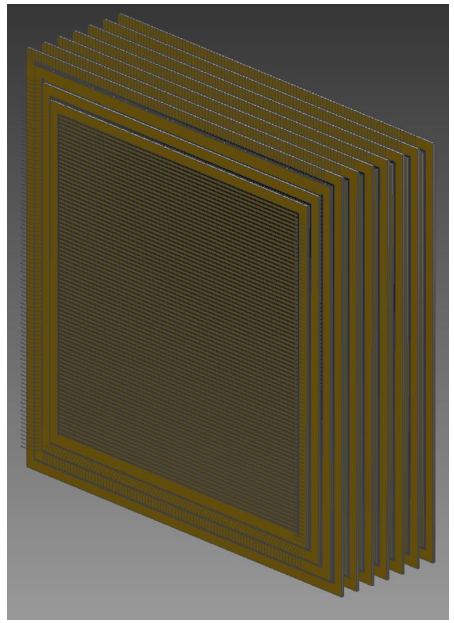
- We have the following signals
  - $A = ab + \ ...$
  - $B = ab + bc$
  - $C = bc$
  - All information are recorded and can be solved (e.g. Wire-Cell concept in LArTPC)

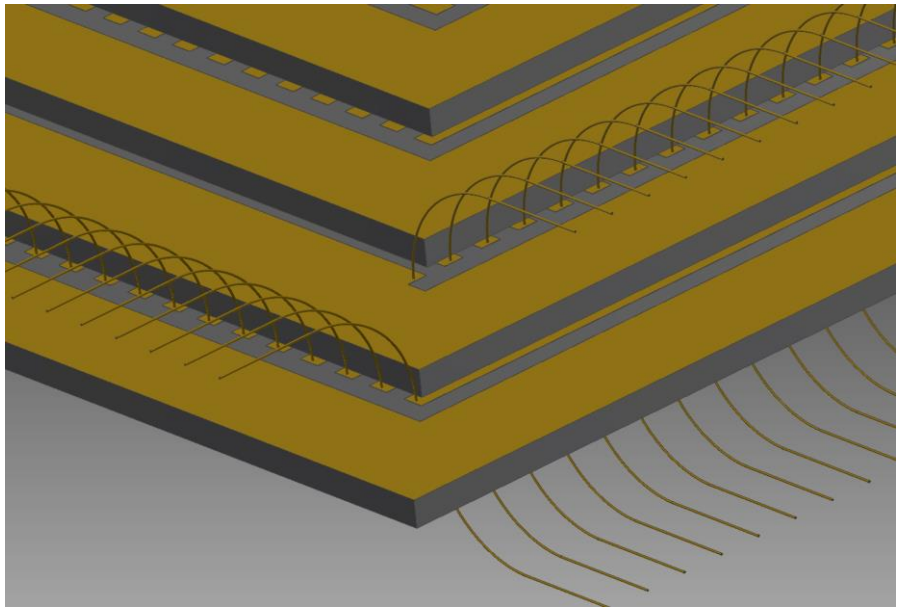


Consideration of Mechanical Structure

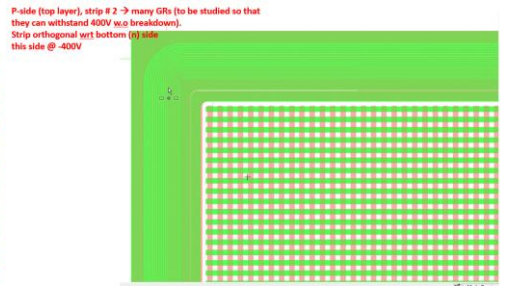


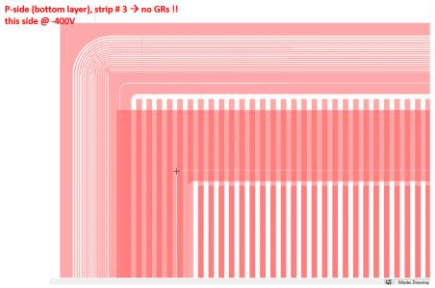






- Pyramidal structure is required
  - Guard rings that avoid breakdowns at the edge of sensor
  - Wire bonding for signal readout

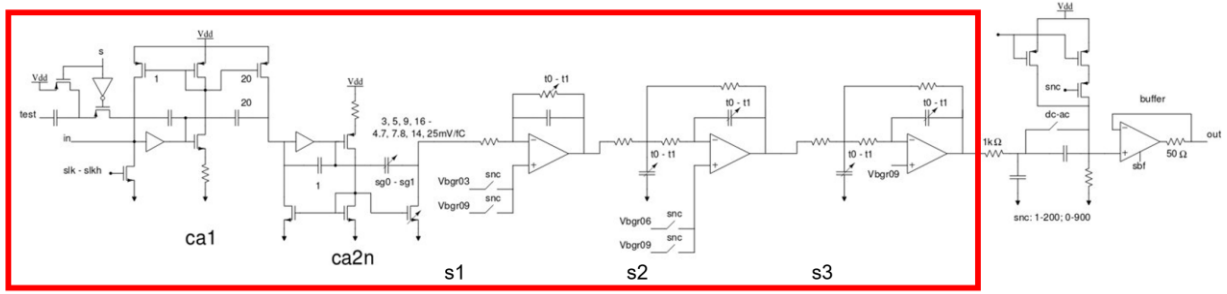




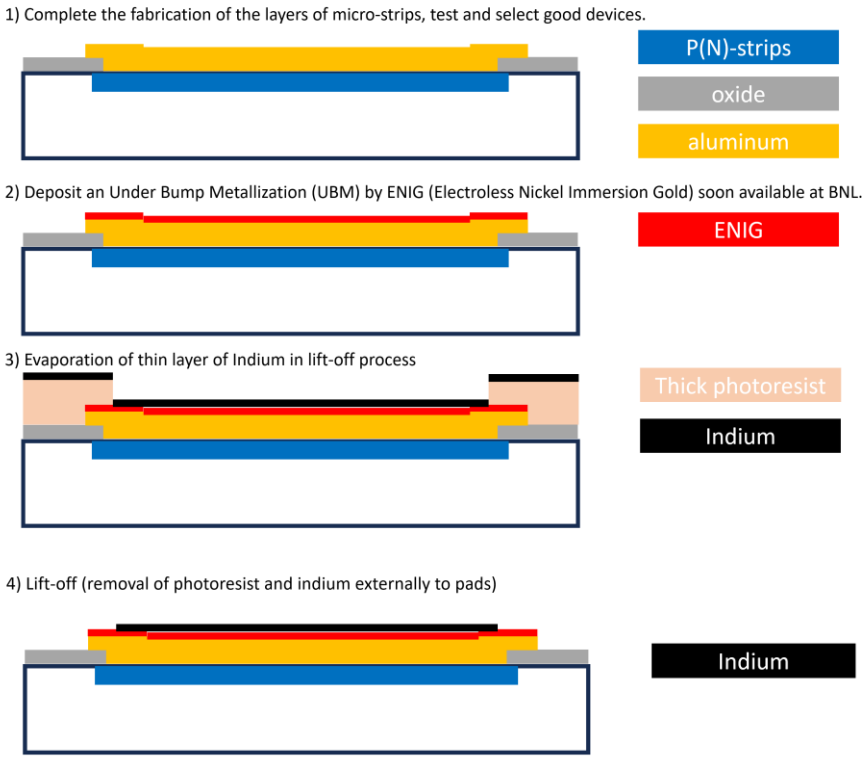
R&D Needed for the Alternative ATAR Design

Development of Electronics

- Modification of LArASIC for PIONEER
  - Redesign LArASIC from 180-nm to 65-nm technology is in progress
    - Minimal shaping time 500 ns
    - Dynamic range & linearity over 12-bits
    - Optimized for 200 pF det. capacitance ENC ~ 600
  - Modification of shaper circuit can satisfy the need of PIONEER (~ 20 ns)
  - Preamp part does not meet the need though
  - **Modification of preamp is needed, but no showstopper observed**



Mechanical Structure (Concept)



From Gabriele

Also input from Aleksey

Key is to minimize the gap between the adjacent layers ~ 2 um

Expected Milestones of Physics Performance of Alternative Design

- Requirement of in-situ πev tail measurements for all positron directions
  - Relax requirements on the dead materials that need to be minimized
- Acceptance of πμν and πev both defined by ATAR only
  - Pion stopping point + positron direction (e.g. 5-hit)
- Trigger scheme of πev events
  - Coincidence time and position, also energy (not dE/dx) cut based on topology to suppress πμν

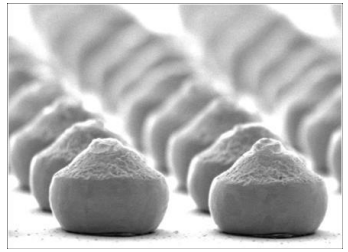
- Demonstrate the in-situ tail fraction measurement with the current design parameters
  - Iteration with variations on design parameters
- Demonstrate the acceptance difference between πμν and πev using ATAR only
- Provide guidance and requirements on the Trigger Scheme

Interconnecting Si strip detectors

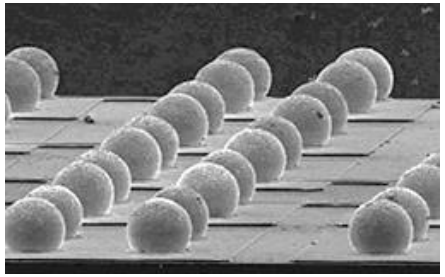
From Aleksey

- A variety of flip-chip techniques can be used
- Interconnecting large area strips seems like a simple task – we need to find a suitable technic and tune the process
  - How it works: Small bumps, balls, or solder preforms are deposited on metalized strips of the first die
  - The second die is inverted to bring the solder bumps down onto strips of the first die
  - Solder is re-melted to produce bonding, typically using a thermosonic bonding or alternatively reflow solder process, T < 300 C
  - Just a few bonds will be enough, e.g., to bond a 1x1 cm2 SiPM for nEXO we use 6 50-micron bumps
- An important question is about gaps between the dies
- Test for thermal expansion

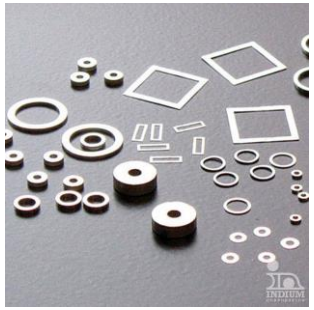
Bumps



Solder balls



Solder preforms



Bonding materials:
- Solder – use fluxless solder, potential diffusion in Si
- Conductive epoxy – potential contamination of LAr

Done Pinelli (pinelli@bnl.gov) is an expert in bonding and interconnection at Instrumentation James Clayton President & CEO at Polymer Assembly Technology, Inc.

1) Complete the fabrication of the layers of micro-strips, test and select good devices.

P(N)-strips

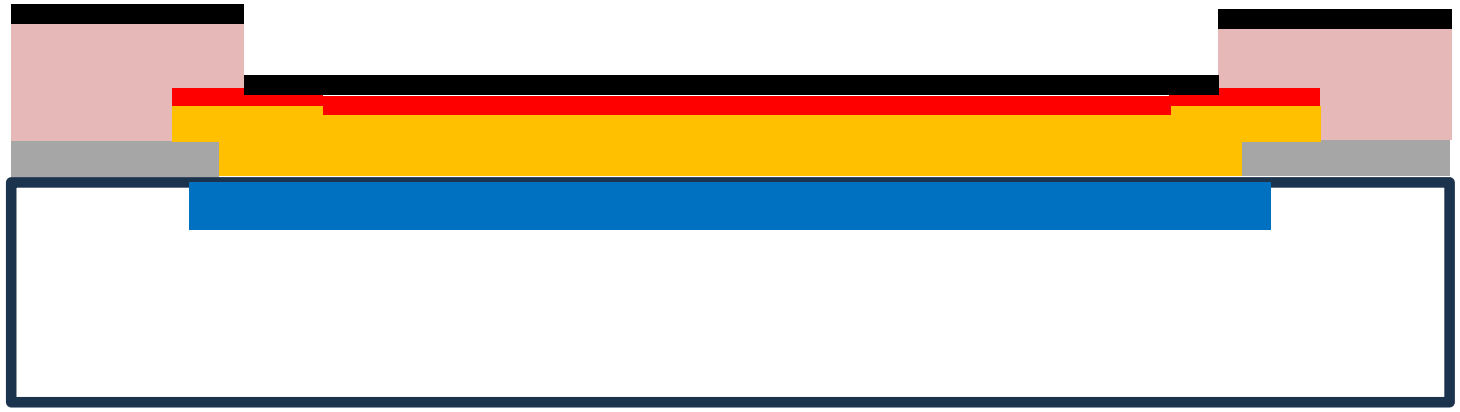
oxide

aluminum

2) Deposit an Under Bump Metallization (UBM) by ENIG (Electroless Nickel Immersion Gold) soon available at BNL.

ENIG

3) Evaporation of thin layer of Indium in lift-off process



Thick photoresist

Indium

4) Lift-off (removal of photoresist and indium externally to pads)

Indium

5) Flip-chip and connection of two strip layers together