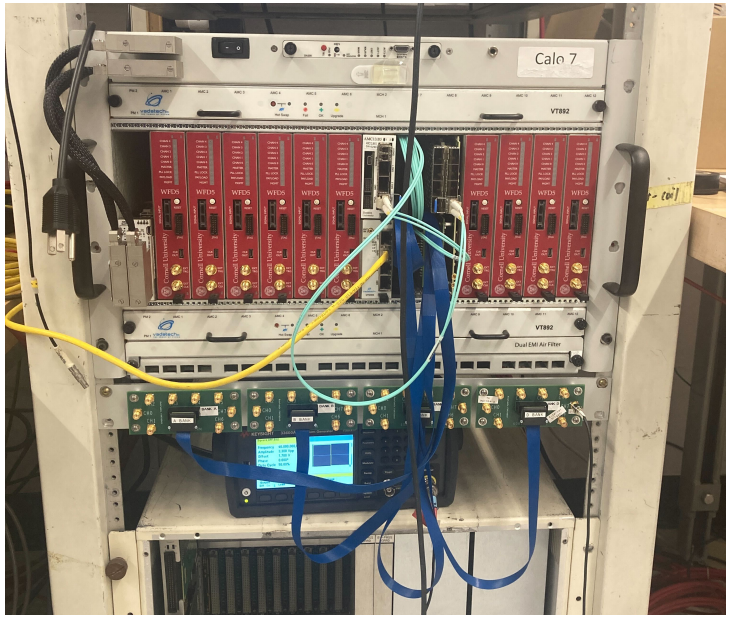
Brief tour of theTestbeam DAQ hardware

Lawrence Gibbons

Platforms: build on CMS



UW uTCA crate

microTCA (μTCA) crate w/ star topology

- backplane provides:
  - ethernet access
  - clock
  - TTC protocol
  - parallel 5 Gb/s readout
- μTCA Carrier Hub (MCH) provides (our use)
  - 1 Gb ethernet switch to backplane
  - IPMI for remote control and monitoring of crate

CERN Timing, Trigger and control (TTC) protocol (https://ttc.web.cern.ch/)

- basic 40 MHz frequency
- two-channel biphase encoding @ 160 MHz
  - Channel A: trigger distribution
  - Channel B: synchronous commands
    - g-2 used to specify “trigger type” of next trigger

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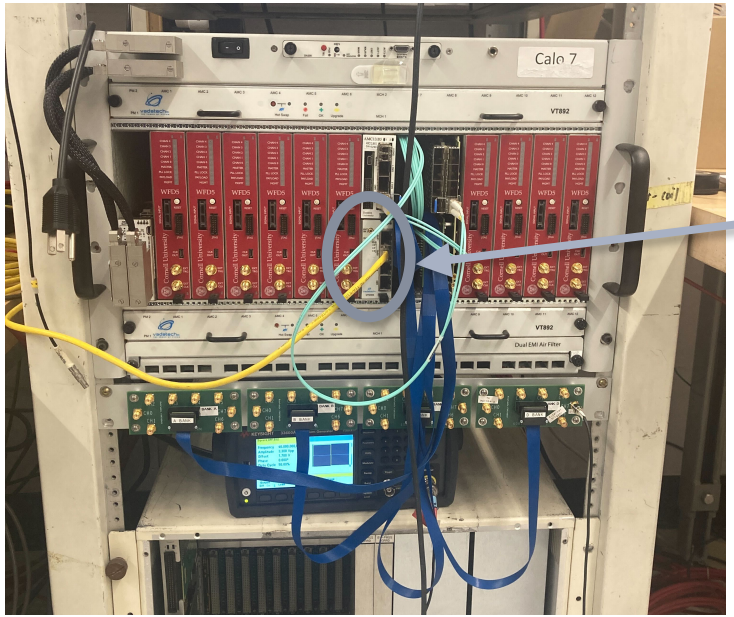

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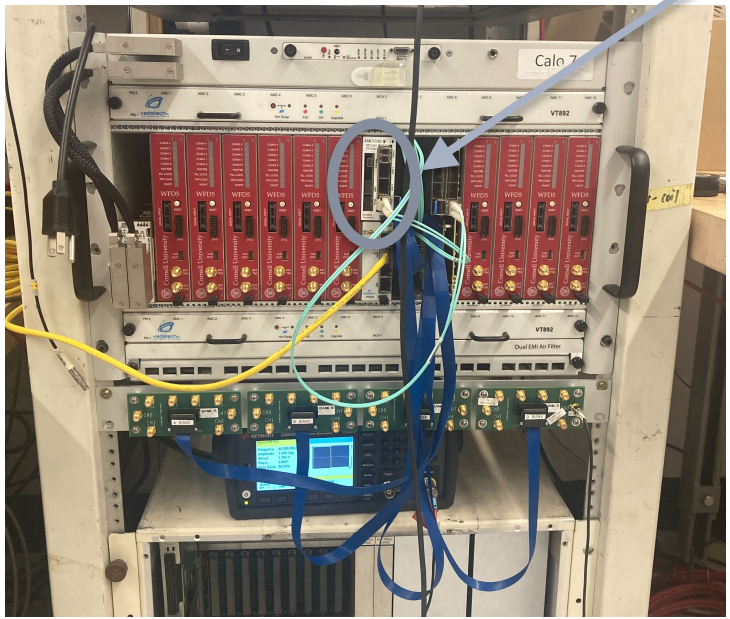
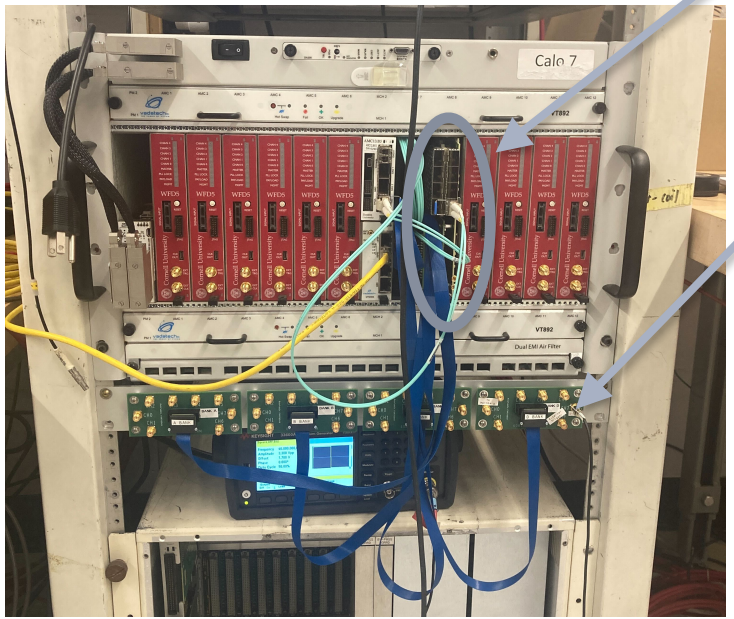


UW uTCA crate

BU “AMC13” (http://amc13.info)

- recovers clock from TTC signal
- distributes clock, trigger, TTC over backplane to all “Advanced Mezzanine Cards” (AMCs) in crate
- asynchronously reads data for each trigger over 5 Gb/s backplane lines
- local even building
- data → midas frontend server via 10 Gb ethernet
  - up to 3 links available — we use 1 link

Platforms: build on CMS

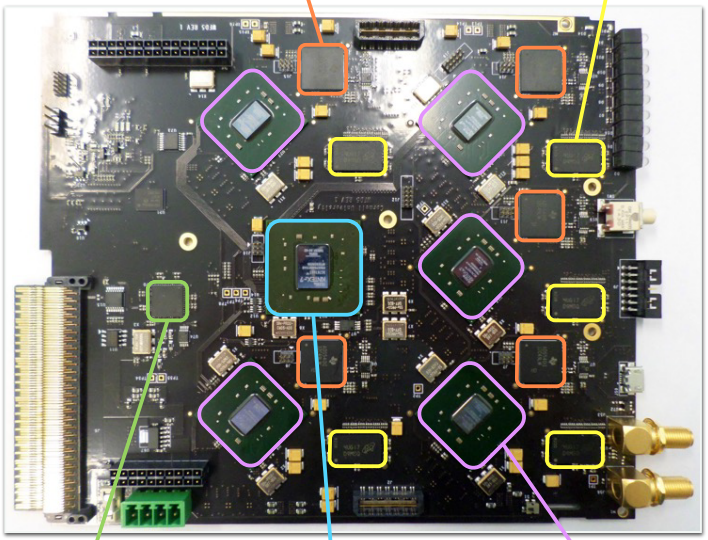


UW uTCA crate

Encoder FC7

- encodes TTC protocol using
  - input precision 40 MHz clock
  - input external trigger
  - user-specified TTC trigger pattern
    - current firmware: up to 4 TTC triggers with specification of
      - » “type”
      - » delay
      - » width
- distributes optical TTC to AMC13 in up to 8 μTCA crates
  - additional crates supported using “fanout FC7s” — 16 per module
- distributes 4 analog copies of TTC
- can distribute up to 24 analog triggers based on input trigger
  - delay and width configurable

WFD5 digitizer AMCs

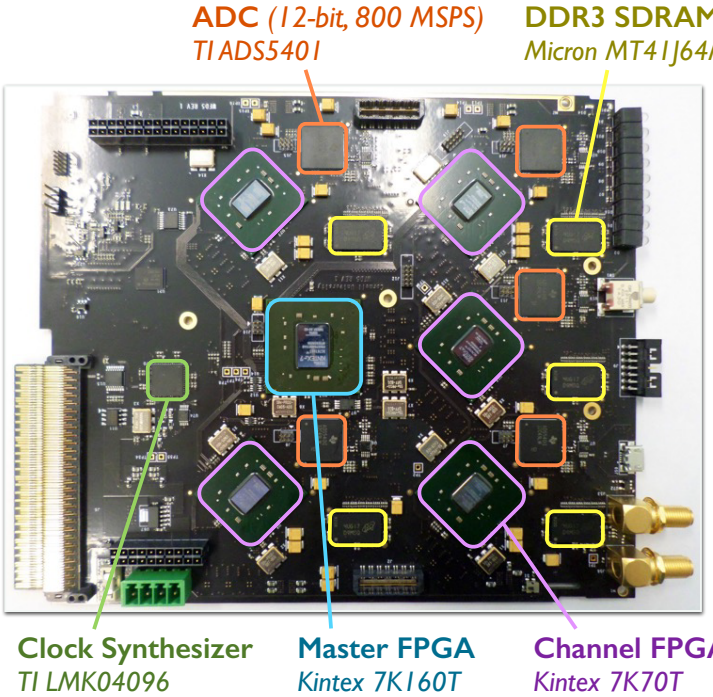


Main WFD5 board — power supply and analog front end mezzanines removed

5 channel digitizer

- based on TI ADS5401 ADC chip
  - up to 800 MSPS via 2 on-die interleaved 400 MSPS channels
    - common clocking → stable 180° phase difference
    - but, odd/even sample pedestal difference
- dedicated FPGA and DDR3 buffering (64 MSamples) on each channel
- Currently 3 modes of operation
  - TTC-triggered circular buffer (suggested mode for pioneer testbeam work) NEW
    - Via ODB, specify
      - » # samples total
      - » # samples preceding TTC trigger arrival
    - Buffers 128 Samples ⟷ 160 μsec @ 800 MSPS
  - TTC-triggered acquisition pattern (main g-2 mode)
    - can enable up to 3 patterns ← TTC trigger type
    - configurable via ODB
    - no sample buffering
  - Circular buffer via front panel trigger
- Current analog front end mezzanine card
  - DC coupled differential signal (100 Ω impedance)
    - 1 V peak-to-peak maximum (ADC chip constraint)
    - 1.9 V common mode
  - ODB-configurable voltage offsets: use full ADC range w/ single-sided pulses

WFD5 digitizer AMCs



Main WFD5 board — power supply and analog front end mezzanines removed

5 channel digitizer

- On-board clock synthesizer
  - up-converts 40 MHz TTC master clock from backplane
    - settings for 200, 300, 400, 600, 800 MHz in hand (specify via ODB)
- timing resolution(s):
  - sampling phase alignment across ADC chips (and WFD5 modules) not implemented
    - not the plan for pioneer digitizers!
  - g-2 template fits: timing jitter in WFD5 contributes < 20 ps to timing resolution
    - much smaller for timing comparisons within single WFD5
  - but beware: jitter on master 40 MHz distribution to AMC13
    - uTCA crates could differ by ±25 ns (one period) on timing of external trigger (in g-2 based on independent FNAL clock)
    - no jitter: timing stable after AMC13s lock on clock
    - g-2: simultaneous laser flash of all crystals resolves such issues automatically

Questions about system?

- I’ll be posting documentation within the pioneer software/firmware GitHub repositories
- and / or please contact me…