DAQ and triggering electronics for PIONEER

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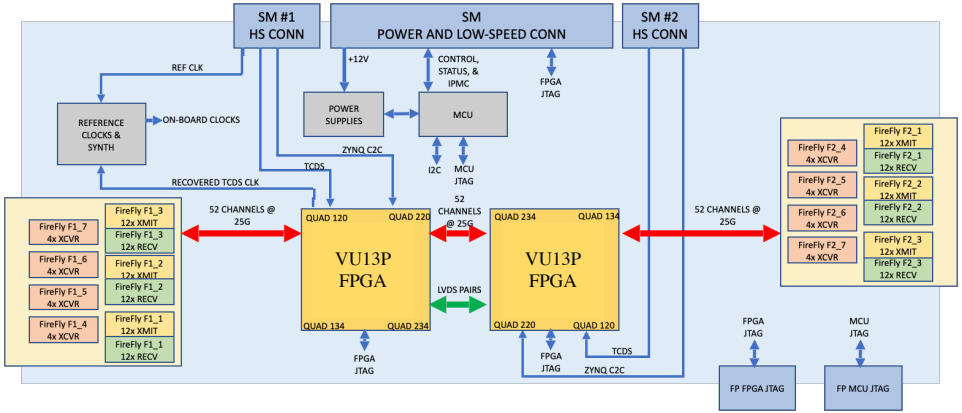
Electronics “backbone” for DAQ / triggering (reminder)

- The system should
  - handle a large number of inputs to the triggering
    - 300 - 1000 calo channels
    - 1000’s of bits from ATAR hit topology
    - …
  - be flexible
  - have low latency for trigger decisions – O(few 100 ns)



- CU/CMS APOLLO Command Module a good match
  - 104 Samtec Firefly serial I/O lines
    - 64 bits @ ~250 MHz / channel
    - optical option → DAQ / detector isolation
  - lots of logic / processing power
  - HL-LHC lifetime (support related)

Command Module (CM) Status

PIONEER's 2 XCVU13P-2 FPGAs awaiting production run

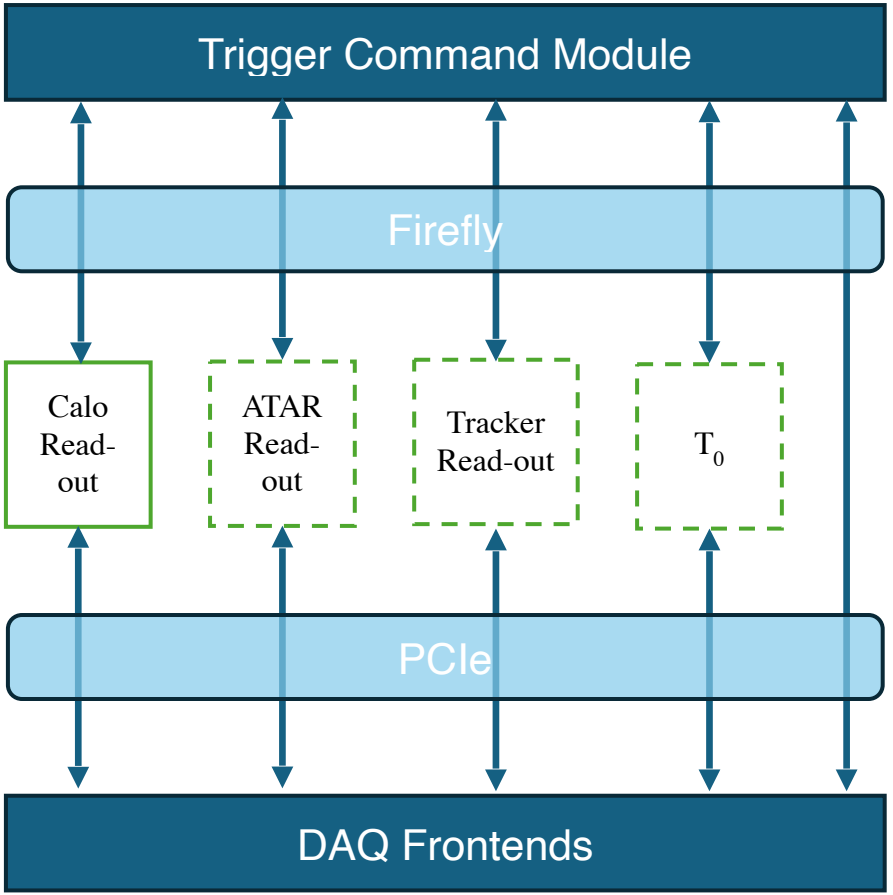
Pre-production board

- Small production order expected this summer
  - 1 CM for PIONEER
- Developer (P. Wittich) now shares my lab!
  - 1-FPGA pre-production board available for development

Proposed protocols

- Communication to PCs: PCIe
  - configuration: IPBus over PCIe
    - excellent experience with original IPBus over ethernet in g-2
- Pipelined trigger information → trigger CM: AXI4 over Firefly
  - industry standard FPGA ↔ FPGA communication
- Real time command / control / monitoring: ??
  - a group to evaluate needs & implement would be welcome!

PCIe over Firefly card in hand



12-Channel calo digitizers

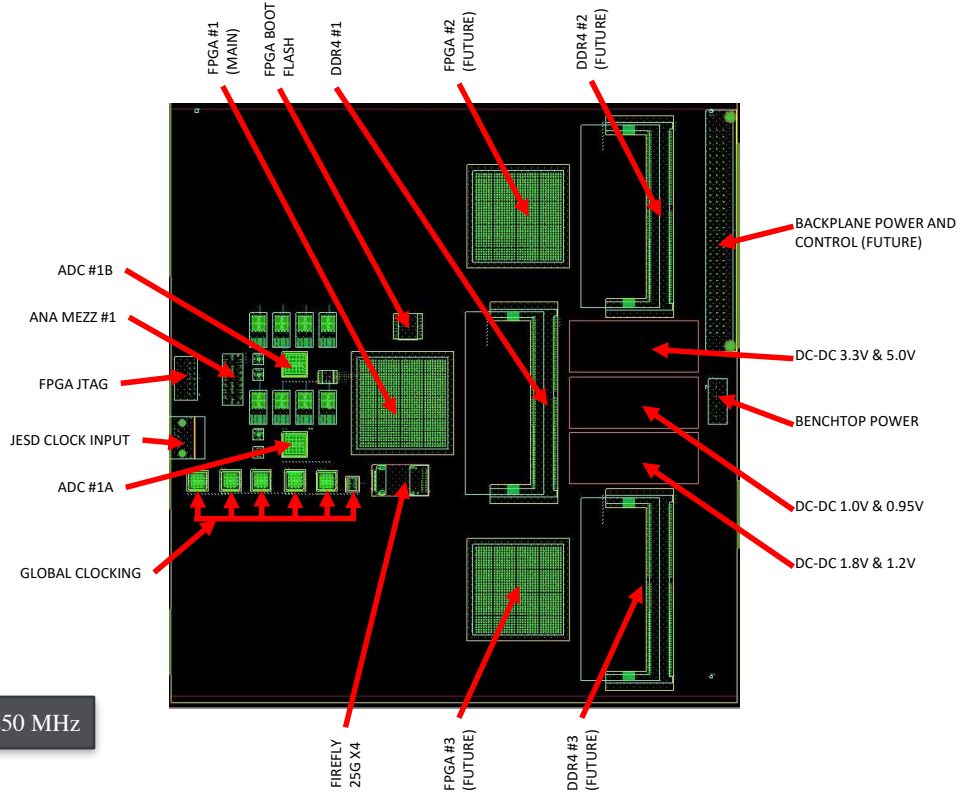
- ADC: dual-channel 12-bit 1 GSPS AD9234
  - low latency (~60 ns)
  - reasonable price (for a 1 GSPS ADC)
- 3 XCKU025 FPGAs
  - each handles 2 ADC chips
  - dedicated DDR4 buffer
  - 1 Firefly output channel
- 4th Firefly channel for configuration / realtime commands
- Data packaging in 64 bit Firefly words— flexible:

16 bit trigger info	12 bit ADC 1 readout	12 bit ADC 2 readout	12 bit ADC 3 readout	12 bit ADC 4 readout

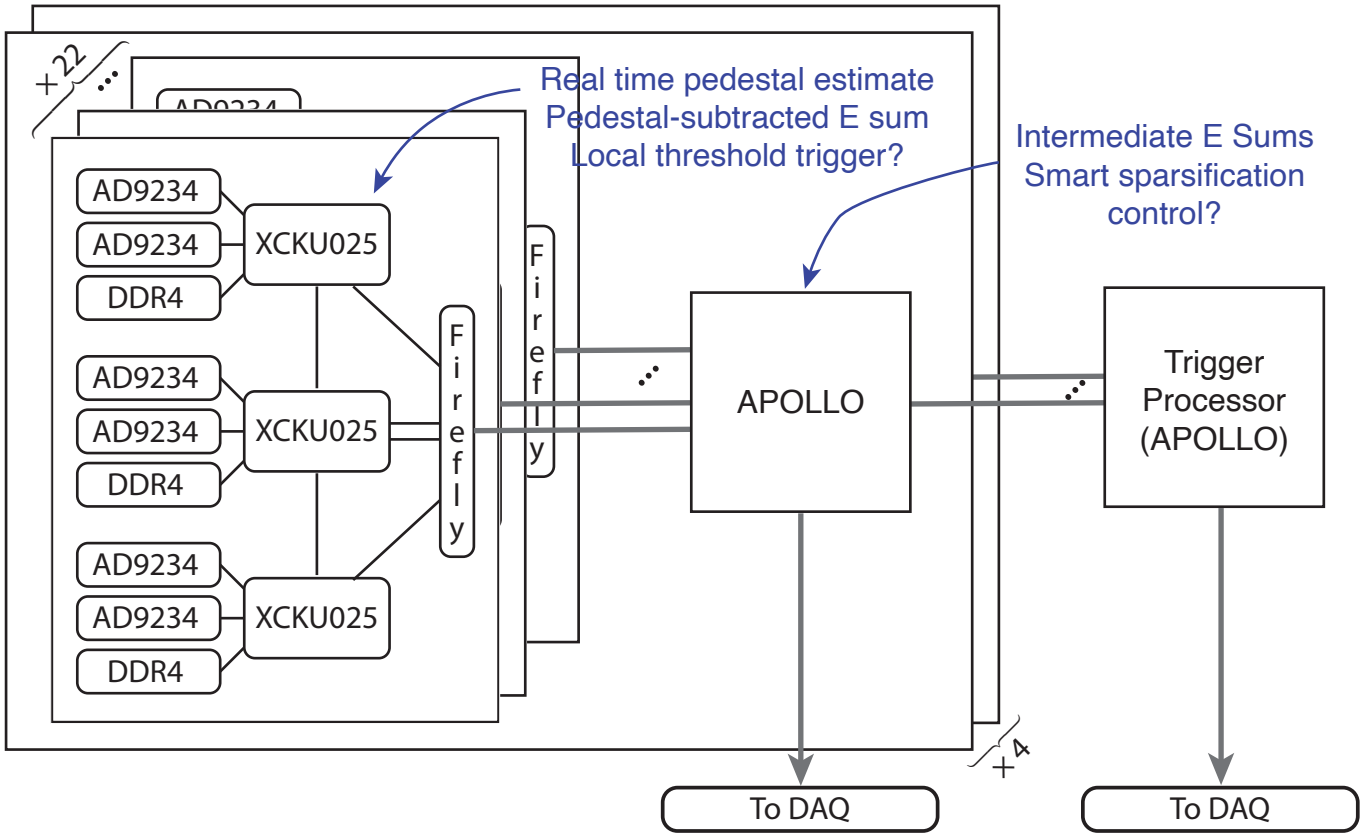
@ 250 MHz

40 bit trigger info	12 bit ADC 1,2 readout	12 bit ADC 3,4 readout

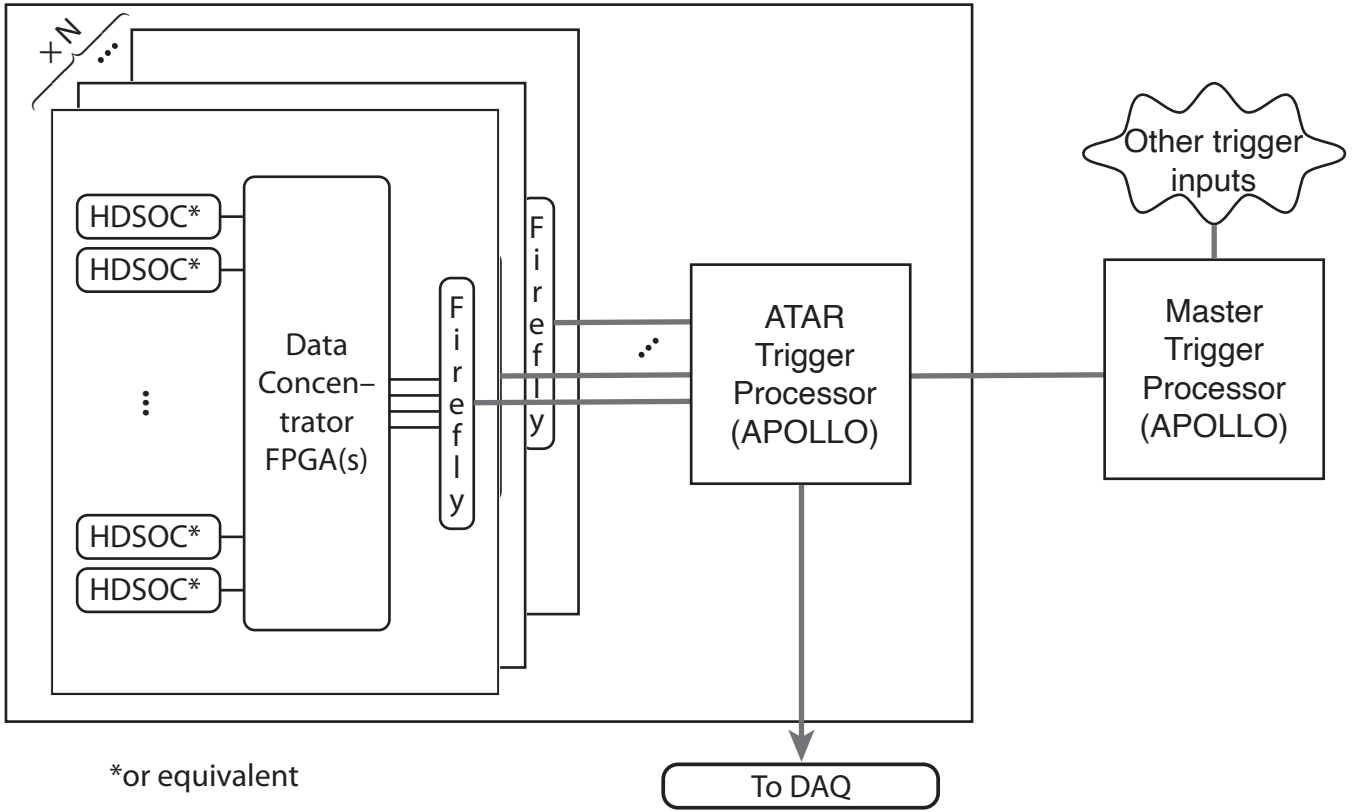
4-channel prototype layout



Instrumenting a ~1000 channel calorimeter



A reminder: could imagine similar for ATAR



*or equivalent

Goal: Deadtime-free design

- Option 1: DDR4 as direct circular buffer
  - ADC data streamed directly to DDR4 memory
  - Assuming 4 consecutive "bursts" of 8 512-bit words for reading / writing:
    - 50% rate efficiency ⇒ 150 MHz burst rate
  - Streaming → DDR4 uses 125 MHz burst rate
  - Leaves 25 MHz for reading
    - 10 kHz trigger rate w/ 256 ADC samples / channel / trigger needs 0.32 MHz burst rate
  - 32 GB DDR4 → ~0.5 s buffering
    - no constraint on trigger decision speed
    - problematic for downstream writing bottlenecks
- Option 2: Intermediate FPGA Circ. Buffer
  - Eg., g-2 WFD5 has a 65K buffer → 65 μs buffer
    - should be fine for triggering (we want O(100s ns))
  - Only Triggered events → DDR4
    - hours of buffering for even small DDR4

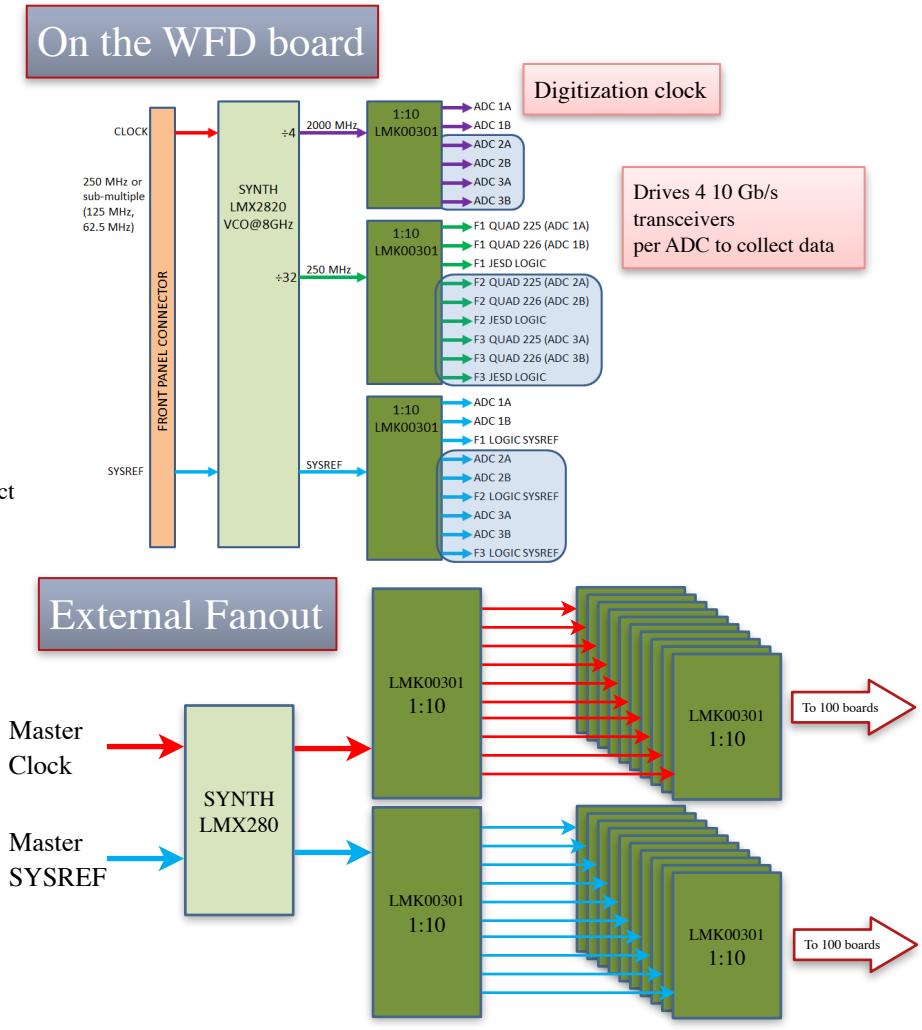
- ADC and FPGA data flow:
  1. The ADCs will run at 1000 MSPS.
  2. Two ADCs are in a chip.
  3. Two ADC chips will connect to two independent JESD204C blocks in each FPGA.
  4. Each ADC chip will transfer data from its two ADCs over 4 serial lines running at 10 Gbps using 8b/10b encoding.
  5. The JESD204C blocks will run at 250 MHz (10 Gbps line rate divided by 40).
  6. The JESD204C blocks will produce 128-bit words at 250 MHz. Each word contains 8 samples (4 per ADC).
  7. A 256-bit word will be formed at 250 MHz by joining the outputs of the two JESD204C blocks.
  8. For memory storage, a 512-bit word will be formed at 125 MHz by joining 2 consecutive 250 MHz words. The 64 bytes in this word contain 8 2-byte samples from each of 4 ADCs.
  9. For triggering, 4 consecutive samples from each ADC will be summed, producing a 16-bit word at 250 MHz. The 4 words from the 4 ADCs will be joined to produce a 64-bit word at 250 MHz. This will be sent downstream.

- FPGA and DDR4 memory maximal data flow:
  1. A -2 speed grade FPGA can handle a memory speed up to 2400 MHz (1200 Mhz clock).
  2. The memory data bus word width is 64 bits
  3. The memory module socket is a 260-pin SODIMM.
  4. Data is written or read in "bursts". A burst is 8 consecutive 64-bit words, or 512 bits.
  5. The interface between the FPGA logic and the memory controller is 512 bits wide (8 words). This matches the
     words produced in step #8 above.
  6. The interface to 2133 MHz memory can accept or produce bursts at 300 MHz.
  7. Alternating writes and reads of at least 4 consecutive bursts can achieve a memory utilization efficiency of 50%. This is a maximum burst rate of 150 MHz. Writing needs 125 MHz, leaving 25 MHz for reading.
  8. If each readout is 256 samples, or 32 bursts, a 10 kHz event rate requires a 0.32 MHz burst rate.
  9. Efficiency can be improved by reading or writing more consecutive bursts. It can get up to 90% if 64 consecutive bursts are in each write or read operation

The Cory DDR4 Details (C Stroman)

Clock distribution & alignment

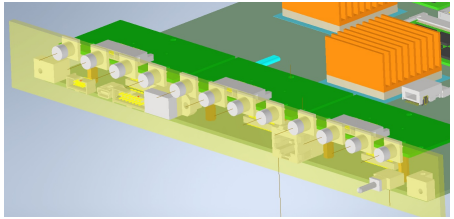
- One g-2 WFD5 irritation: clock jitter → time misalignments between ADCs at several different clock periods
- Build time-alignment into PIONEER system
  - standardized ADC protocol (JESD204B) provides tool
    - periodic SYSREF signal tightly timed to rising edge of ADC clock (2 GHz clock for 1 GHz sampling) to collect
      - O(100 ps) tolerance
  - special purpose clock synth chips allow creation / control / realignment of SYSREF + CLOCK
    - PIONEER: TI LMX2820
    - LMK00301 low-jitter clock buffer for fanout (1:10)



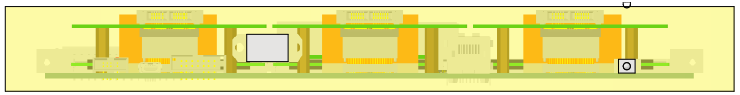
Form factor & Mezzanines

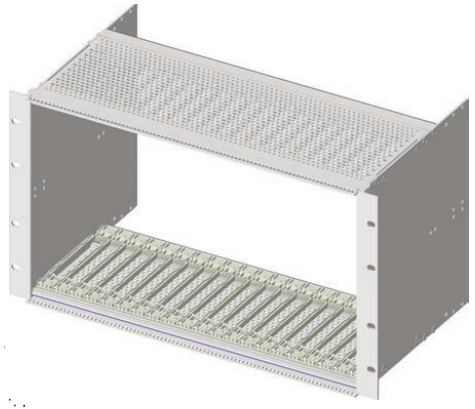
- Main board: 6U×220mm Eurocard format, 1.2” spacing
  - 14 boards in (probably) a Vector Electronics CCA68-84-01 chassis
  - power distribution via a 3U backplane
- Analog Front End (AFE), power supply → individual mezzanines
  - the power supply failed most often for g-2 WFD5s
    - replace cheap mezzanine than instead of expensive full board
- Need guidance / specs for AFE
  - differential input? (better noise immunity)
  - single-ended input? (convenience)
  - looking for options that could support both form factors

standard SMA OK,
Twinax SMA challenging

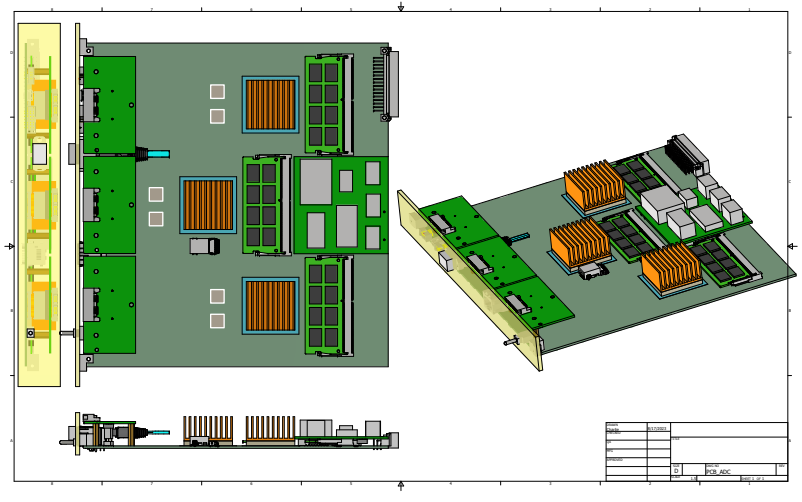


3 g-2-style 4-channel differential inputs





Status / Near-term plans



- Design of 4-channel (1 FPGA) well along
  - 1st pass of physics data flow complete: schematics and routing
    - routing for clocks, power, utilities remains
  - Full design always in mind to ensure everything fits
    - simplifies addition of remaining channels

- Next steps
  - Firmware for Command Module
    - IPBus
    - PCIe over firefly
    - Timing / latency measurements
  - Resume 4-channel prototype of digitizer (WFDP?) when funding available