# ATAR Readout

Peter Kammel

Representing ATAR team: UCSC, UW, BNL

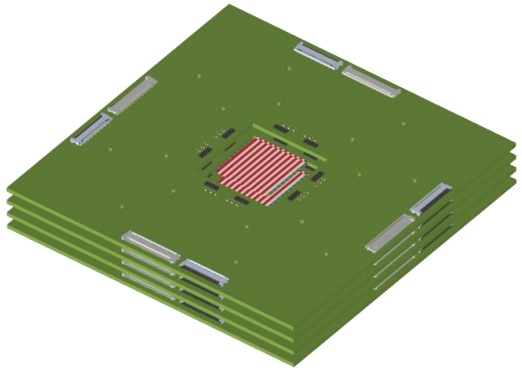
Simone, thanks for your slides !

UW: Theresa, David P., Tim van W., Marcel and Ryan

# Strategy FEB Development

## Front End Board

Reality check compared to Oct 23 Coll meeting



pFEB with minimal board spacing. Few mm gaps between pFEBs and sensor modules.
FAST3

FEB, Rigid-flex board with minimal thickness retracked behind ATAR.

Pre-production prototype

UCSC board and FAST2 chip

Baseline goal before 2026 shutdown

2023 — Start

2024 — Step1

2025 board
2026 integration — Step2

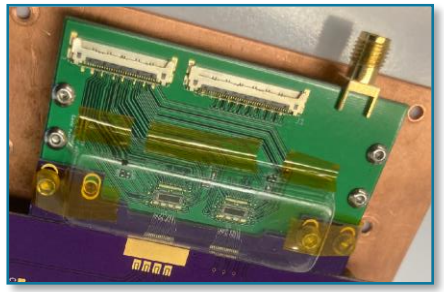
2026 board — Step3

Step4

Including digitizer

proto frontend board pFEB, UW

First transmission LGAD board

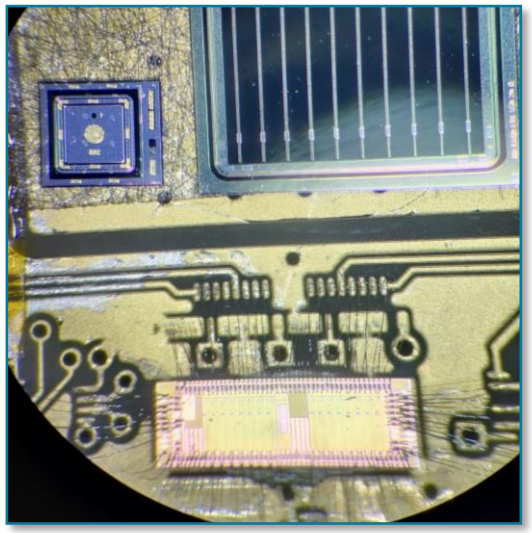


pFEB with flex between sensor and amplifier. Sensor close packing.

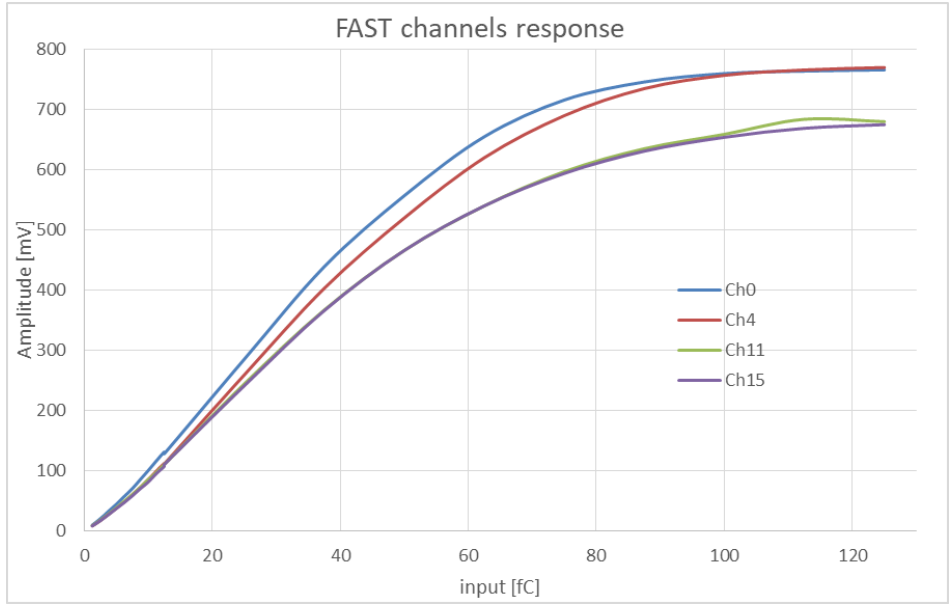
Stretch goal before 2026 shutdown

# FAST3

- Received FAST3 chip a few months ago
  - Improved driver and dynamic range
  - Noise ~1 mV, dynamic range up to ~800 mV
  - 8 different configurable gain settings
- Tested with calibration system, LGADs, AC-LGADs and PIN sensors
- Tested all 4 channels with calibration (0, 4, 11, 15), noticed difference in performance and baseline
  - Highest value reachable is 100mV lower for 11/15
  - If 11/15 are exposed to light, the gain is reduced
    BUT higher maximum voltage
    Mystery, discussion with designers



- Channel 0/4 have higher response and range than 11/15
  - At low input roughly the same, difference higher at large inputs. Up to 20% variation. Not sure why?
- Noise roughly the same for all channels
- But baseline is different! Mainly for 11, 15
- Rise time between 1-1.5ns,
- Full collection in 5-7 ns + undershoot

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# FAST3 dynamic testing

- Tested FAST with HPK 3.1 50 um thick single pad LGAD sensors and same geometry PIN detector (4.2 pF input capacitance)

  RMS noise in both cases is around 1 mV

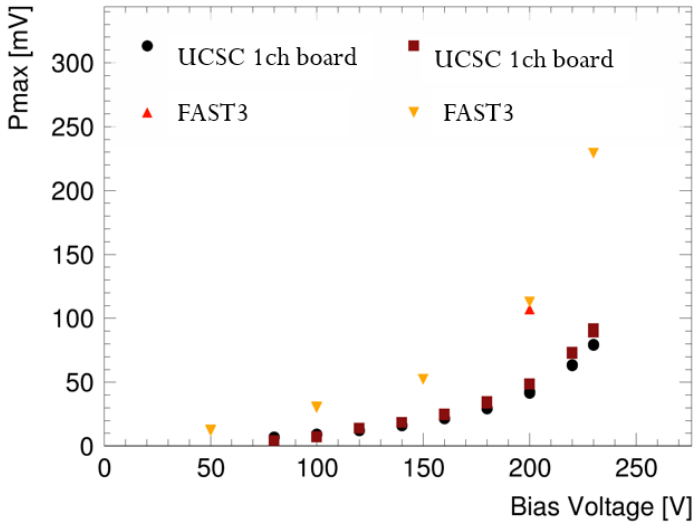
Response to LGAD better than expected
(~10-15 mV/fC, expected 10 mV/fC)

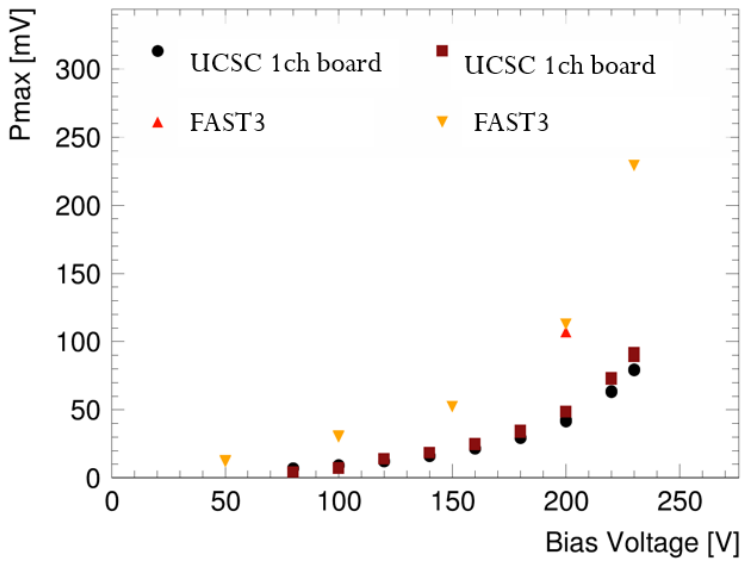
For 50 um PIN less than (naively) expected

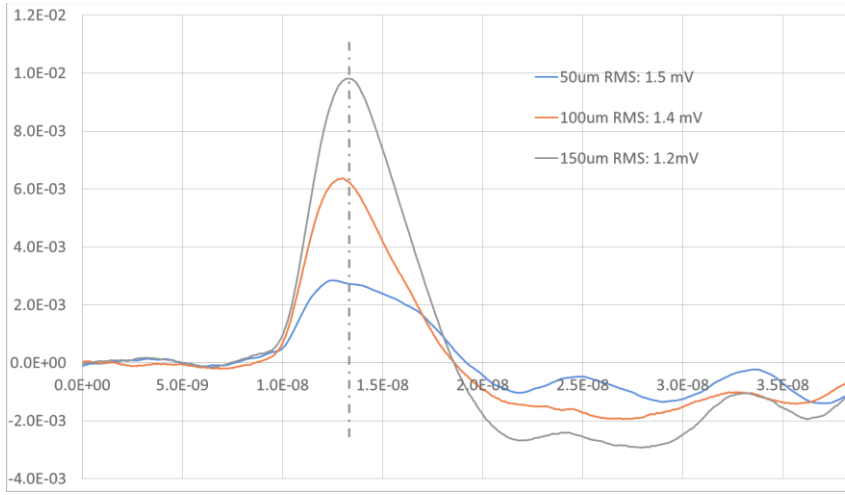
- expect a signal >5mV (S/N > 5),
- observed S/N to 4
  probably ballistic deficit (PIN signal is too fast)

For a 150 um PIN device we get a S/N > 10!

- Possible option for PIN version using thicker ATAR layers?
- Pmax scales with thickness

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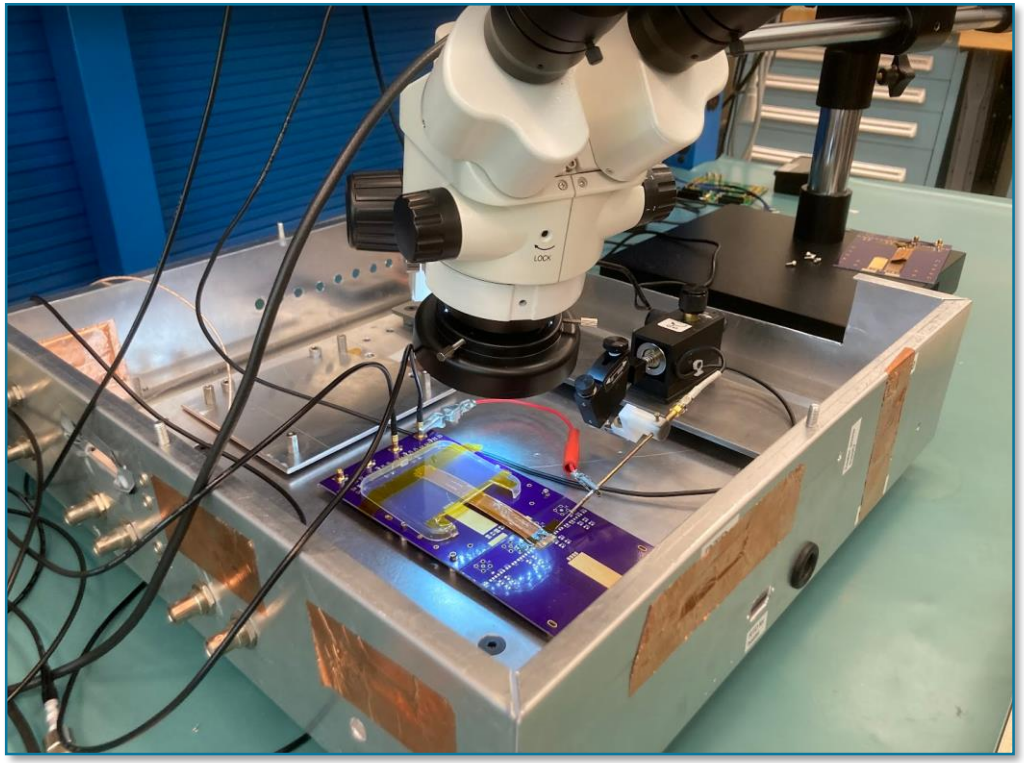
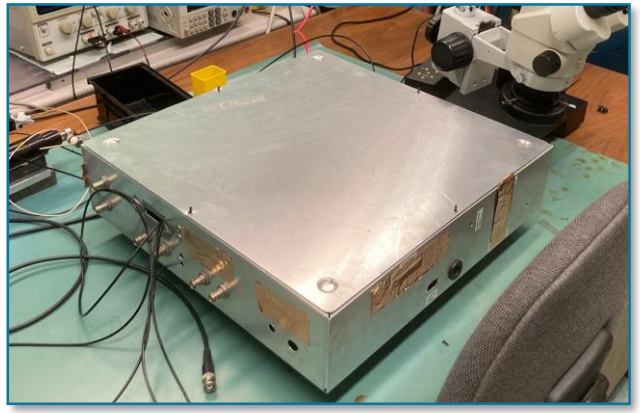
# Infrastructure development @ UW

- Mini Probe Station
  - Shielded probe station
  - 3 probes on micro positioners, one “RF” probe
  - Flexible and well-grounded mounting plate to test various LGAD-flex-electronics combination



- Parylene coating
  at Washington Nanofabrication Facility
  Marcel

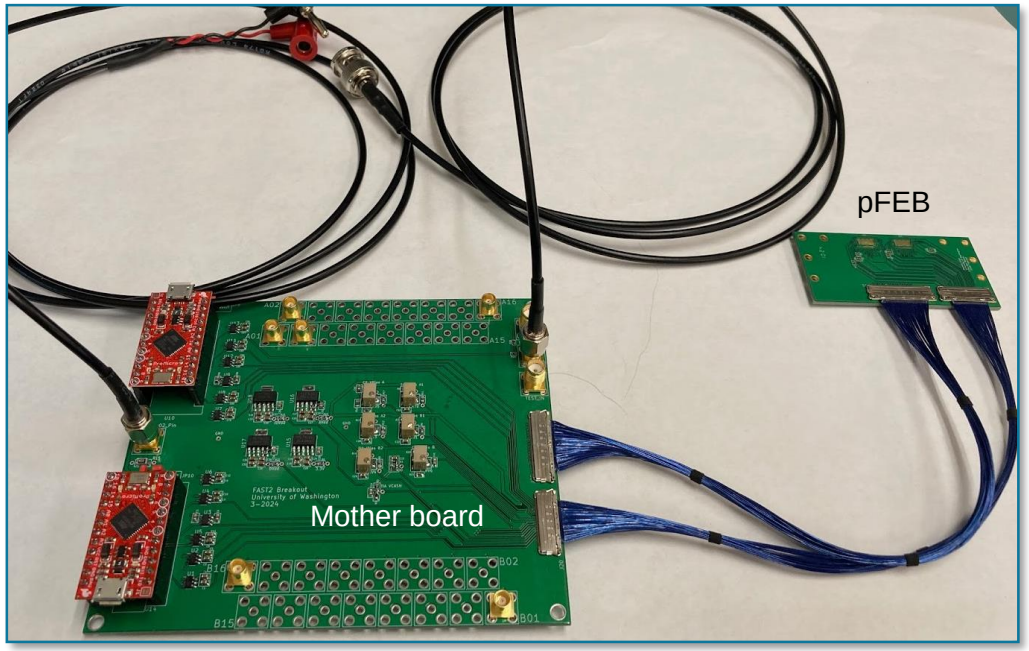
Powerful radio stations in Seattle



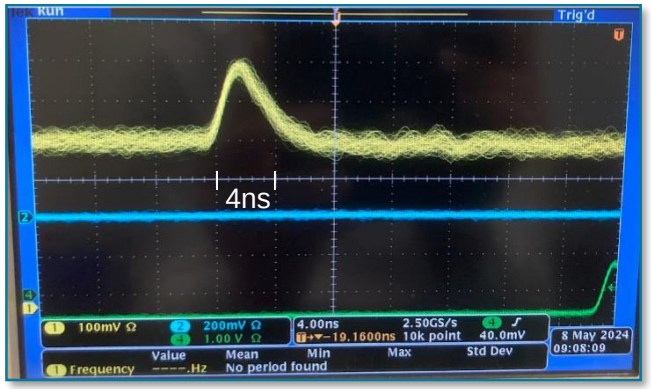
# pFEB Status

- pFEB system
  - Small front-end board for two FAST2 (32 channels)
  - Low voltage periphery on mother board
  - Connection analog and supply
    - I-PEX CABLINE®-CA II

pFEB system

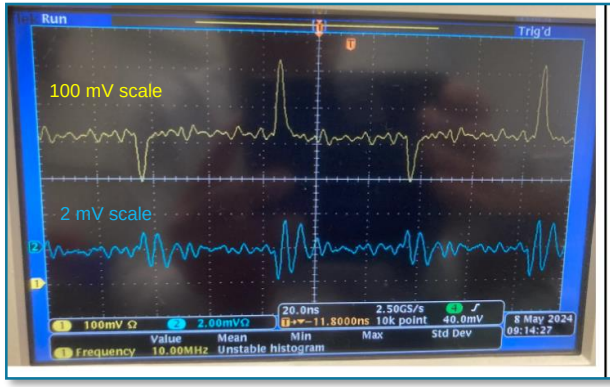



- Performance from initial tests
  - basic functionality ok
  - signal shape ok




  - Cross talk sub percent
  - noise 1.3-1.7 mV,
    somewhat better than UCSC board, lower bandwidth?
  - dynamic range still problematic. Signal flattens out after 200 mV
  - RF pickup with probe tricky

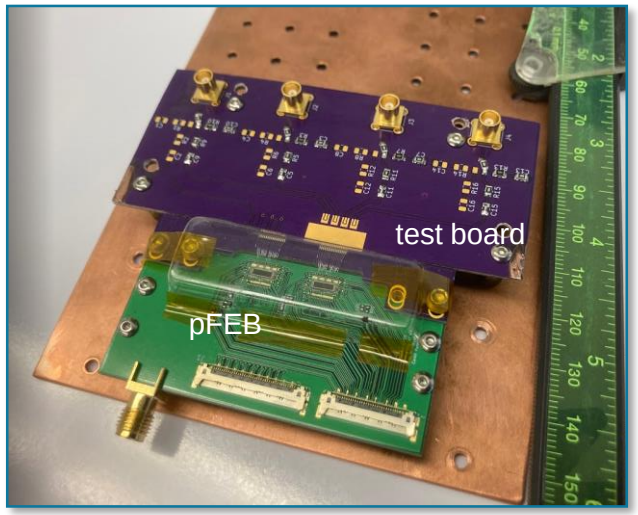
Next channel




Far channel

# pFEB Plans

- Testing
  - Repeat basic tests with 2nd board and SMA charge injection

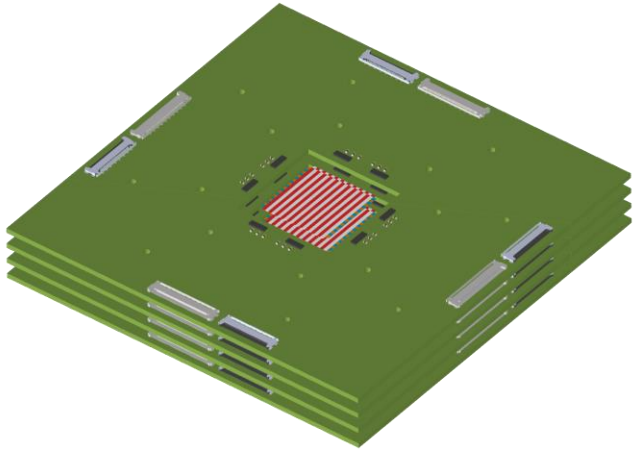



pFEB with test board

  - Advanced tests
    - explore bit pattern gain control on Arduino, maybe hardware issue
    - check all channels V vs charge, 4 SMA inputs
      - measure cross talk as well
      - measure FAST2 gain
      - measure FAST input impedance (gain dependent)
    - measure allowed range of V, I of low voltage supplies
      - criteria
        - pulse shape
        - V vs charge
    - establish DAQ with SAMPIC (11 bit, SCA cells, 1V, BW>1GHz)
    - other commissioning tests ?
    - strip LGAD - FEB, many channels
    - strip LGAD - Flex - FEB

- Recap 2026 configuration

| | | fraction of final |
|---|---|---|
| Sensors/board | 4 | |
| LGADs/board | 8 | |
| FAST/LGAD | 2 | |
| channels/LGAD | 32 | |
| # boards | 4 | |
| **totals** | | |
| thickness (mm) | 1.92 | 0.32 |
| channels | 1024 | 0.21 |
| LGADs | 32 | 0.17 |
| sensors | 16 | 0.33 |



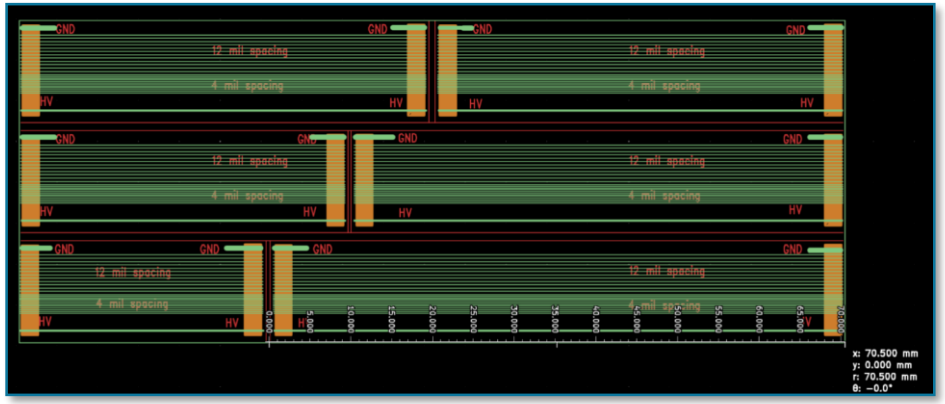
# Flex

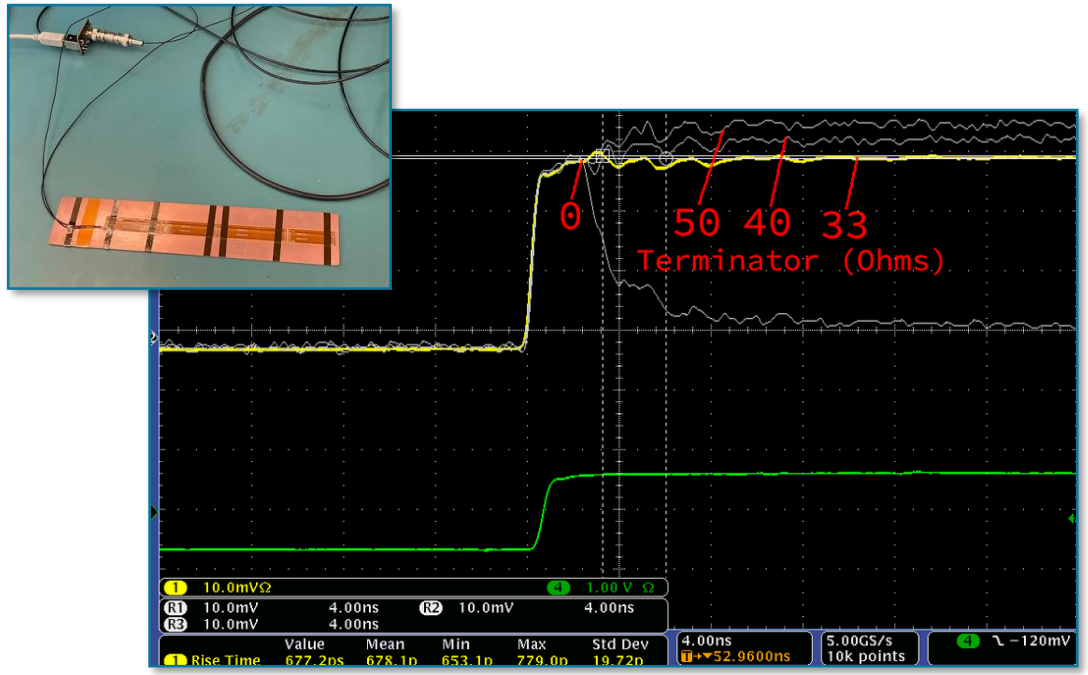
Flex between LGAD and electronics unusual, but unavoidable for PIONEER

Independent studies at UCSC and UW

- Issues
  - Cross talk
    - For a long time UCSC measured ~10% for 5cm cable, see discussion. Not expected from UW calculations
  - Poor impedance matching of present flex design
    - 33 Ohm (Tim and David)
  - Additional capacitance
    - Calcs Peter and Tim: 1-2 pF/cm depending on design
  - Noise pickup

- Goal
  - Understand and design optimal flex



# New Flex measurements UCSC

**Issue of higher-than-expected cross talk in the flex over long distance**

Setup with injection probe had high external pickup and reflection issues

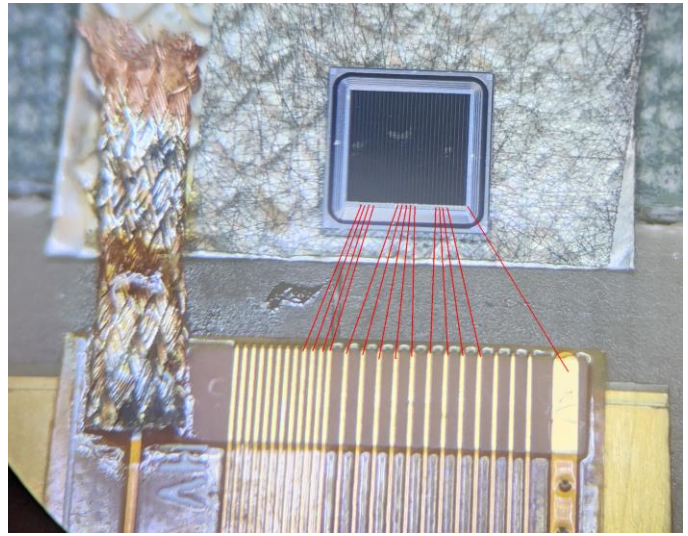
Tested again with mounted sensor to have cleaner (and more realistic) signal injection

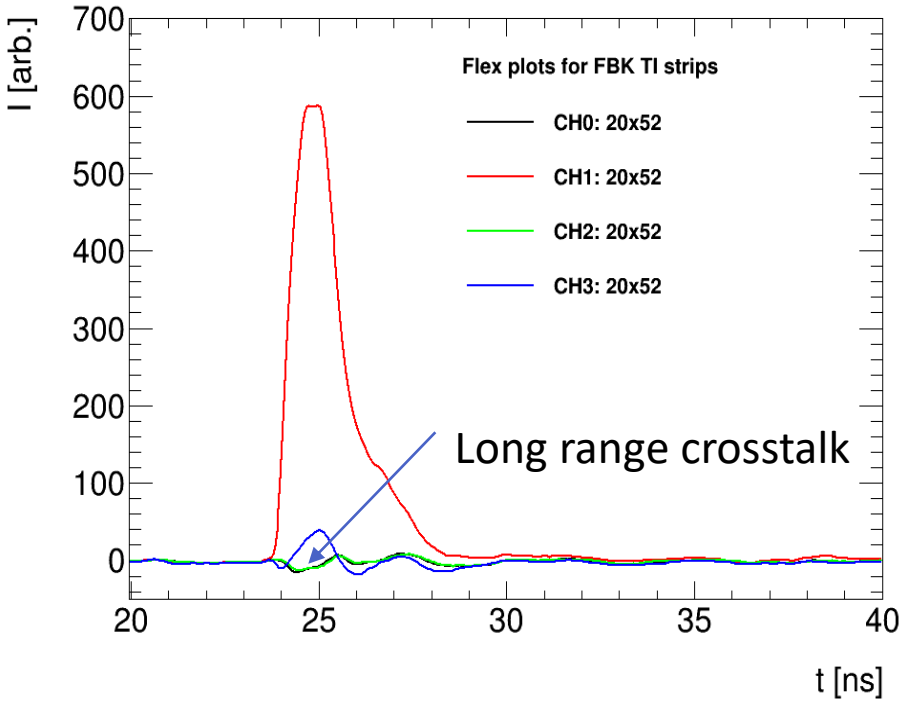
- FBK TI-LGAD strip sensor
- Laser on top of CH1
- Ch3 neighbor, Ch1 and Ch2 far away strips

Results

- No cross talk from strips connected to the board (how it will be in PIONEER)
- Cross talk with first neighbor ~10%
- Long range cross talk is minimal

- Cross talk from the gold grounding pin that was also used for previous needle tests!



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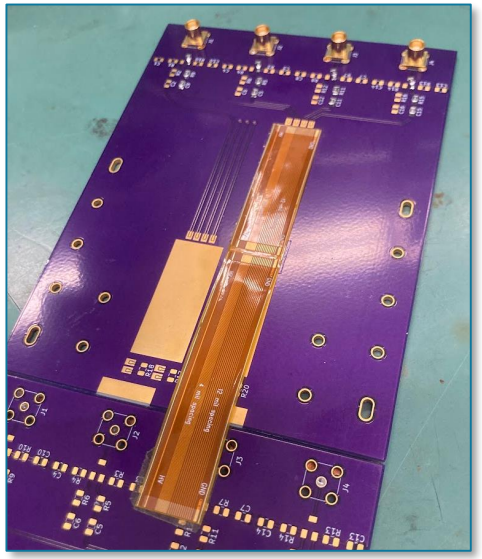
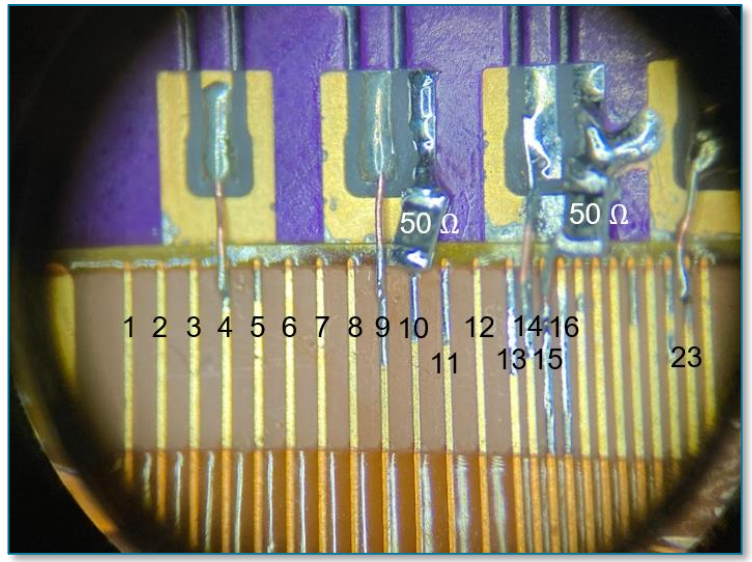
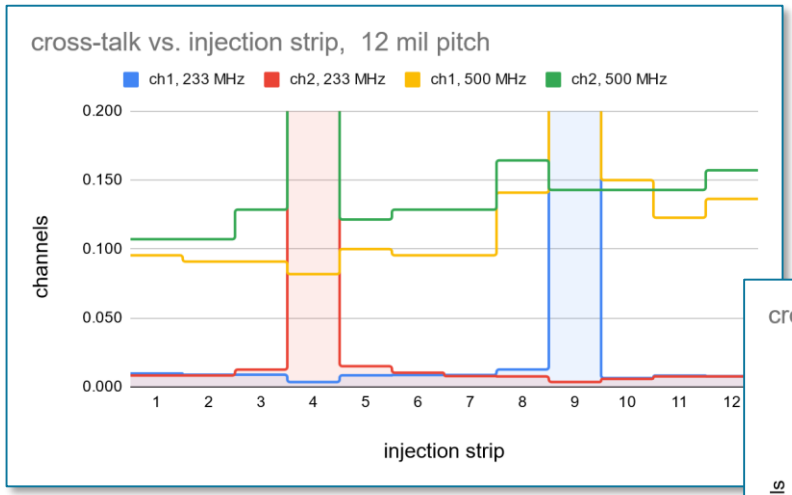
# UW Flex Tests

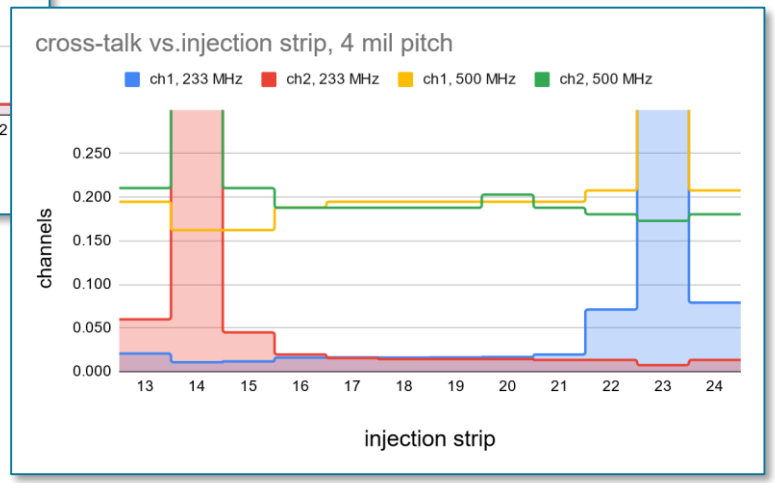
- Tests (clean set-up, 10 cm flex)
  - Pulse injection
  - RF generator
- First prelim. Results
  - 233 MHz ~ 1.5 ns
    - far cross talk and next neighbor <1%, 300µm pitch
    - far cross talk < 1.6%, NN < 8%, 100µm pitch
  - But strong frequency dependency
    - We might get away, but better be careful
  - syst. measurements with new setup starting
- Further plans
  - Match flex impedance
  - Measure with pFEB and LGAD
  - Design optimized flex





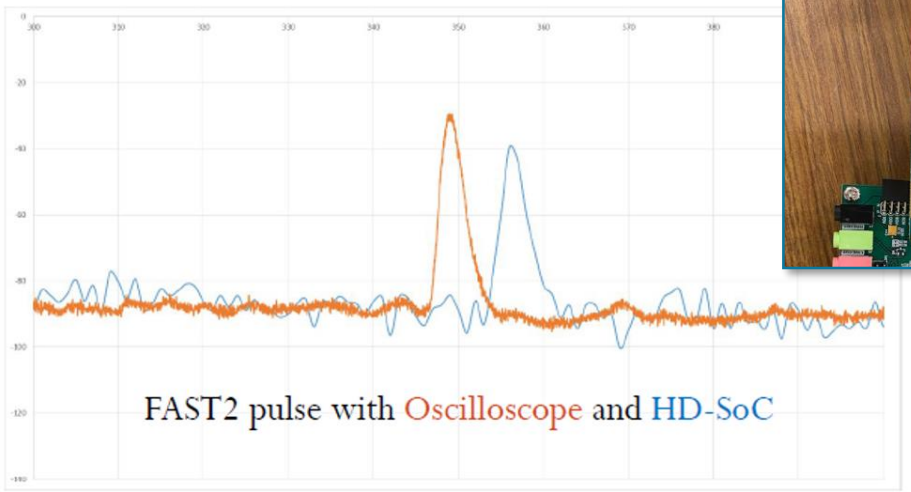




Measurements 6/18/2024

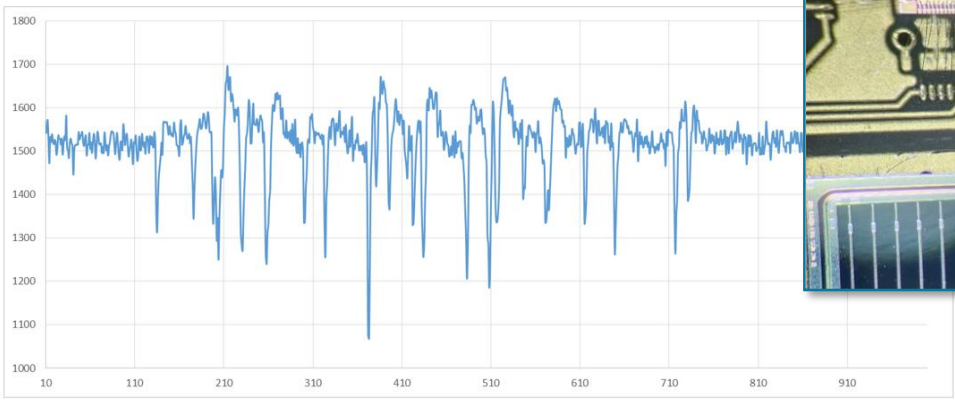


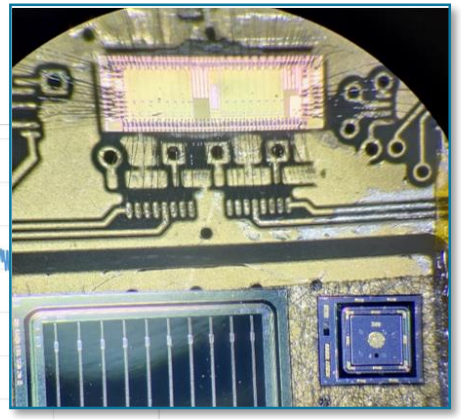
# Digitizer HD-Soc from Nalu

- HD-SoC from Nalu Scientific in evaluation at UCSC:
  - 32 channel (Next version: 64 channels)
  - 1Gs/s digitizer chip (might be up to 2Gs/s)
  - Buffer length 1024: 1 us window
  - 2.5 Vpp, 12-bits
- Collaboration with Nalu Scientific to understand the triggering capabilities of the chip
  - Trying the right firmware/software recipe to get to 2Gs/s




- FAST3 and HD-Soc tested at SSRL
  - using oscilloscope and HD-SOC digitizer
    - Test-beam two weeks ago, will analyze data in the next months
  - Single pad HPK 3.1 and HPK AC-LGAD 2 cm strips
  - Result of FAST3 and HD-SoC, 1us of time window
    - Useful to test repetition rate capabilities of this setup



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# Parylene Coating

- Marcel applied 5um parylene to copper plates at Washington Nanofabrication Facility
- Peter's tests

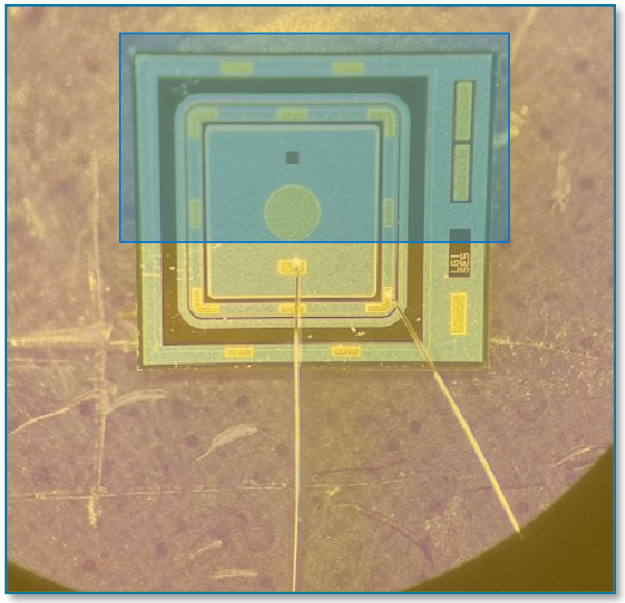
**First plate**

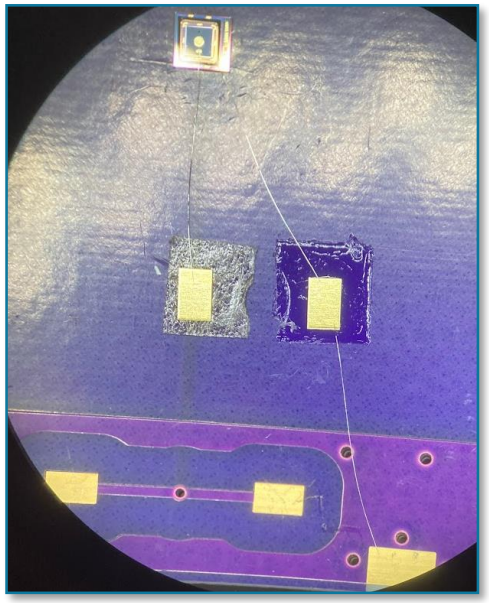
I placed the parylene covered plate on the bare plate and applied HV with a chamber power supply, with a fast trip. I could reach 500 V, then the HV tripped. Afterwards, it tripped at 400 and then at 350V.

**Second plate**

The 2nd plate was better (with the same bare copper plate). I left it on 500V for 30-40 min, and then ramped up to 800V, at which point it tripped. Afterwards it always tripped at 350V. Apparently the spark destroys the parylene cover, leading to lower dielectric strength.

These are promising results and are reasonable relative to the quoted dielectric strength: 276 V/micron at 25.4microns. Potential poorer performance can be due to our surface roughness. I suggest using 8 um in the future to play it safe.





- Produced boards for parylene coating
  - Example of Theresa's board
  - Will be coated after I-V test
- Marcel will try photolithography on parylene
  - That would allow selective coverage, no parylene over active LGAD region

# Summary

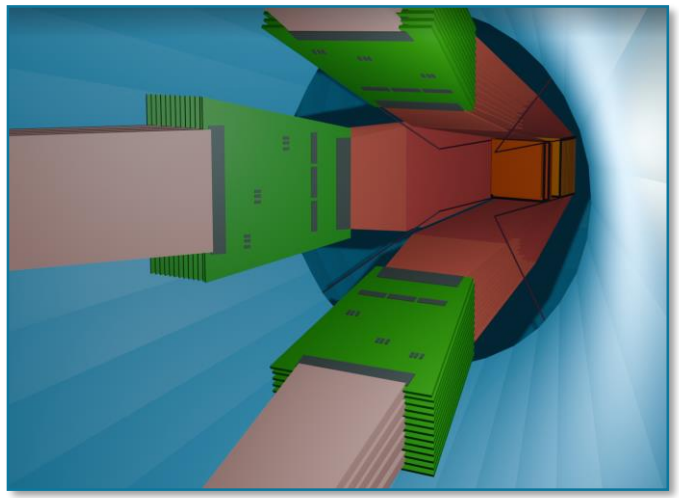
- Substantial progress since October 2023
  - FAST3 significantly improved over FAST2
  - pFEB from design to commissioning, several obstacles overcome
  - Flex. Does not seem insurmountable issue, though still challenges by long cable and full demonstration required.
  - Digitizer from Nalu. Promising, slow but steady progress.
  - Infrastructure at UW established

# Backup

# Read Out within Overall ATAR R&D

Update from my PSI BVR 2024 presentation

- Development directions
  - optimal customized PIONEER sensor
    - fully depleted 120 µm sensor, minimal dead material
    - minimal cross talk, small gain saturation, large dynamic range
  - Interface and Electronics for 5000 channels
    - frontend chips and board
    - flex
    - digitizer
  - Integration into stack with minimal dead material



- Goals 2024
  - Sensors
    - Characterization of
      new BNL sensors and
      TI-LGADs and thicker LGADs from FBK
    - ~~Acquisition of thin, double-sided Silicon sensors from Micron~~
    - Study of new LGAD devices with test beams at SSRL and CENPA
    - Conclude analysis of the PSI test beam data
  - Electronics
    - multi-sensor pFEB testing with sensors, towards sensor stack
    - Testing readout chips for low-noise PIN readout ?
    - Fabrication of improved flexes after tests and simulation
    - Digitizer development based on Nalu HDSoc chip
  - Integration
    - Sensor thinning (good enough, alternatives?)
    - Double LGAD
      Two sensors close packed and insulated by parylene

# Digitizer

- Sampic

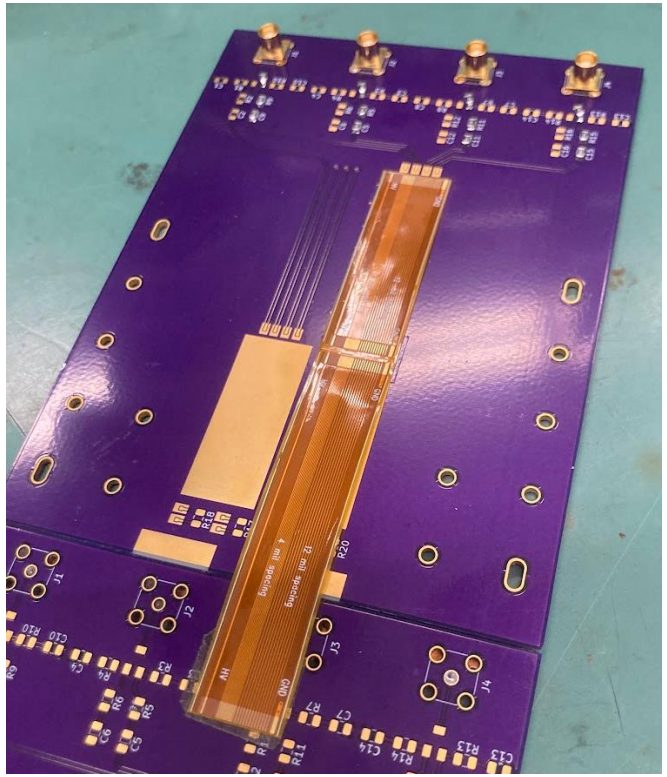
## SAMPIC: PERFORMAN

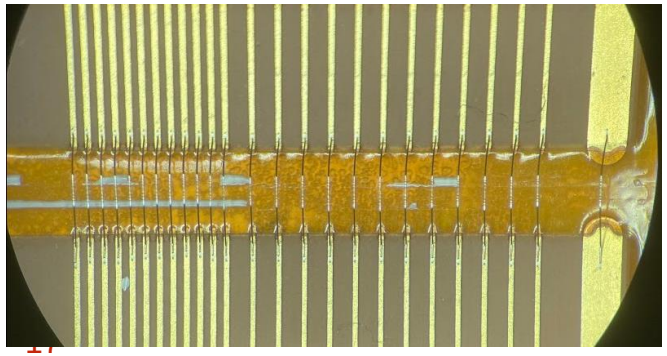
| | | Unit |
|---|---|---|
| Technology | AMS CMOS 0.18µm | |
| Number of channels | 16 | |
| Power consumption (max) | 180 (1.8V supply) | mW |
| Discriminator noise | 2 | mV rms |
| SCA depth | 64 | Cells |
| Sampling speed | 0.8 to 8.5 (10.2 for 8 channels only) | GSPS |
| Bandwidth | > 1 | GHz |
| Range (unipolar) | ~ 1 | V |
| ADC resolution | 7 to 11 (trade-off time/resolution) | bits |
| SCA noise | < 1 | mV rms |
| Dynamic range | > 10 | bits rms |
| Conversion time | 0.1 (7 bits) to 1.6 (11 bits) | µs |
| Readout time / ch @ 2 Gbit/s (full waveform) | < 450 | ns |
| Single Pulse Time precision before correction (4.2 to 8.5 GS/s) | < 15 | ps rms |
| Single Pulse Time precision after time INL correction (4.2 to 8.5 GS/s) | < 3.5 | ps rms |

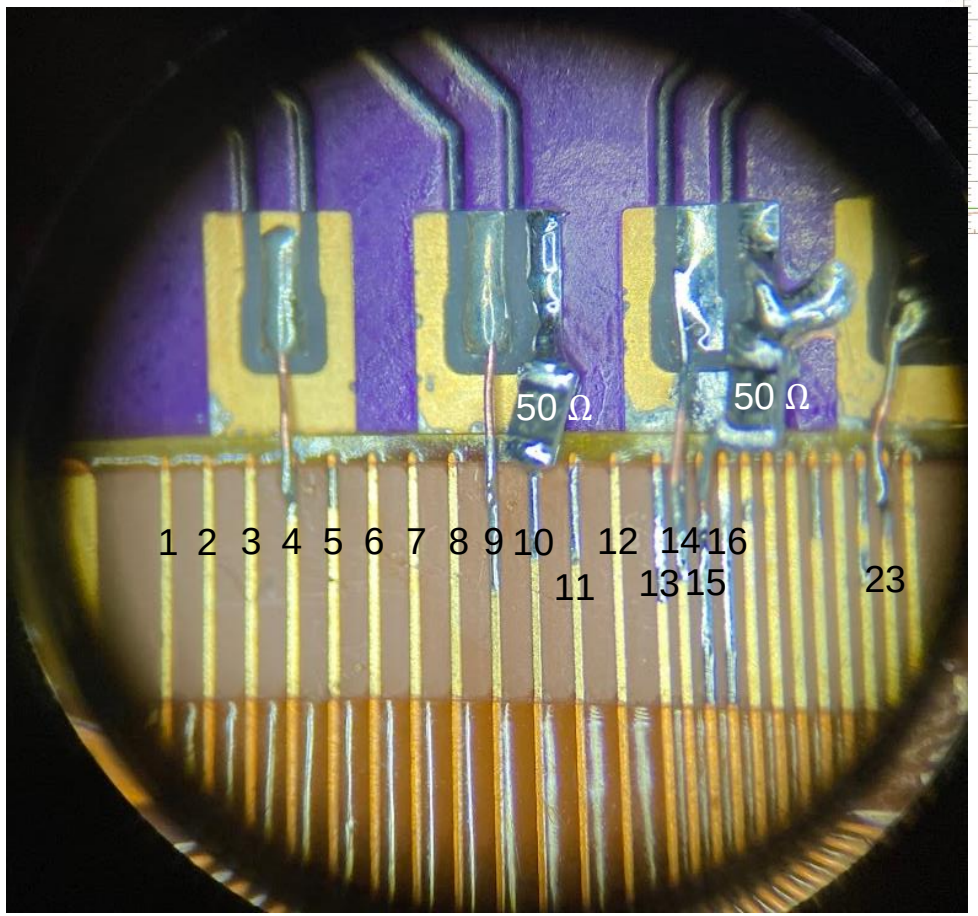
- V1742, domino chip

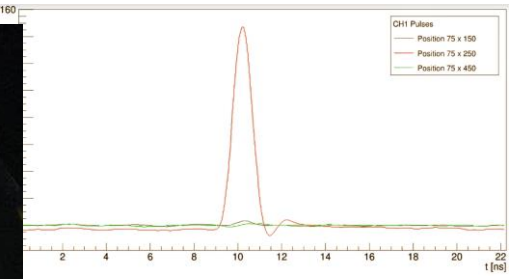
| | | | |
|---|---|---|---|
| GENERAL | **Form Factor**<br>1-unit wide, 6U VME64 (V1742) and VME64X (VX1742) | | **Weight**<br>520 g |
| ANALOG INPUT | **Channels**<br>32 channels<br>2 special channels (TR0, TR1)<br>Single ended<br><br>**Impedance**<br>$Z_{in}$ = 50 Ω | **Connector**<br>MCX<br><br>**Full Scale Range (FSR)**<br>1 $V_{pp}$<br><br>**Absolute max analog input voltage**<br>$3V_{pp}$ (with $V_{rail}$ max +3V or -3V) for any DAC offset in single ended configuration | **Bandwidth**<br>500 MHz<br><br>**Offset**<br>Programmable 16-<br>DC offset adjustme<br>channel. Range: ± |
| DIGITAL CONVERSION | **Resolution**<br>12 bits<br><br>**Switched Capacitor Array**<br>Domino Ring Sampler chip (DRS4), 8+1 channels with 1024 storage cells each | **Sampling Rate**<br>5 GS/s - 2.5 GS/s - 1 GS/s - 0.75 GS/s SW selectable, simultaneously on each channel | **Dead Time (A/D Cc**<br>110 µs, analog inpu<br>181 µs, digitizing T |
| ADC CLOCK GENERATION | Clock source: internal/external.<br>On-board programmable PLL provides generation of the main board clocks from int<br>MHz local Oscillator) or external (front panel CLK-IN connector) reference | | |
| DIGITAL I/O | **CLK-IN (AMP Modu II)**<br>AC coupled differential input clock<br>LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available by A318 adapter)<br>Jitter < 100 ppm requested<br><br>**TRG-IN (LEMO)**<br>External trigger digital input<br>NIM/TTL<br>$Z_{in}$ = 50 Ω | **CLK-OUT (AMP Modu II)**<br>DC coupled differential LVDS clock output locked at ADC sampling clock<br><br>**TRG-OUT (LEMO)**<br>Trigger digital output<br>NIM/TTL<br>$Z_{in}$ = 50 Ω | **S-IN (LEMO)**<br>SYNC/START<br>front panel digital input<br>NIM/TTL<br>$Z_{in}$ = 50 Ω |
| DIGITAL MEMORY | 128 events/ch or 1024 events/ch (1024 S/event) Multi-event Buffer<br>Independent read and write access; programmable event size and pre/post-trigger | | |
| TRIGGER | **Trigger Source**<br>- *Fast (Low Latency) trigger*: Programmable threshold on TR0 and TR1 (each TRn signal drives two 8-ch groups)<br>- *Self-trigger*: Logic OR combination of channels over/under threshold (each channel self-trigger drives two 8-ch groups)<br>- *External-trigger*: Common trigger by TRG IN connector<br>- *Software-trigger*: Common trigger by software command | | **Trigger Propagation**<br>TRG-OUT programmable digital output<br><br>**Trigger Time Stamp**<br>30-bit counter<br>8.5 ns resolution<br>9 s range |

User Manual UM4279
V1742/VX1742






50 Ω
50 Ω
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 23


160
CH1 Pulses
Position 75 x 150
Position 75 x 250
Position 75 x 450
2 4 6 8 10 12 14 16 18 20 22
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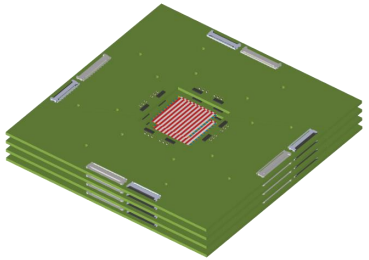

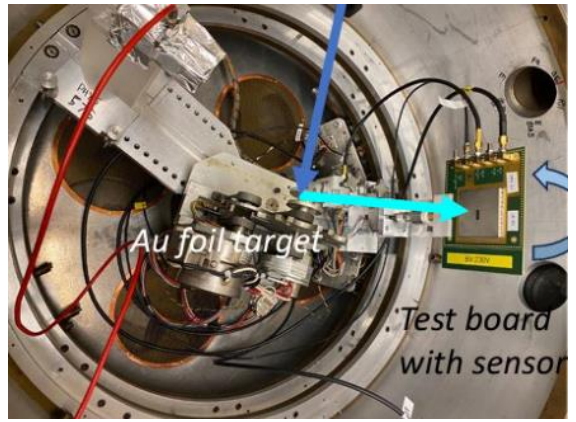
Au foil target
Test board
with sensor