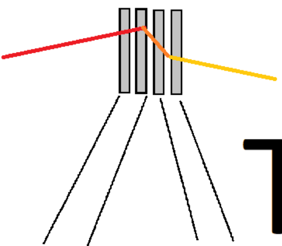
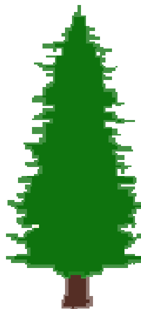
ATAR sensors processing, mechanics and DTAR discussion

Dr. Simone M. Mazza (UCSC) with inputs from many!

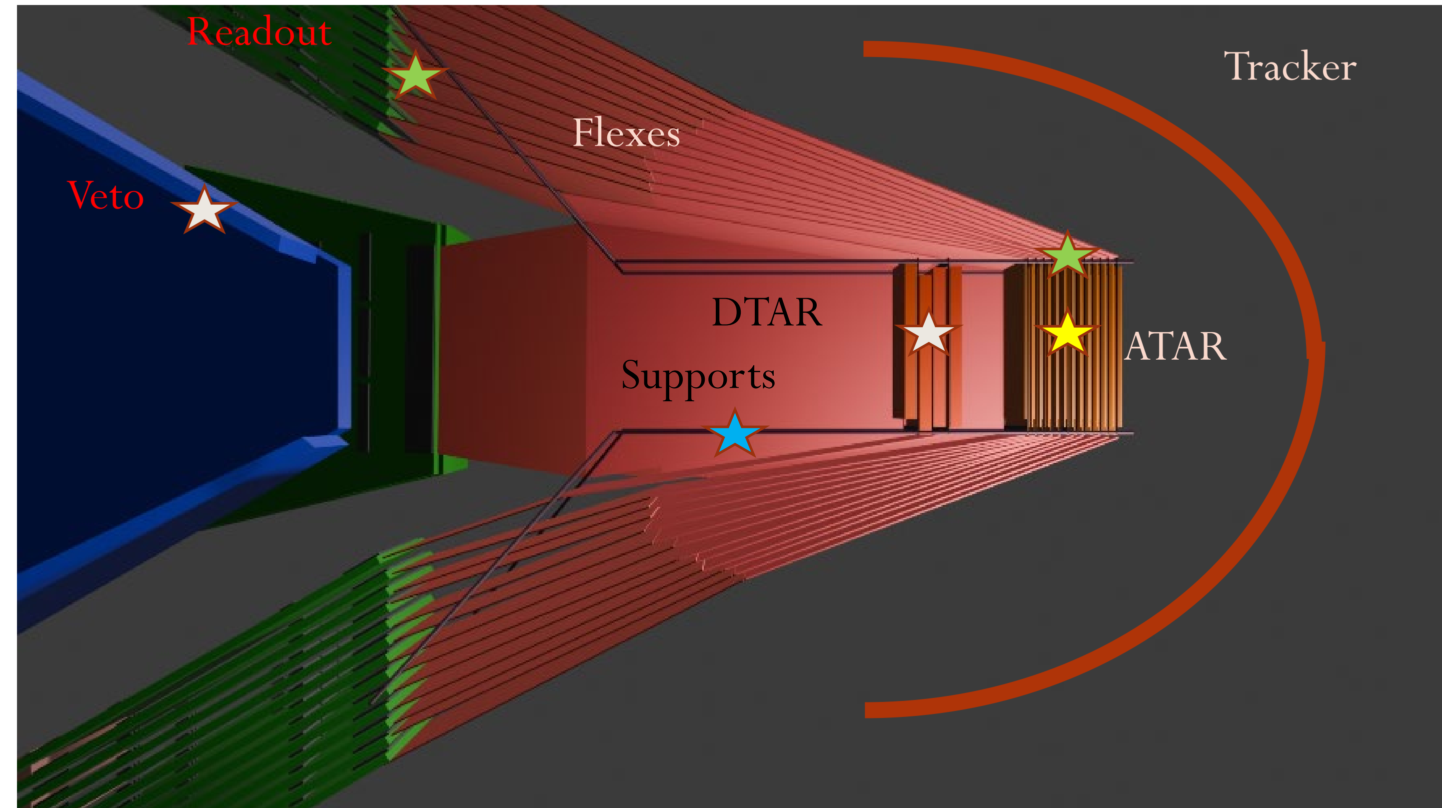




SCIPP
SANTA CRUZ INSTITUTE FOR PARTICLE PHYSICS
UC SANTA CRUZ

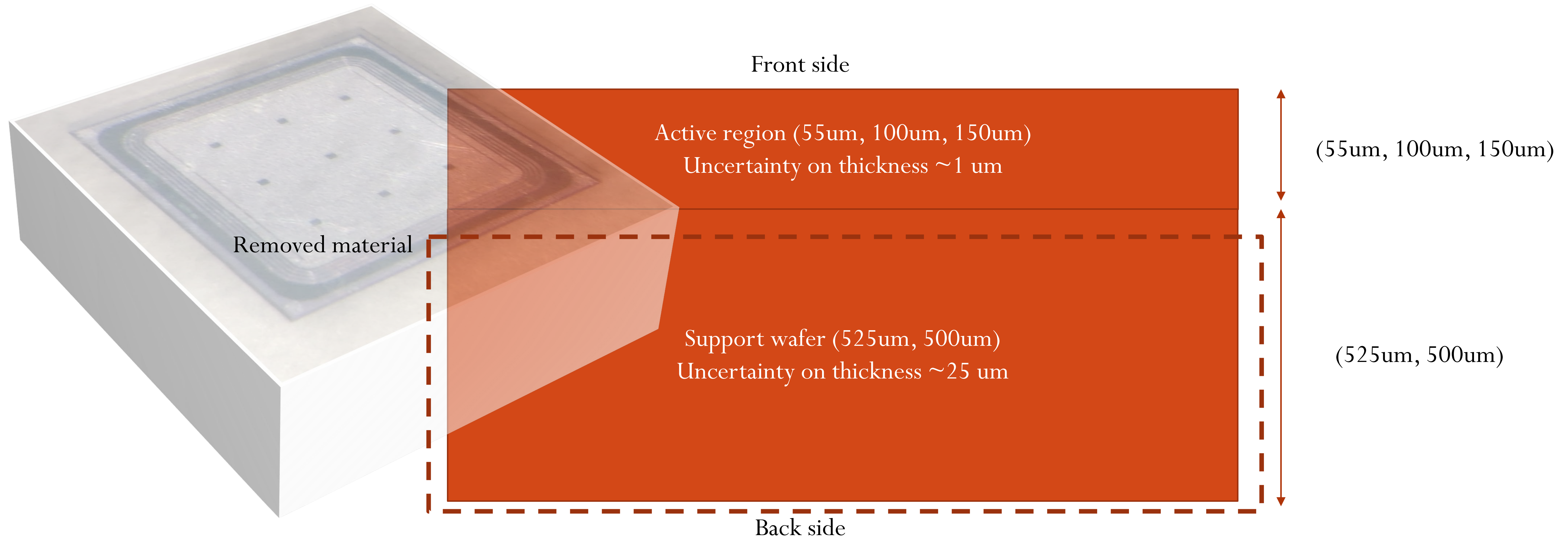
Summary

- Sensors processing ★
  - Die thinning
  - Parylene coating
- Assembly ★
  - spTAB
  - Metal bonding techniques
- Mechanics support ideas ★
  - Power dissipation
- DTAR/VETO ideas ★



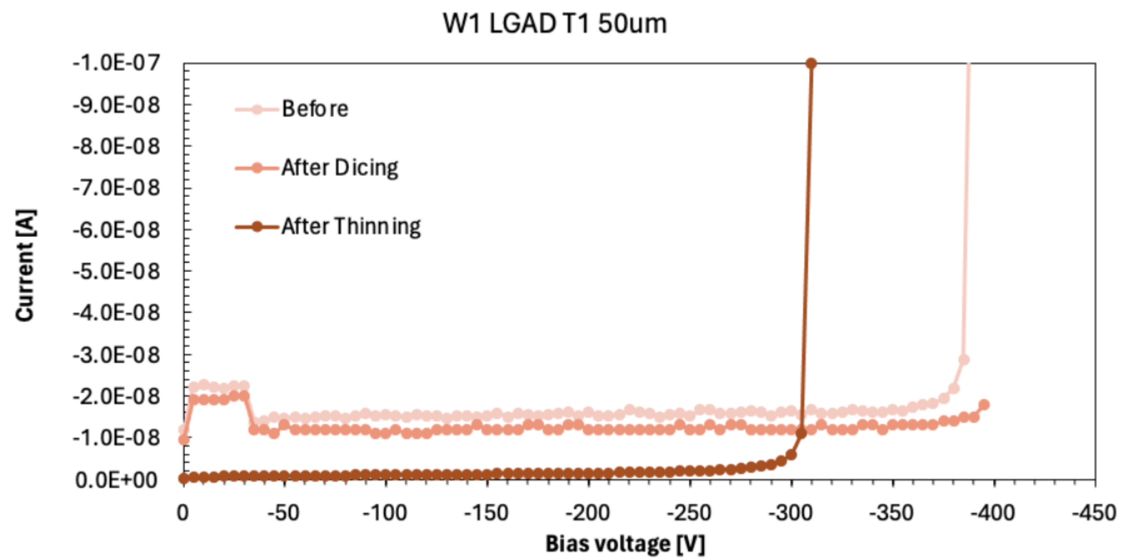
Sensor side view

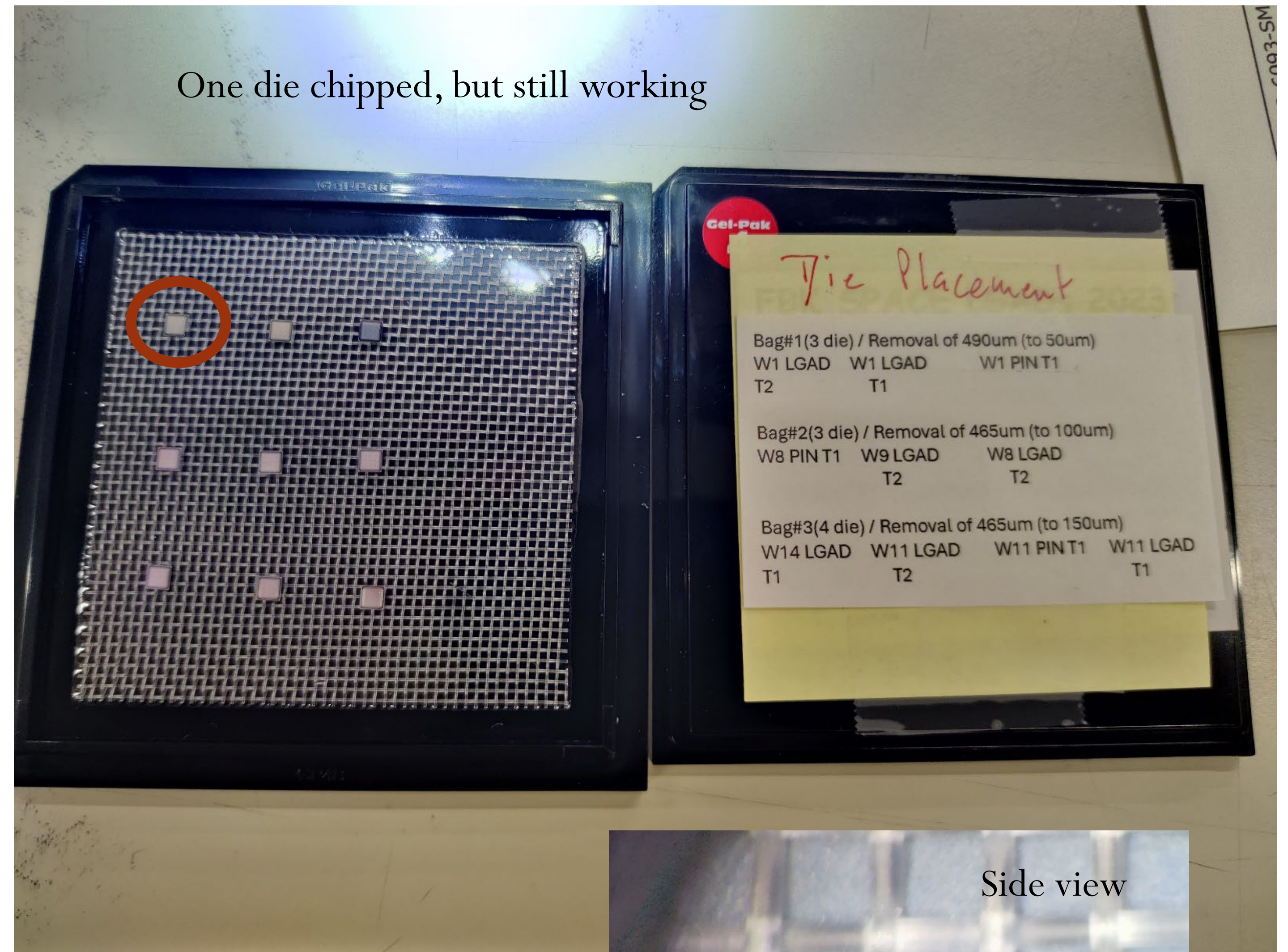
- The device has a thin active area on the front side and a thick support on the backside

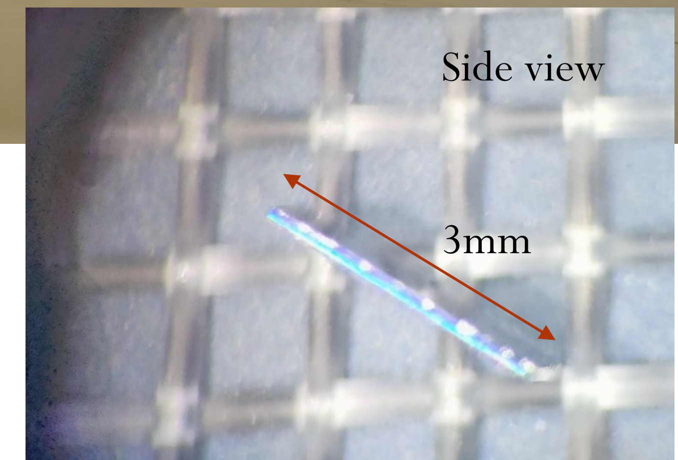


Thinned sensors

- Thinned 10 devices of different thicknesses from FBK
  - Active area thickness known well, support known within 25um
- Sensors work after thinning!
  - Cost of entire processing <1000$ (350$ dicing + 570$ grinding) for 10 small dies
- Crucial test to show that we can fabricate and thin down devices!
- Current and breakdown change
  - Behavior and gain to be investigated further

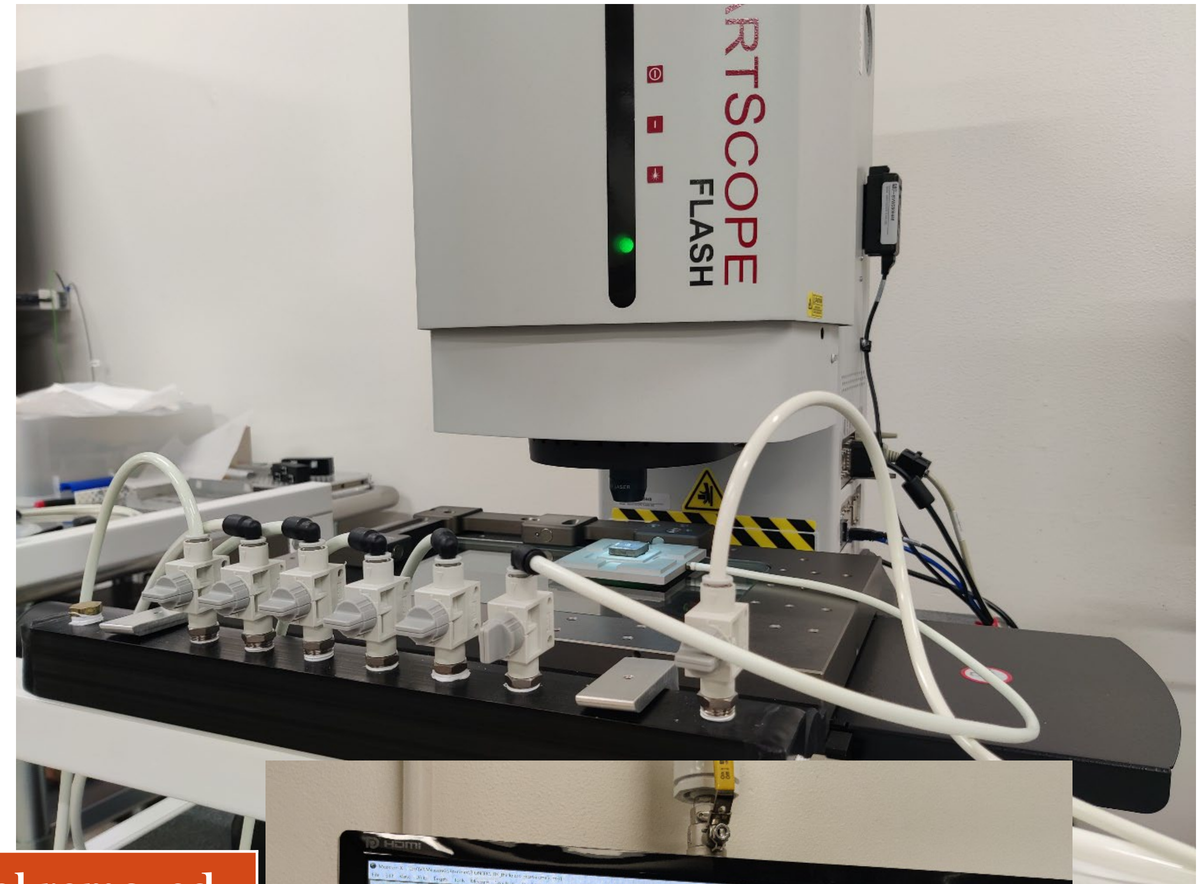


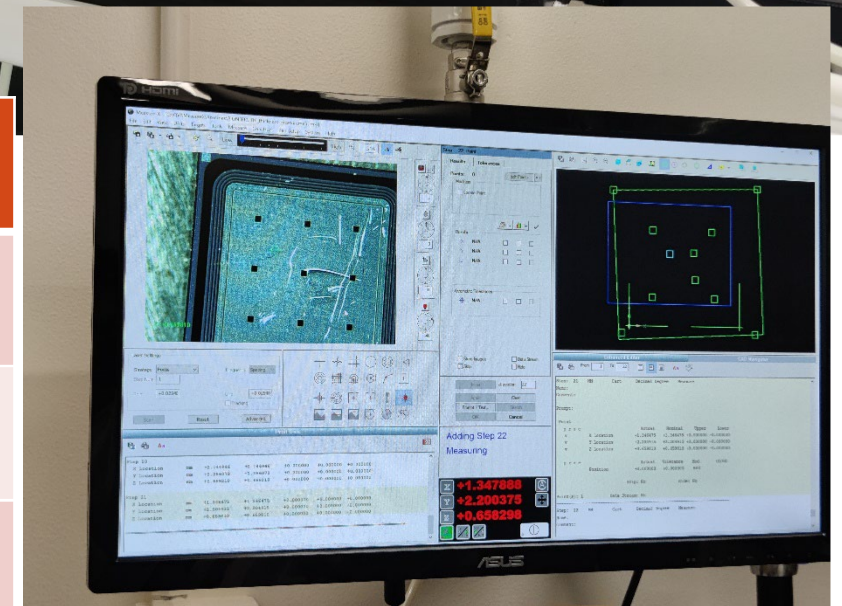




Metrology measurements

- SmartScope measurements on all the devices after thinning (and other device from the same wafer before thinning)
- 5-10 um off from the nominal thickness
  - Nominal thickness with support wafer uncertainty
  - Thinned/Un-thinned error from 8 measuring point on the die
- 50um device seems to have the higher shift from nominal
- Will test all available devices for statistics: might change die to die
- Next steps: use Metrology measurements to thin down as close as possible the support
  - Then: thin down a larger device

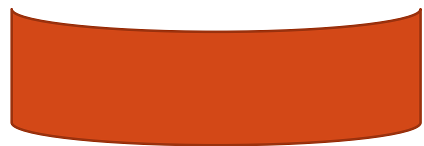




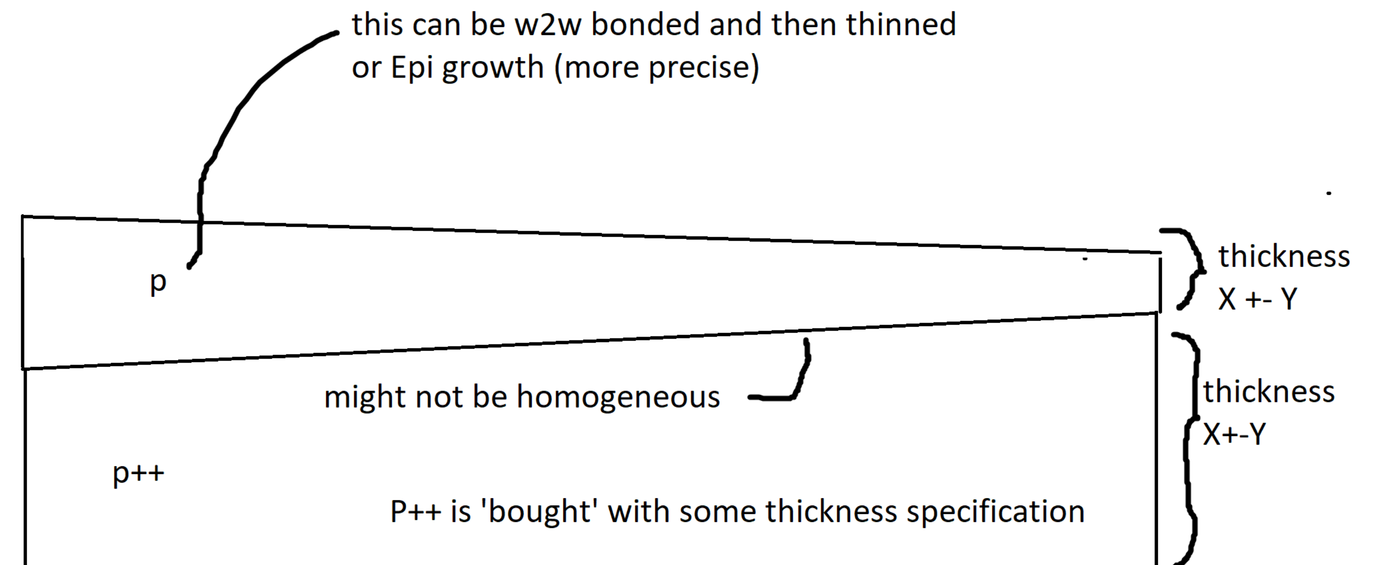
Sensor	Nominal thickness	Un-thinned thickness	Thinned thickness	Material removed (nominal)
FBK W1 LGAD (55um)	580 um ± 25 um	591 ± 3 um	88 ± 3.2 um	503 um (490 um)
FBK W9 LGAD (100um)	600 um ± 25 um	607 ± 1.7 um	141 ± 2.3 um	466 um (465 um)
FBK W14 LGAD (150um)	650 um ± 25 um	655 ± 1.2 um	187 ± 1.8 um	468 um (465 um)

Discussion with FBK – wafer thinning

- FBK suggested a few ways to remove completely the support wafer:
  - Chemical attack that is sensible to doping, so it would stop at the interface.
  - Grinding machines should have an end-point mechanism that detects the change in interface, which is useful for understanding support thickness in the test structures.
  - Using SOI support, the support wafer is an insulator, so the interface can be detected more effectively. One might need particular SOI wafers for this, but nothing crazy.
- One big issue they pointed out is the sensor bow, which is there even before processing. This might be an issue over the large area sensors.



Plus, there might be sensor 'bow'



Parylene testing (Peter, UW)

- Parylene coating, type N can insulate hundreds of V with a few um
- First tests at UW, first test on dummy pieces, laser and masking to have coating only in some parts of the devices

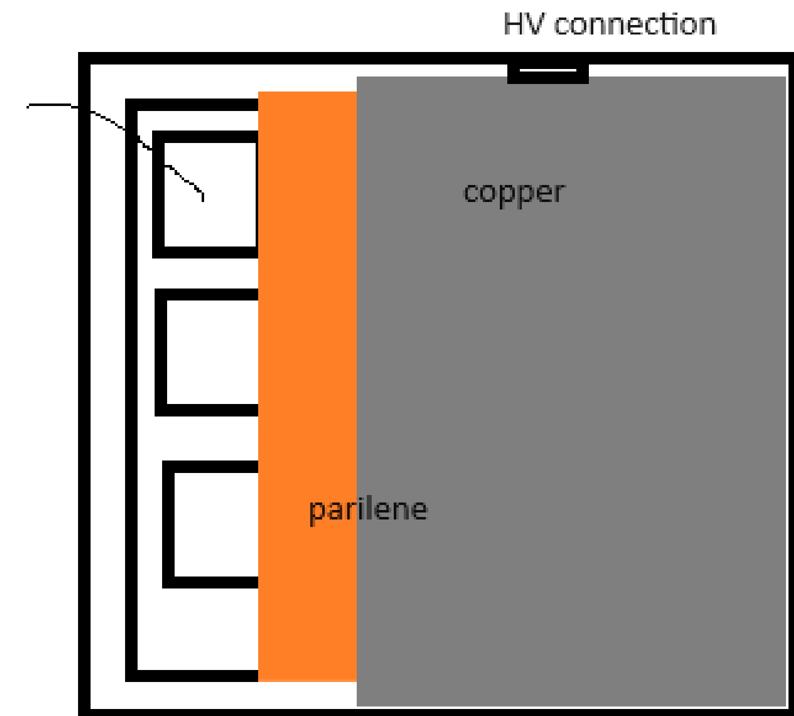
Table 1. Parylene Electrical Properties

Properties	Method	Parylene N	Parylene C	Parylene D	Parylene HT	Acrylic (AR)[a,b]	Epoxy (ER)[a,b]	Polyurethane (UR)[a,b]	Silicone (SR)[a,b]
Dielectric Strength V/mil	1	7,000	5,600	5,500	5,400	3,500	2,200	3,500	2,000
Volume Resistivity ohm·cm, 23°C, 50% RH	2	1.4×10^{17}	8.8×10^{16}	1.2×10^{17}	2.0×10^{17}	1.0×10^{15}	1.0×10^{16}	1.0×10^{13}	1.0×10^{15}
Surface Resistivity ohms, 23°C, 50% RH	2	1.0×10^{13}	1.0×10^{14}	1.0×10^{16}	5.0×10^{15}	1.0×10^{14}	1.0×10^{13}	1.0×10^{14}	1.0×10^{13}
Dielectric Constant									
60 Hz	3	2.65	3.15	2.84	2.21	–	3.3 – 4.6	4.1	3.1 – 4.2
1 KHz		2.65	3.10	2.82	2.20	–	–	–	–
1 MHz		2.65	2.95	2.80	2.17	2.7 – 3.2	3.1 – 4.2	3.8 – 4.4	3.1 – 4.0
Dissipation Factor									
60 Hz	3	0.0002	0.020	0.004	<0.0002	0.04 – 0.06	0.008 – 0.011	0.038 – 0.039	0.011 – 0.02
1 KHz		0.0002	0.019	0.003	0.0020	–	–	–	–
1 MHz		0.0006	0.013	0.002	0.0010	0.02 – 0.03	0.004 – 0.006	0.068 – 0.074	0.003 – 0.006

a. *Handbook of Plastics, Elastomers, and Composites*, Chapter 6, "Plastics in Coatings and Finishes," 4th Edition, McGraw Hill, Inc., New York, 2002.

b. *Conformal Coating Handbook, Humiseal Division, Chase Corporation, Pennsylvania, 2004.*

Test Methods:
1. ASTM D 149
2. ASTM D 257
3. ASTM D 150



Parylene Coating

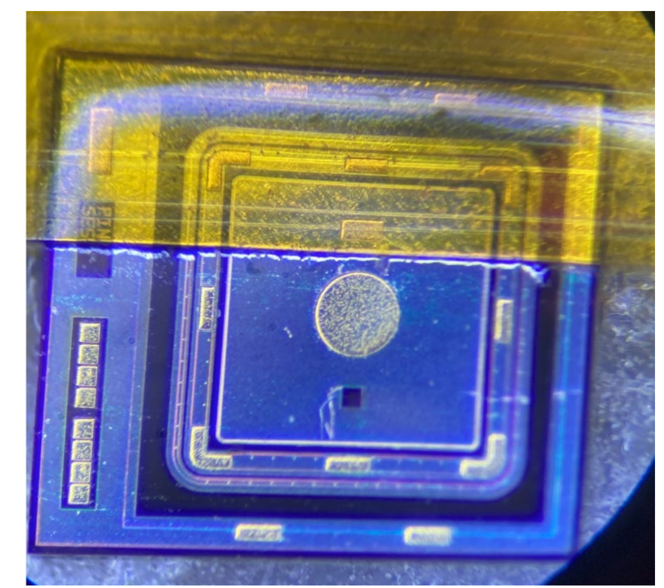
- Marcel applied 5um parylene to copper plates at Washington Nanofabrication Facility
- Tests on the copper plate

First plate

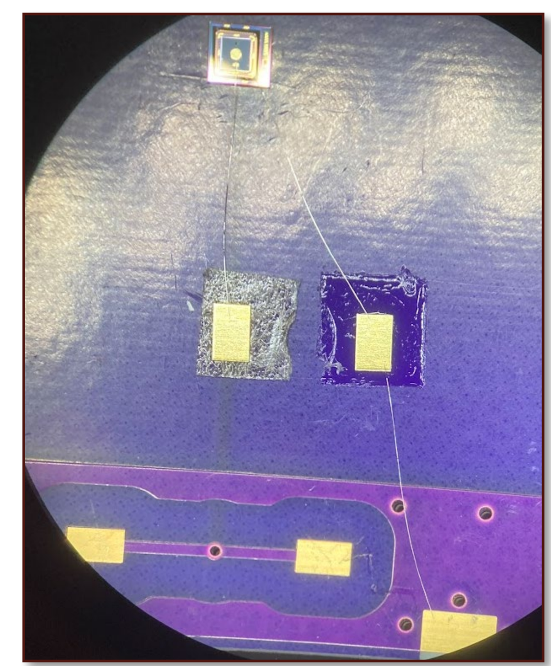
- I placed the parylene covered plate on the bare plate and applied HV with a chamber power supply, with a fast trip. I could reach 500 V, then the HV tripped. Afterwards, it tripped at 400 and then at 350V.

Second plate

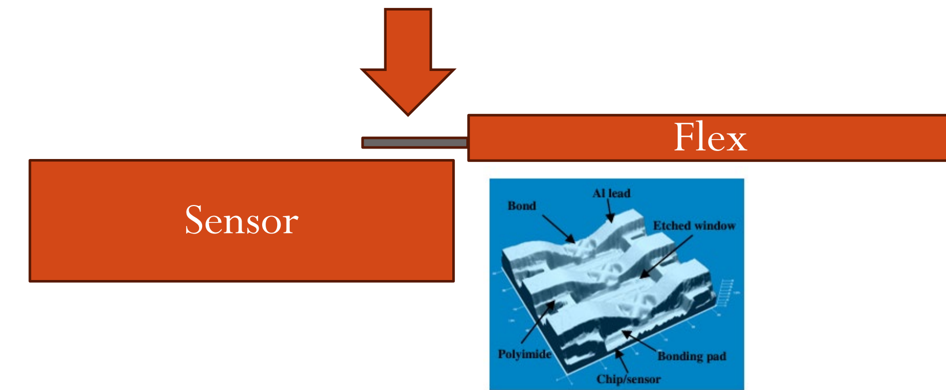
- The 2nd plate was better (with the same bare copper plate). I left it on 500V for 30-40 min, and then ramped up to 800V, at which point it tripped. Afterwards it always tripped at 350V.
- Apparently the spark destroys the parylene cover, leading to lower dielectric strength.
- These are promising results and are reasonable relative to the quoted dielectric strength: 276 V/micron at 25.4microns. Potential poorer performance can be due to our surface roughness. I suggest using 8 um in the future to play it safe.



- Produced boards for parylene coating
  - Example of Theresa’s board
  - Will be coated after I-V test
- Marcel will try photolithography on parylene
  - That would allow selective coverage, no parylene over active LGAD region

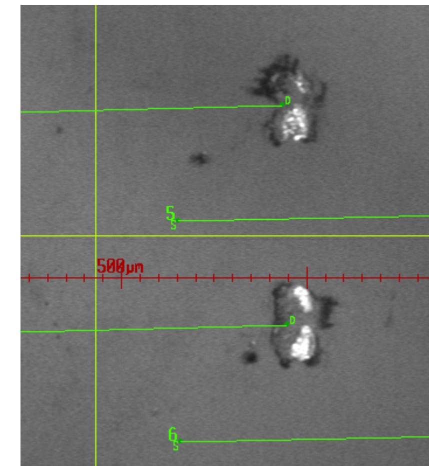


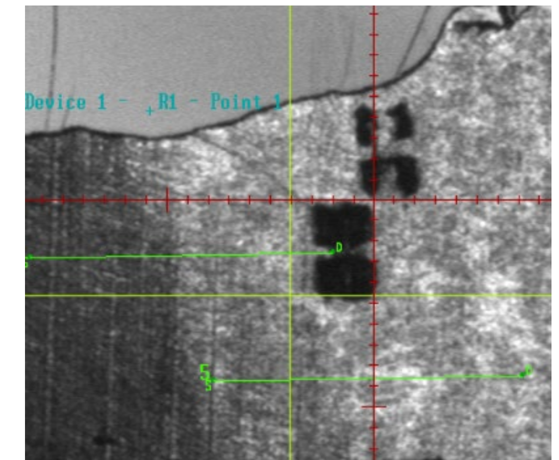
spTAB

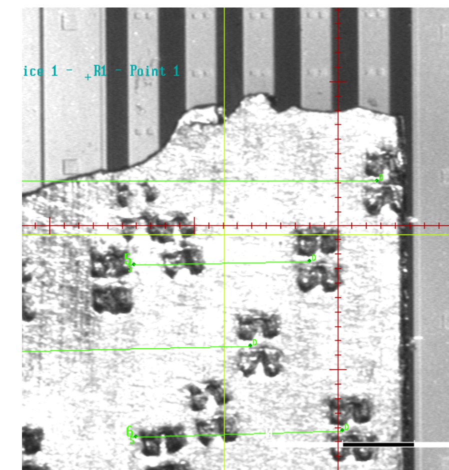


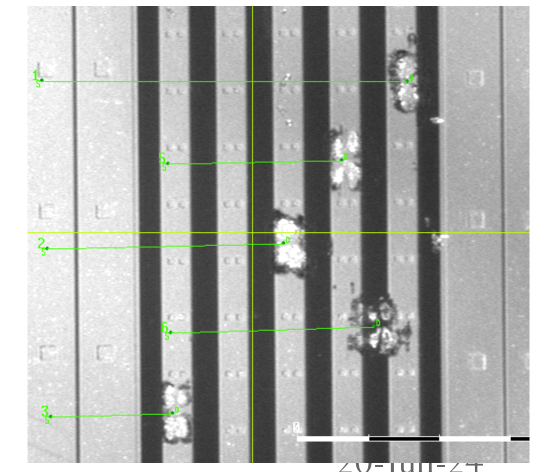
- spTAB instead of wire bonding
  - Pro: no need for wire bonding overhead in the assembly. More mechanical stability of flex on sensor
  - Cons: might be prone to disconnection with mechanical stress

- With a 'cross' large tool, with bonds ~150um X 500um.
  - The tab should be ~25um thick
- Backside:
  - 1 bond pull strength 61g
  - 2 bonds pull 97 g
  - 3 bonds 161g
- Bonding on channels also produced strong bonds
  - 6 bonds = ~250g



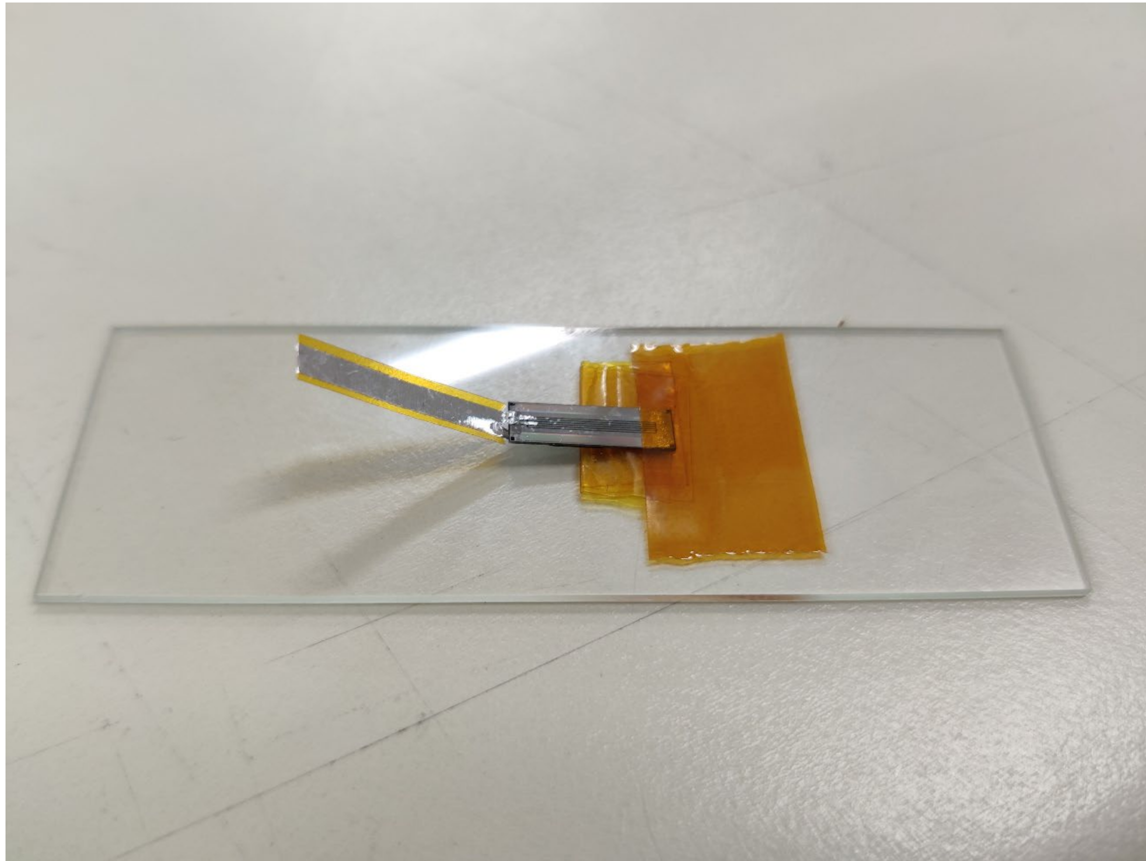


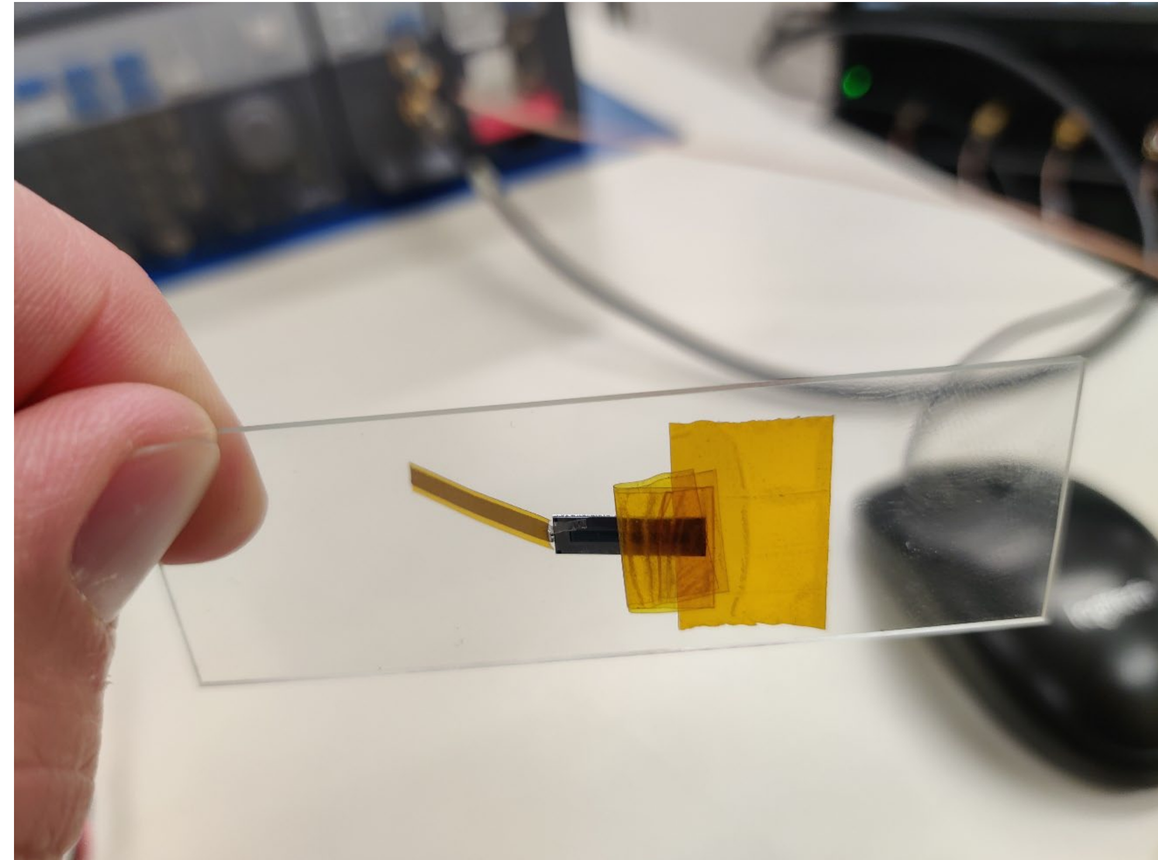




spTabbing tests

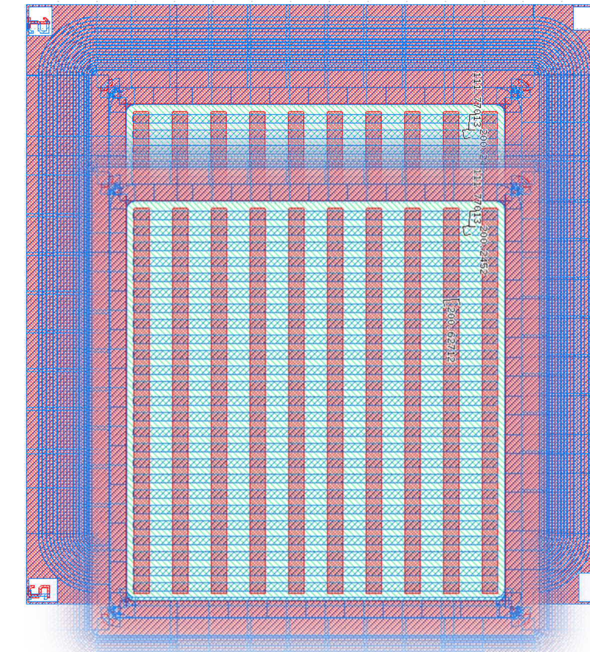
- More realistic tests, connection on both sides on a BNL DS sensor, mechanically quite stable
  - Simulating readout on front and HV connection on the back

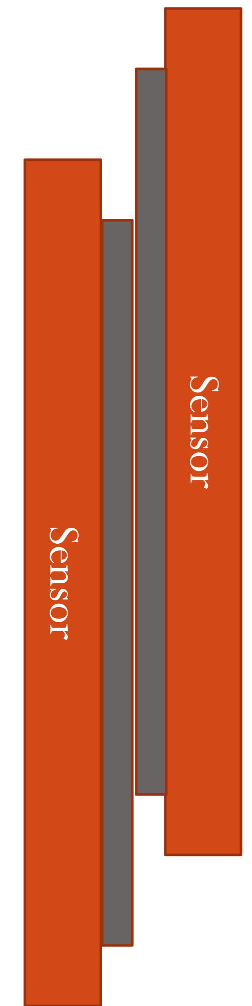


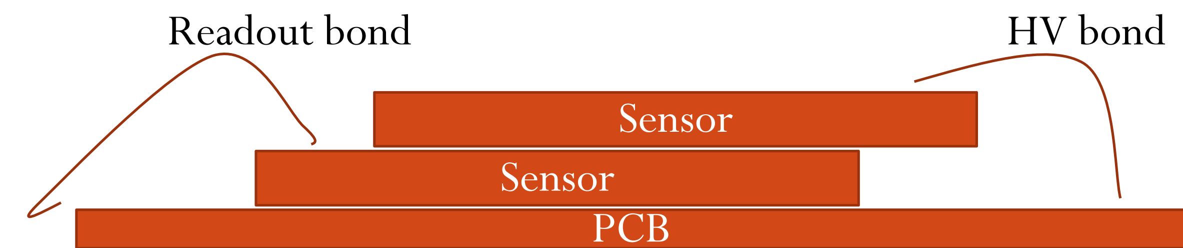


Sensor metal bonding

- Assemble some of the double-sided BNL sensors with M2M bonding
- Anisotropic Conductive Films (ACF) or Paste (ACP)
  - E.g. https://www.dexerials.jp/en/products/acf/paf400.html
  - The samples need to be squeezed together with a 10-100Kg force and heated up to 150-200C for 5-20 seconds.
- ~10um film, ~3um conductor spheres
  - ENIG to increase metal thickness by the right amount (5um each)
  - Likely 10-15um gap
- Other option: gold stud bonds for connection
  - (min ~25um, but it's a starting point)
- Bond the strips with metal bonding or Anisotropic Conductive Films
  - Readout from opening with readout board
  - With 2 sided board we can test both sides



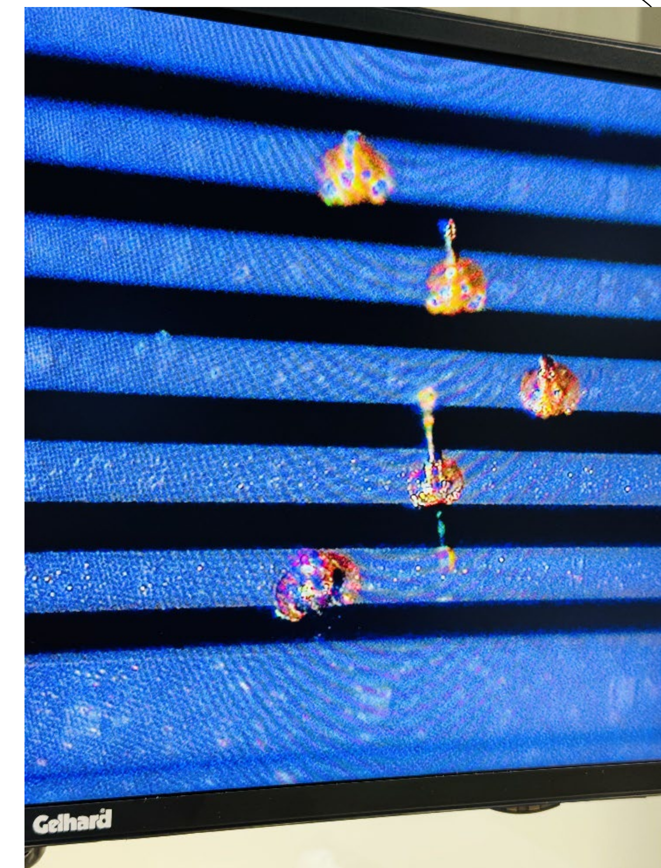




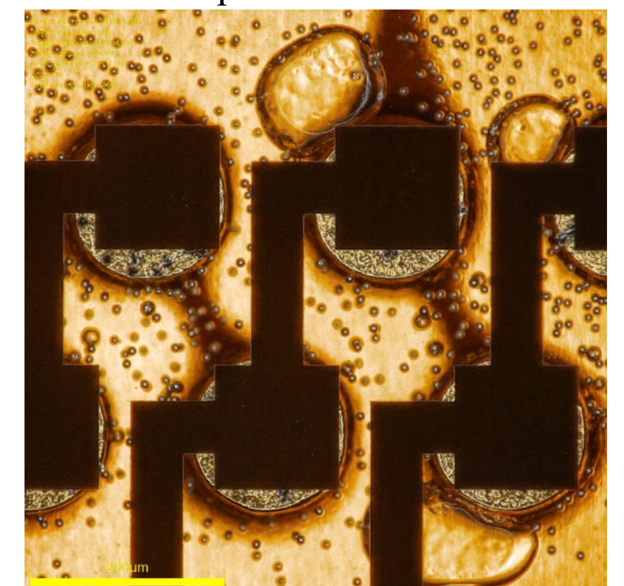
Help from OakRidge/Geneve

- Sent some BNL devices to Oak ridge and UniGe for ENIG and ACP testing
- ACP process tried
  - Electroless nickel immersion gold (ENIG or ENi/IAu) to grow metal for ACF connection
  - 10 μm diameter Ag conductive particles (also 4, 20 and 30 μm silver, or 5 μm Au)
  - The concentration of conductive particles in the epoxy adhesive is 2-5% of the volume ratio
  - The ACP will have 10 μm diameter conductive particles, so the final thickness of the epoxy layer will be <10 μm
- Au studs on a few devices
  - Next will try bonding with an offset to access strips in the inner layer

Gold studs
On BNL device



ACP example



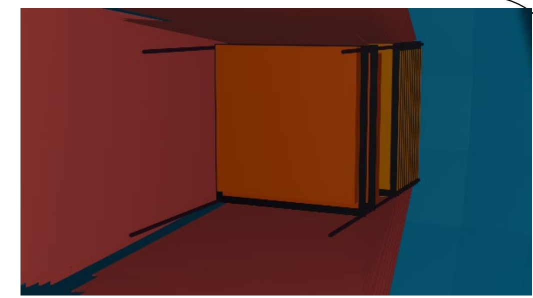
Discussion with T-micro (Yichen, BNL)

- T-Micro bonding technique is with multiple small-size Au balls
- For our application requirements, the proposed bonding materials are 3.5 um Au balls, putting on the bonding surface with lithography
- The bonding is formed with a mechanical press with a heating temperature of 150-200C
- A bonding gap between strips of 1-2 um can be achievable
- The bonding precision with strip-to-strip alignment should be achievable
- For multi-layer bonding with reduced size, T-Micro needs to do some study, an alternative number of layers for single-cell may be necessary depending on the achievable bonding layers.
- T-Micro does not have equipment for doping, the readout chip needs to be provided
- We are going to provide more details about the strip micro-dimensions -In conclusion, T-Micro can deliver the bonding gap < 5 um

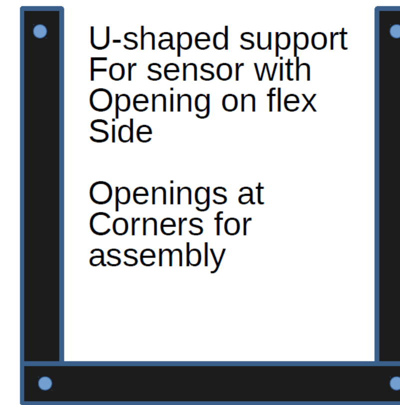
- Other option: Thin Indium biscuit-shape bump with 50-100um diameter with 5-7 um thickness before pressing (Inquiring photos)

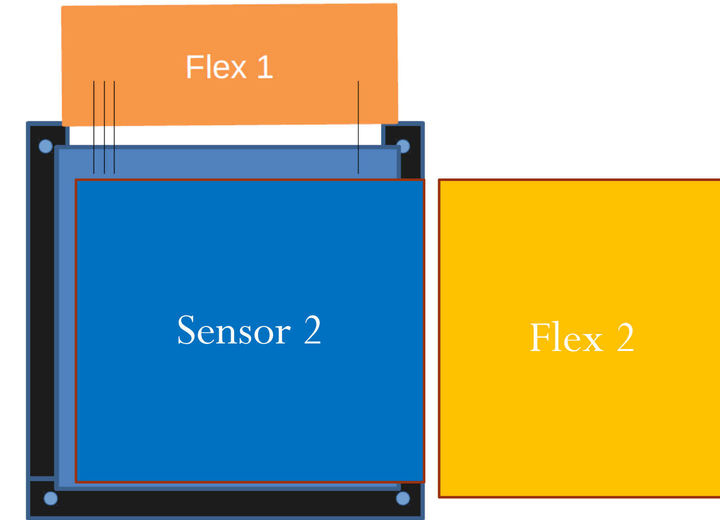
Mechanics support

Old considerations on mechanics support

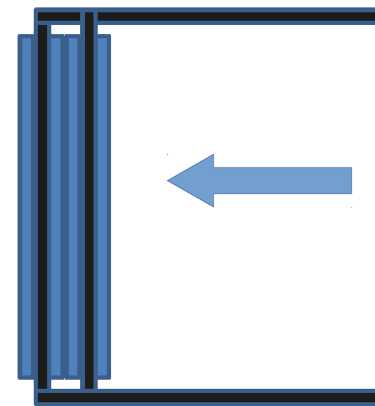


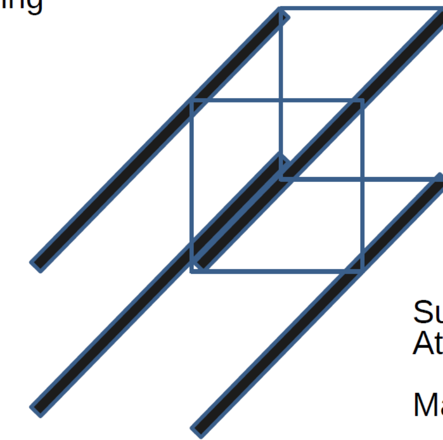
- Old ideas for the mechanics support of the ATAR
- Sensors can be connected on the backside (HV) with a thin conductive glue frame, nominally 25um, could be less without glue
  - Need to study the effect of the sensor 'bow' for thin gaps
  - Also thin gaps will have HV (outside guard ring) close to sensor ground, needs better insulation (parylene)
- The sensors sit on a frame that overextends and has 4 slots at the corners to mount on support "rods"
  - Support is "U-shaped" for the connection of the back sensor (front sensor is exposed)
  - Support can have 'slots' to house the shifted sensors
- Frame each sensor, each 2 sensors or each 4 sensors?
  - A frame for each sensor is easier assembly, but will introduce gaps
  - Opening can only be on one side, so each 4 needs a different design
- Important point is sequence:
  - Connect sensors, then bond 2-4 sides (4 might be hard), have sensor-flex support, then glue to frame.
  - Bonding after assembly is hard or impossible!
- **With this design it might be possible to replace a layer**





Sensor loaded in the staves after bonding

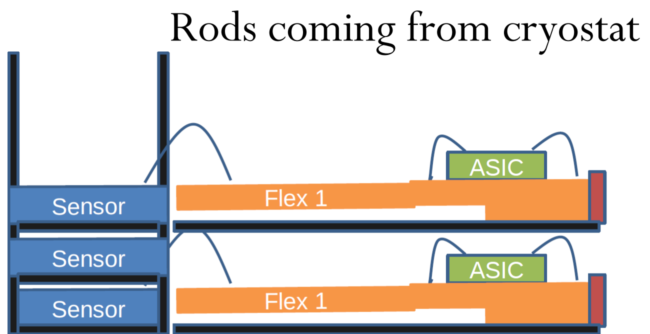




Supported by staves
At the corner

Material: carbon fiber?

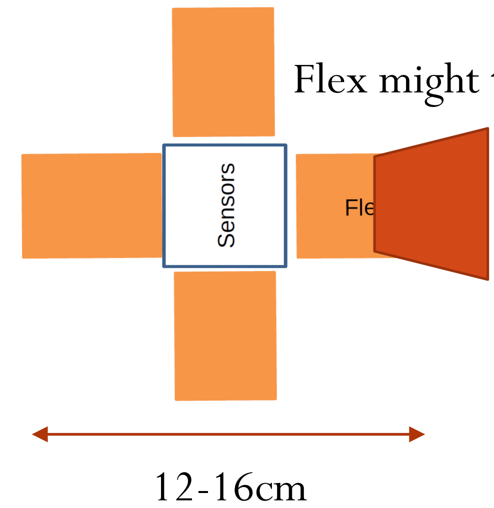
Rods coming from cryostat



Slide all sensor modules in the Staves with temporary support

Flexes are on all 4 sides (simplified in the drawing)

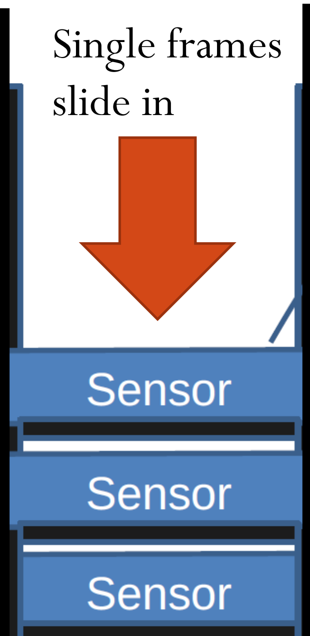
Flex might taper out to reduce cross-talk



Assembled object from the front

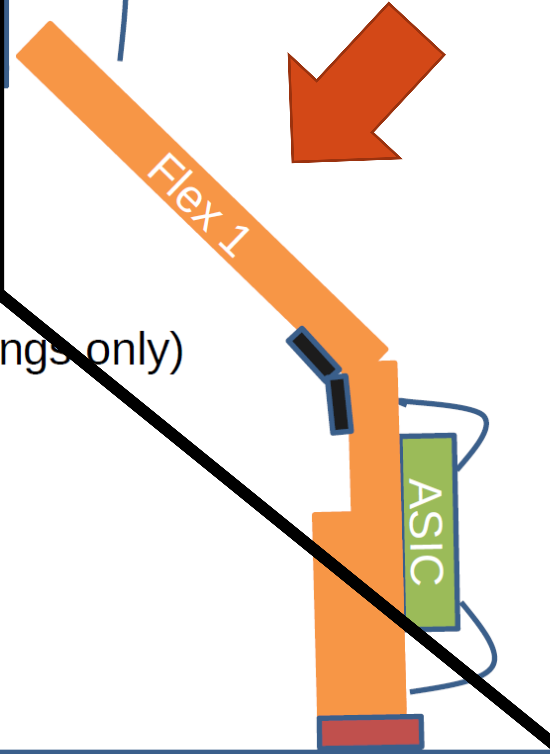
12-16cm

Single frames slide in



The chip is now envisioned on a board
Flex connects to the board

Remove flex support
Bend bonding and flex (or bend bondings only)
Might need flex bending support
Connect to back wheel



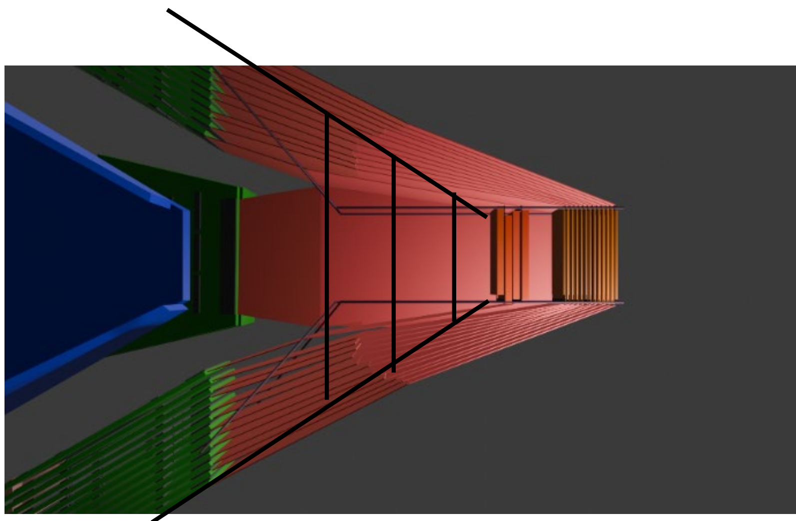
Can Flex connect to board via connector?
“bonded” to the chip on the board and then
Second cable is a connector?

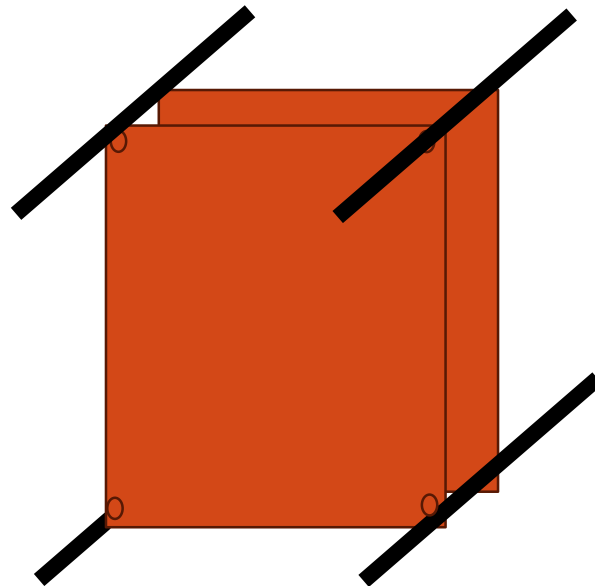
Connect to readout boards one by one

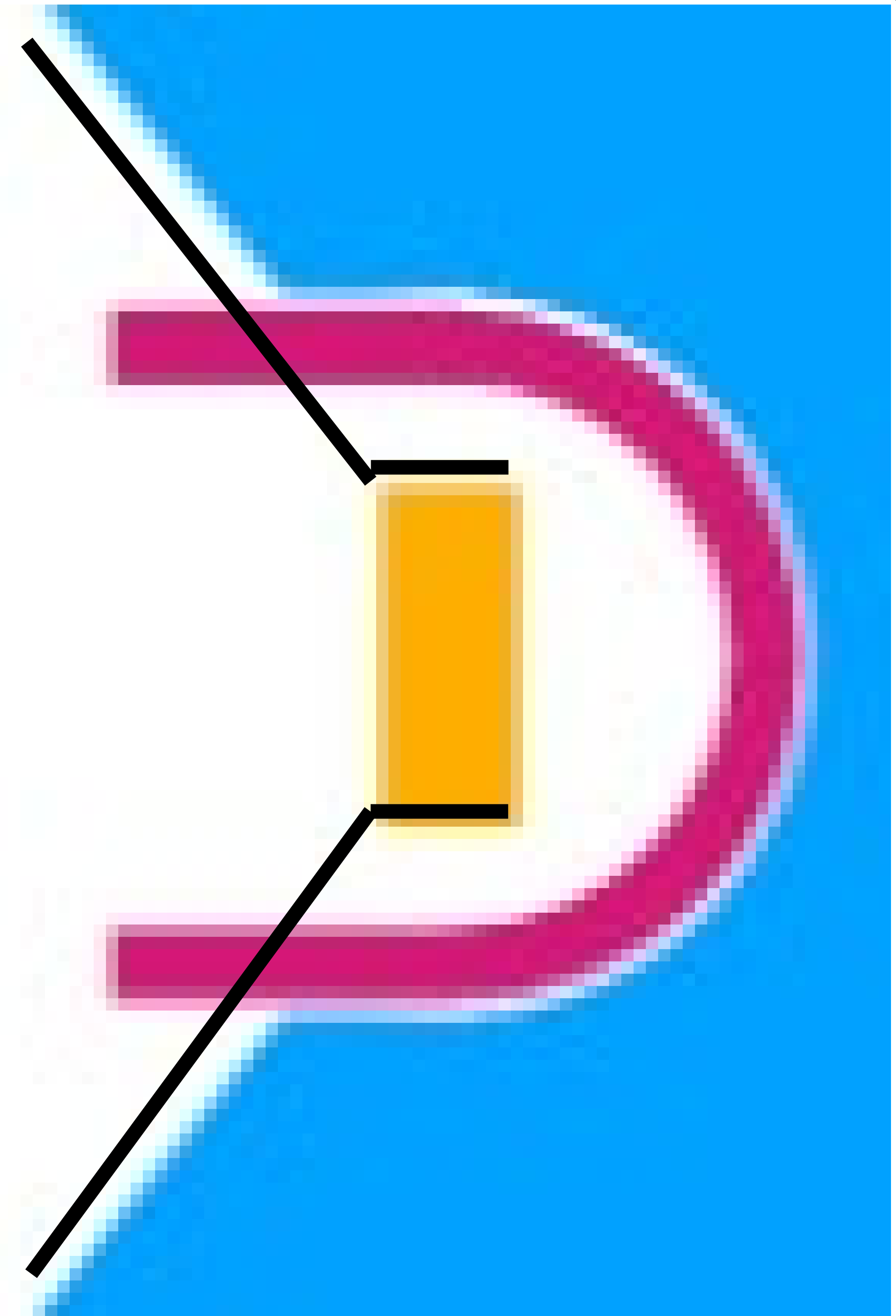
Useful to be able to access and change single ATAR planes

Support

- Could be 4 staves going in with cryostat
- Sensors mounted on a frame support by 4 rods
  - Extra support in between the rods before connecting to cryostat?
- Are the rods enough for rigidity? What is the support/stress provided from the flexes?
- Important to ramp-up effort on realistic mechanics support
  - Need simulation and demonstrator!







Thermal dissipation

Thermal issue

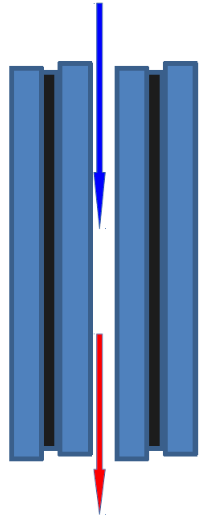
Before irradiation sensor will likely run 300V x nA x 50 →~15 uW for the entire ATAR

After irradiation the current and the voltage will increase due to radiation damage

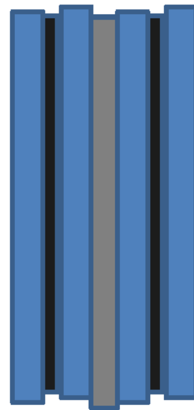
600V x uA x 50 → ~30 mW, < 1mW per layer (this is for PiBeta phase, PieNU might be fine)

Not high, but ATAR is very compact, need to think about heat extraction.
Might need to cool down the sensors (0C might be enough) to decrease the leakage current.

Air flow?

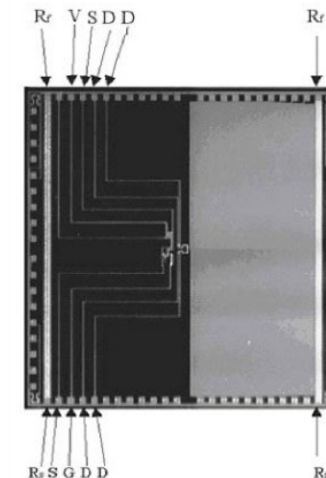


Thermal paste?



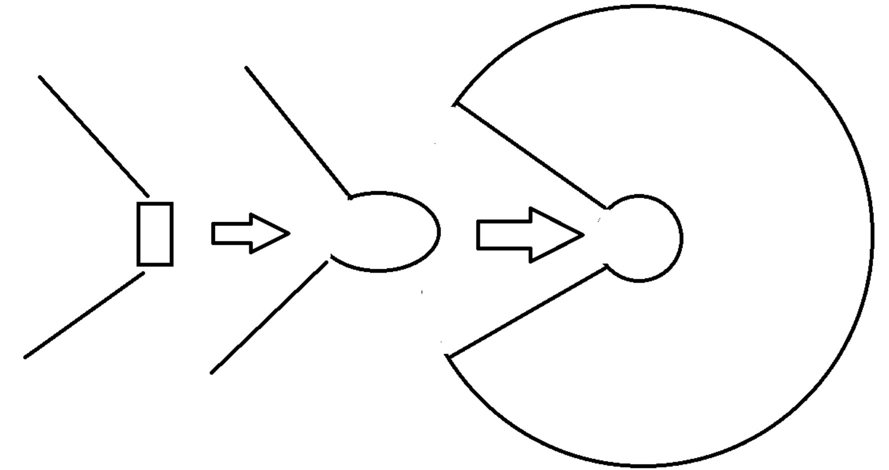
For HGTD we have a thermal budget per chip of 4 W (500mW/cm2), that's with active CO_2 cooling at -30 C

- Simulation of the power dissipation of the current ATAR structure
  - Simulation heat extraction from the support
  - See if air flow is necessary or if it's enough to cool down structures
- Also readout chip will dissipate mWs/ch, simulate if active cooling is needed where readout boards are!
- Build a demonstrator with silicon heater dies
  - E.g. https://www.topline.tv/PST.html
  - Could be expensive! 200$ a piece

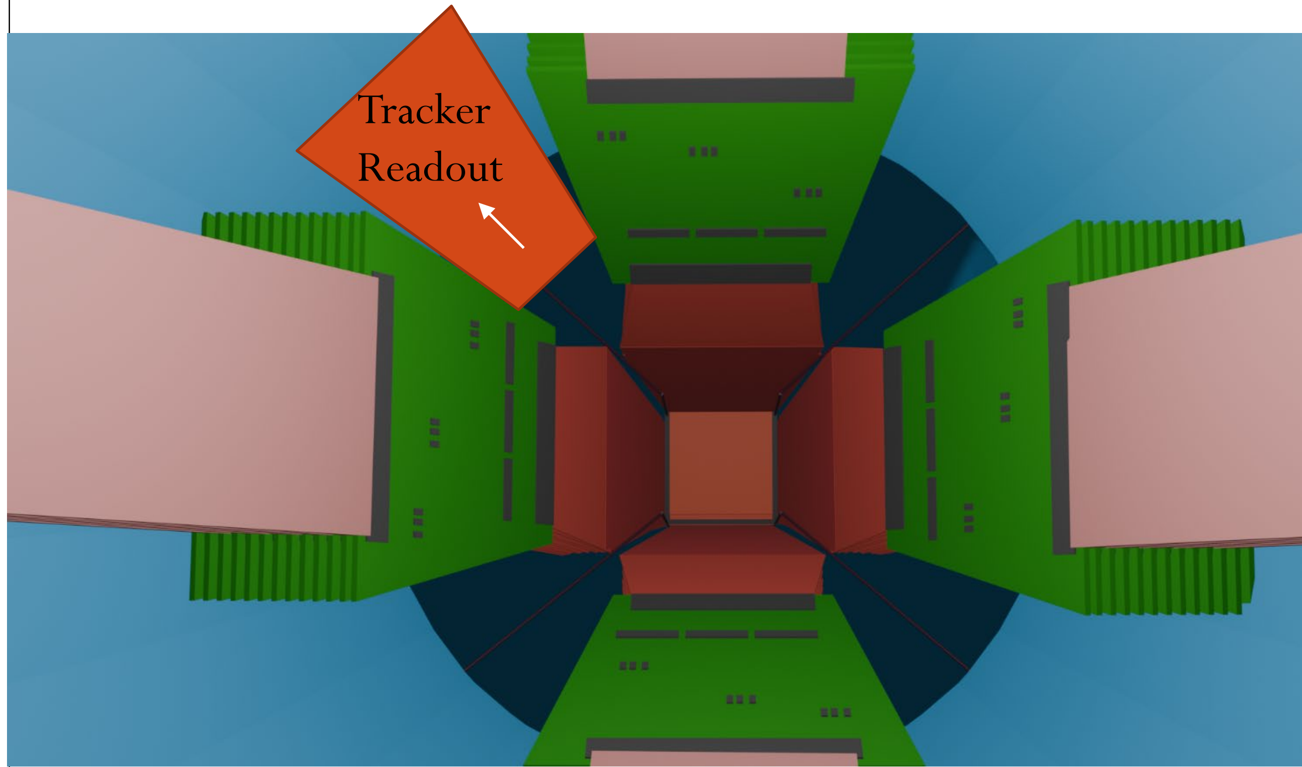


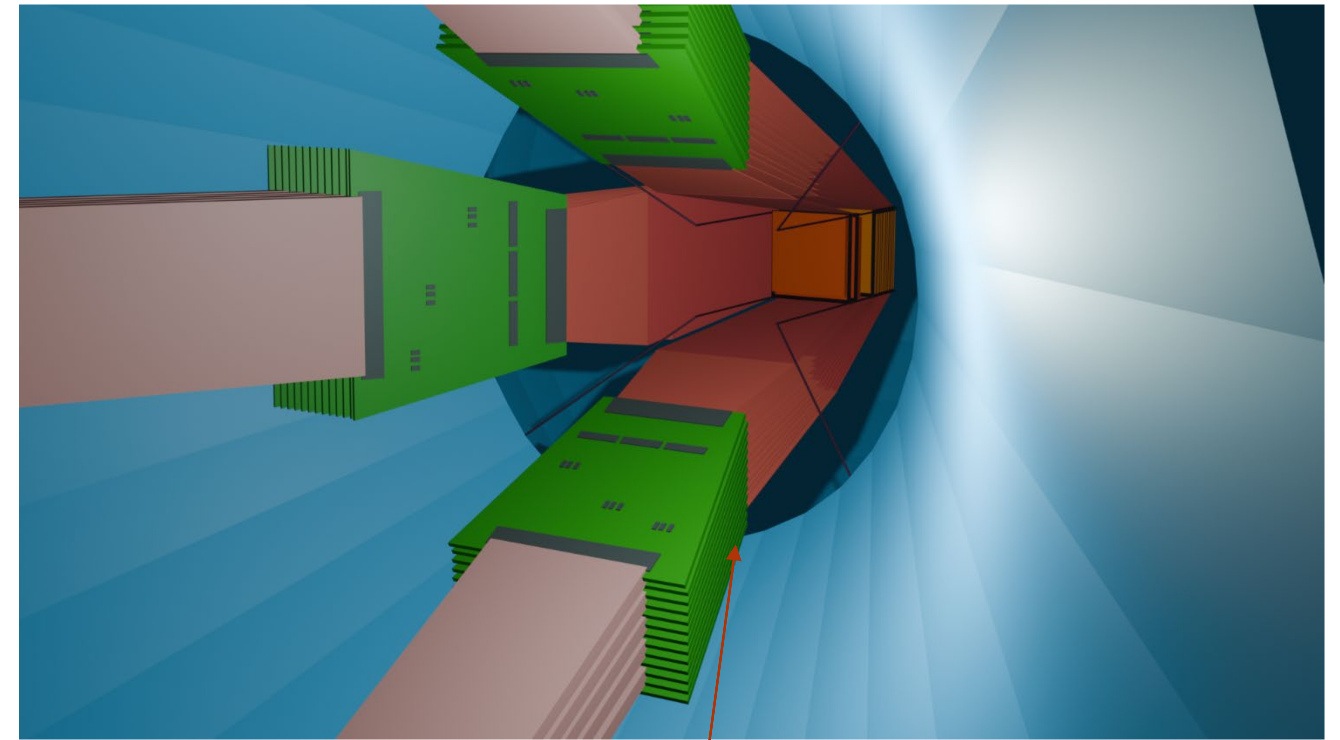
Where does the tracker go?

- Tracker (whatever technology) has to be read out
- If the readout is thin enough it could be behind the FAST boards
- Otherwise it has to be readout in between readout boards
- It has to allow ATAR access and Calo removal, on a different support structure?
- Onion-like support structures on wheels?
  - **Re-alignment is an issue!**



ATAR -> Tracker -> Calorimeter





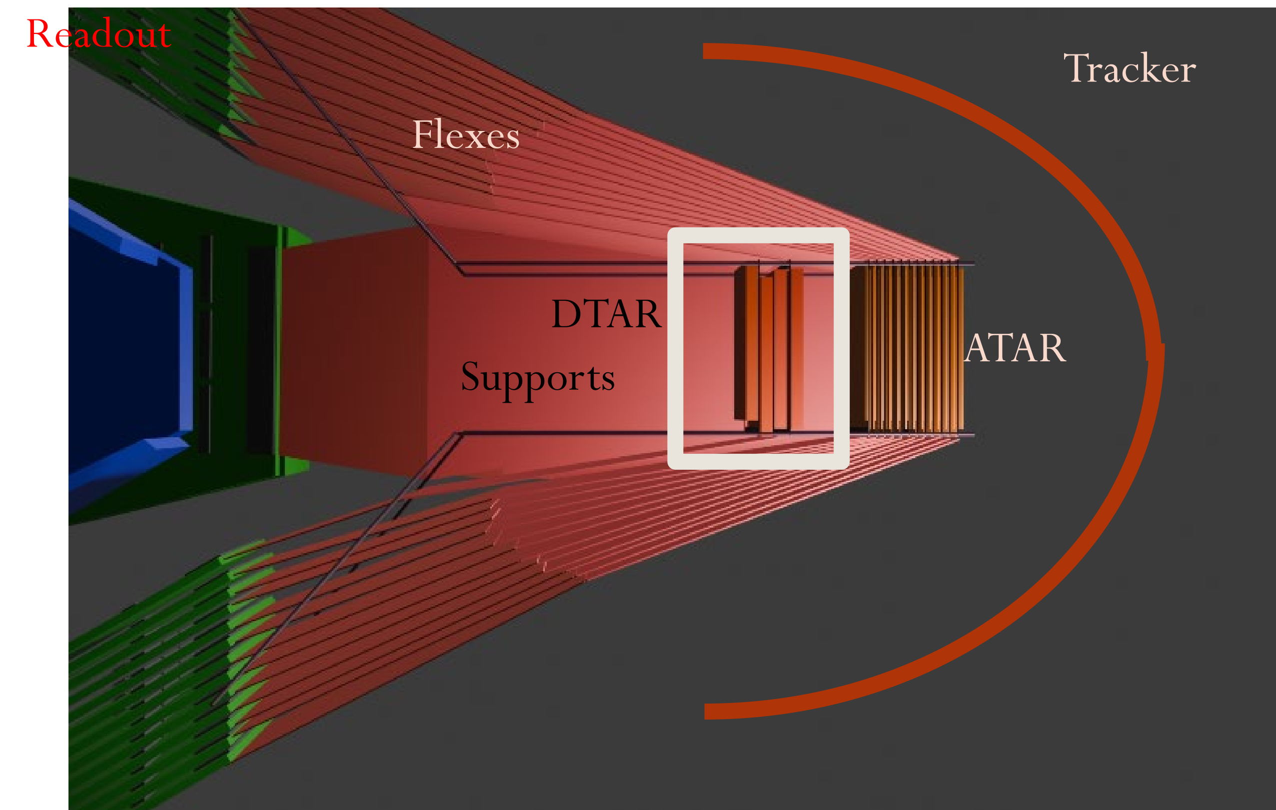
Continuous and behind the boards?

DTAR and Miscellanea detectors

The DTAR

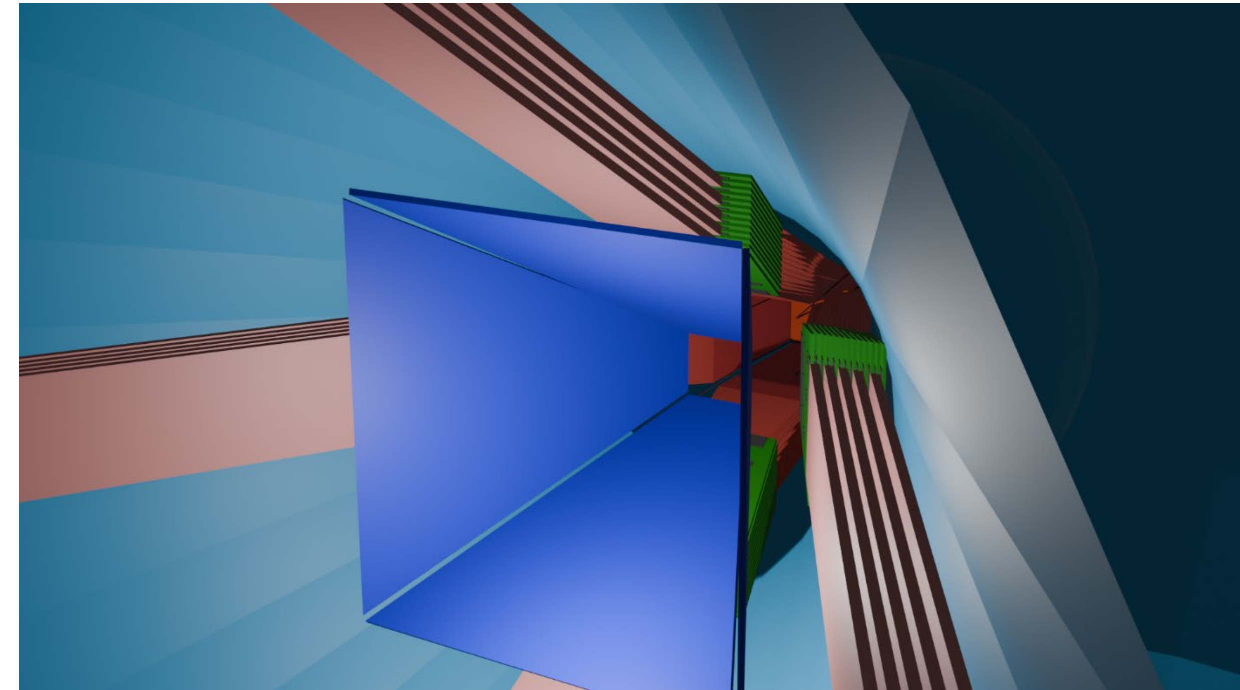
- What do we know about the DTAR
  - Same size of the ATAR and as close as possible to it
  - Has to be several mm to degrade energy, scalable in case we need more degradation!
  - Active detection of pions tracks
  - Energy loss measurement?
  - low granularity (can't afford a lot of channels), need tracking at all?
- Does it have to recognize exiting positrons? Needs timing?

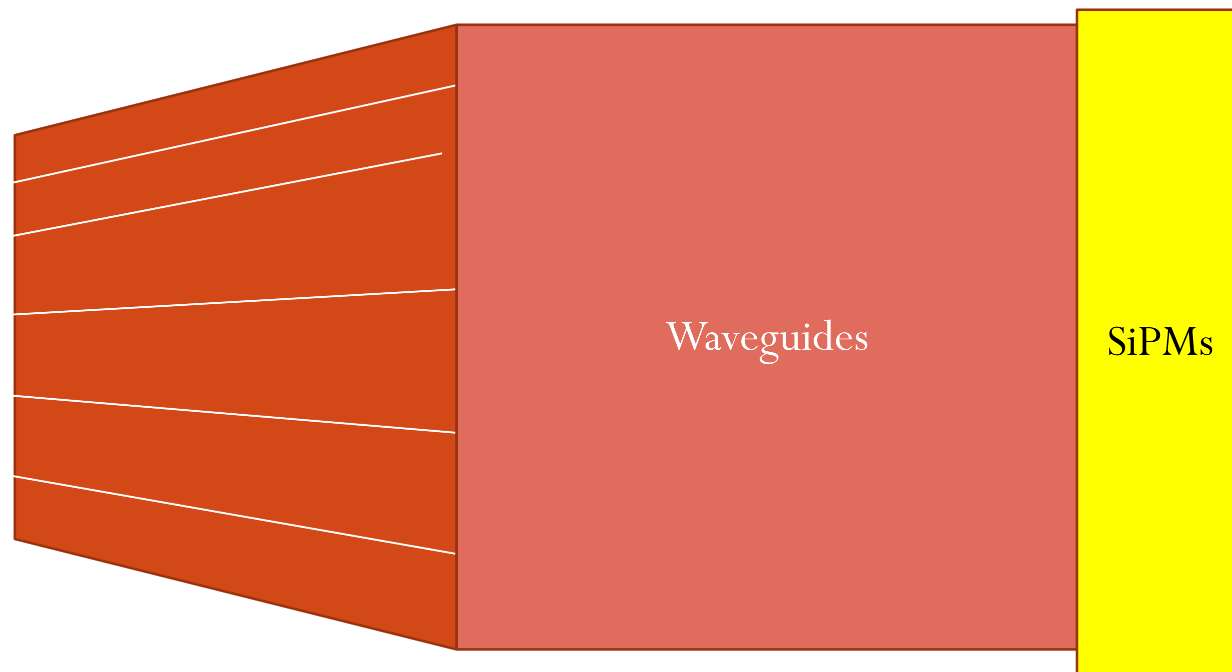
- <u>Example design</u> for 2mm thick:
  - 4 layers of 2x2 cm standard Silicon sensors strips with thickness of 500um
  - Decent track with 2X, 2Y points
  - Could be ok to read out with FAST chips but with lowest gain setting (same readout as ATAR)
  - Total channels 160, same as 1.5 ATAR layers (manageable)
- Or just plastic scintillator with side readout (SiPM?) on all four sides? How critical is tracking? Timing to avoid overlap?
- Thick Se CMOS (or other substrate)?

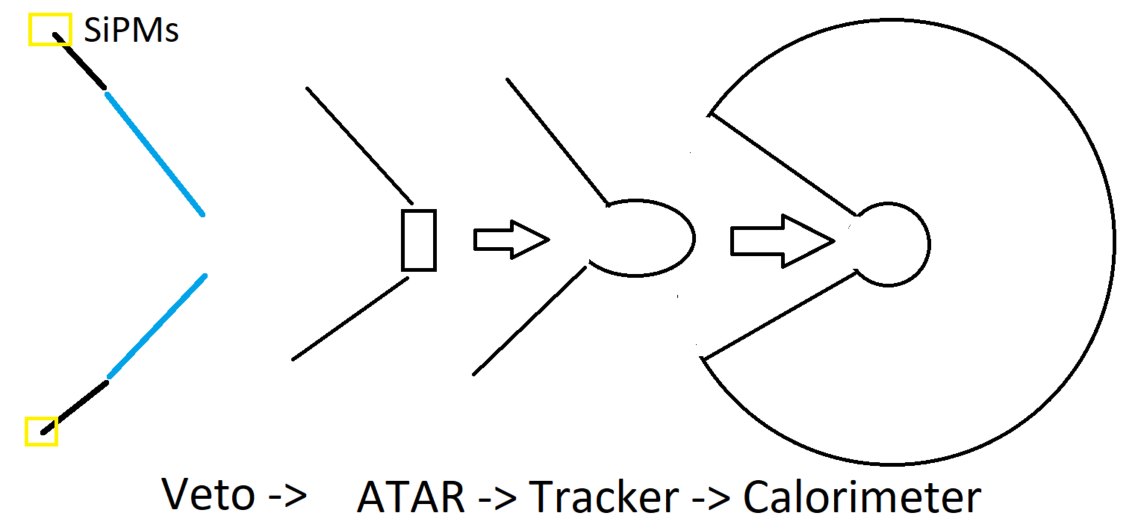


Veto counters

- Plastic scintillators wedged together?
  - With segmented sub-sections
  - Read out with waveguides, SiPM more far away
- Still 'on-wheels' to allow access

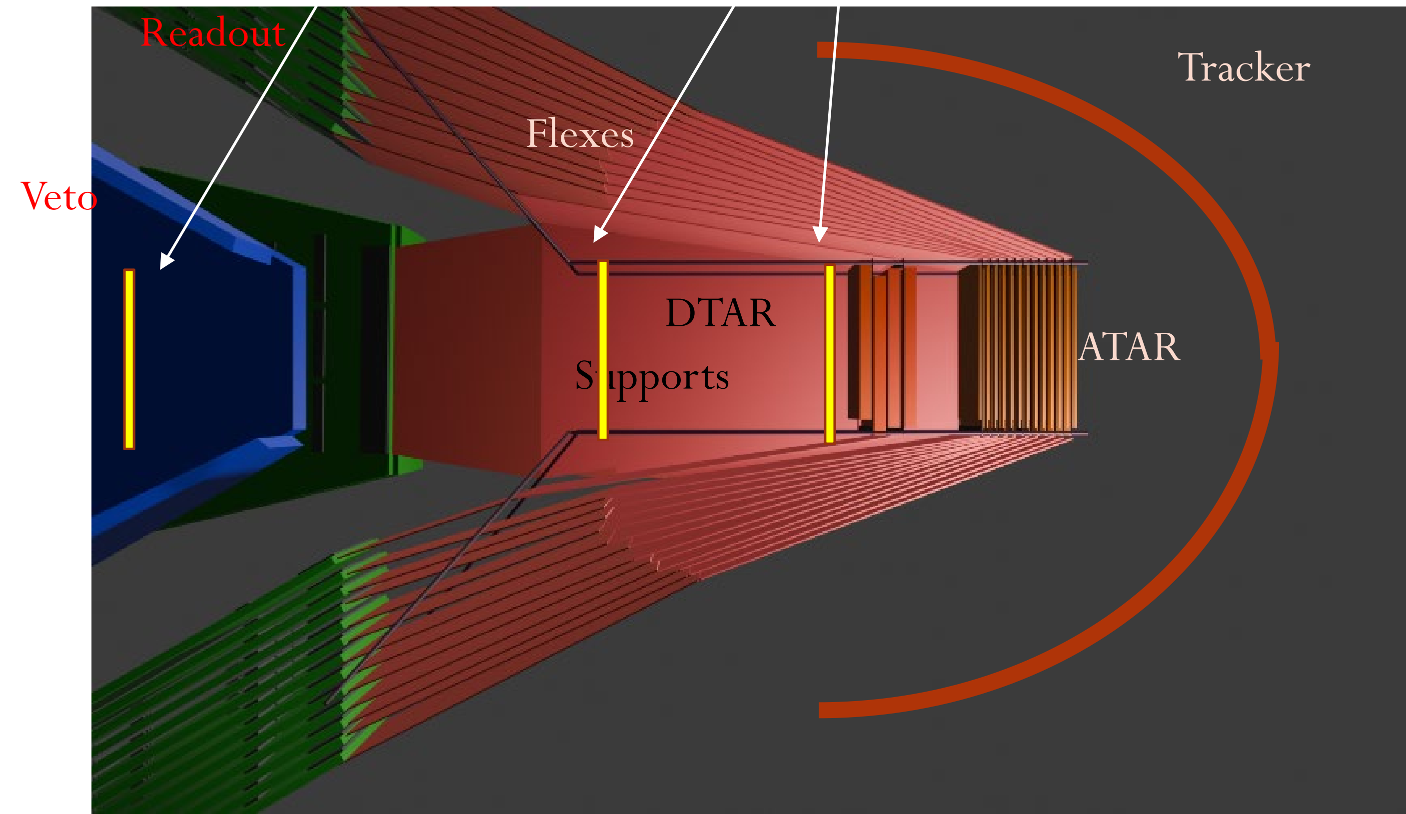


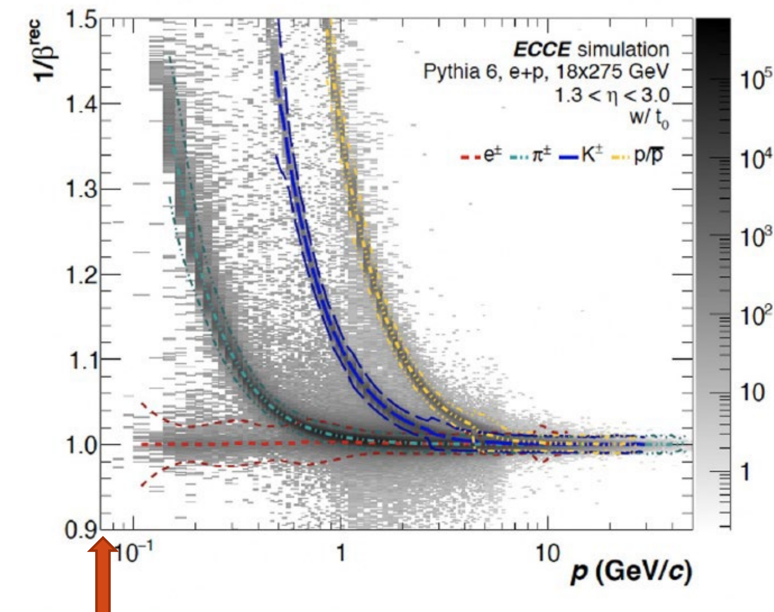




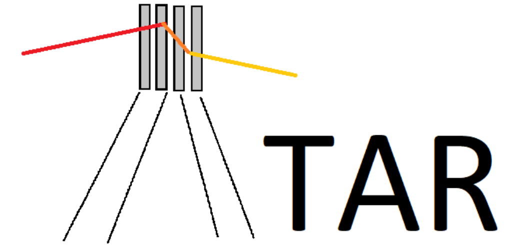
Also a timing layer?

- The addition of a timing layer can help separate beam muons from beam pions by ToF measurements assuming the same momenta
- Could be a simple stand-alone 50um LGAD with no support wafer (or 2 layers)
- Time difference between timing layer and first layer of the ATAR
  - Or between two timing layers
- Need study on distance and timing resolution needed
  - E.g. ePIC, 30ps over 500cm for separation up to a few GeV between Pion (140 MeV) and Kaon (500 MeV)
  - We're much closer but also at much lower momenta!
- Might be interesting to look at as a concept, but can't protect us from 'late' decays (need to assume same momenta)





Conclusions



- Lots of activity ongoing on base assembly and sensor processing
  - Good enough for ATAR v1 in 2026
  - NOT enough for real ATAR
- Need to start thinking about the overall support structure and the thermal load of the object
- Still missing: a realistic DTAR design (needs input on what's needed)
- Still missing: VETOs
- A timing layer could be useful (or not)
- Perfect opportunities for new groups!