DMAPS development at PSI

Hans-Christian Kästli

LTP Seminar

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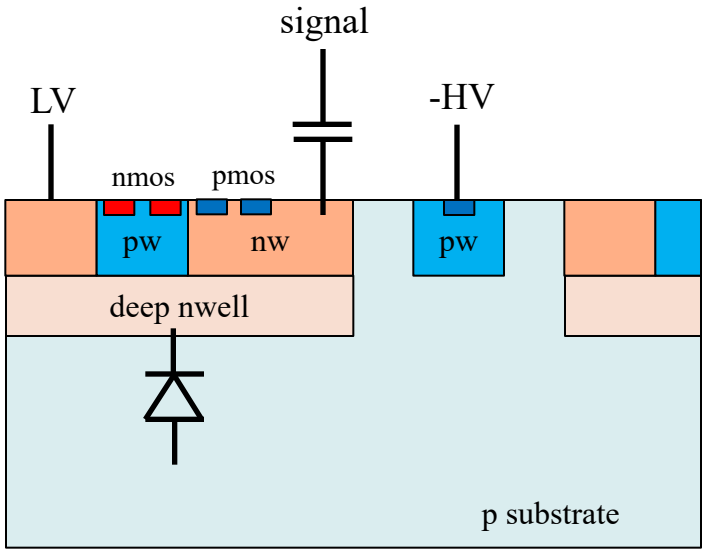
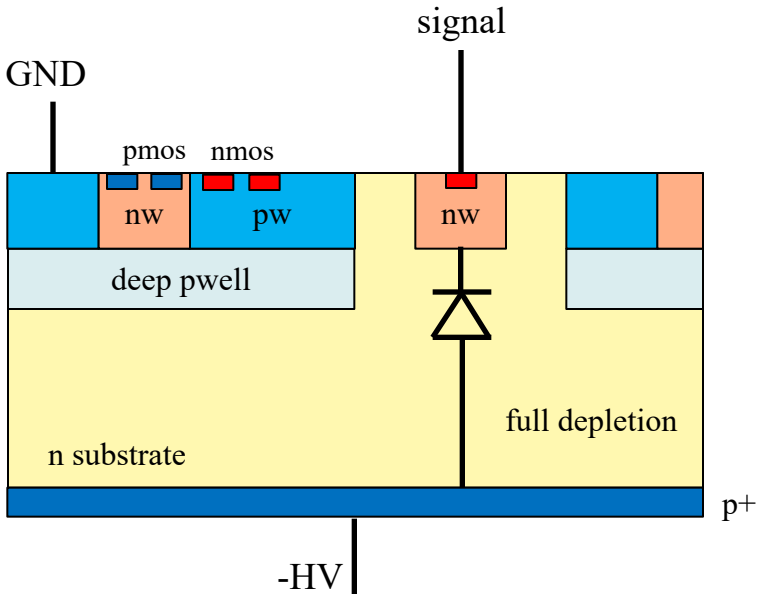
Depleted Monolithic Active Pixel Sensors

- MAPS (non depleted) exist for decades (>1990s) and are with us daily (CMOS cameras)
- Charge collection through diffusion
  - Slow and non homogeneous → not suitable for timing measurement
  - Small charge (charge recombination) → inefficient for MIPs and not radiation tolerant
- Want fast charge collection through drift. Needs an E-field → depletion of the body (DMAPS)
  - Hi resistivity wafers and/or HV process
- Mu3e is the first particle physics experiment using DMAPS sensors. MuPix concept started in 2007 (Peric). Many more upcoming.
- Since then a lot of R&D is going on to increase radiation tolerance, decrease pixel size, reduce power consumption, add timing information…
  - CERN, RD50, Bonn, KIT, INFN, UniGE, Saclay, …
- PSI started in 2020 after finishing CMS layer 1 replacement
  - DMAPS considered to replace hybrid sensors in future in HEP/particle physics
  - A lot of experience in mixed signal design and system architecture
  - Want to make DMAPS available for smaller experiments at PSI or elsewhere

Reminder: DMAPS Types





Large fill factor (area of collection electrode)
Large sensor capacitance
- higher noise, power needs
- slower signals → - for timing

Shorter drift paths → +for timing, + rad hardness
X-talk issues from electronics into collection node

TSI, AMS, LFoundry 150

Small fill factor
Small sensor capacitance
- less noise, power needs
- Fast and larger signals → + for timing

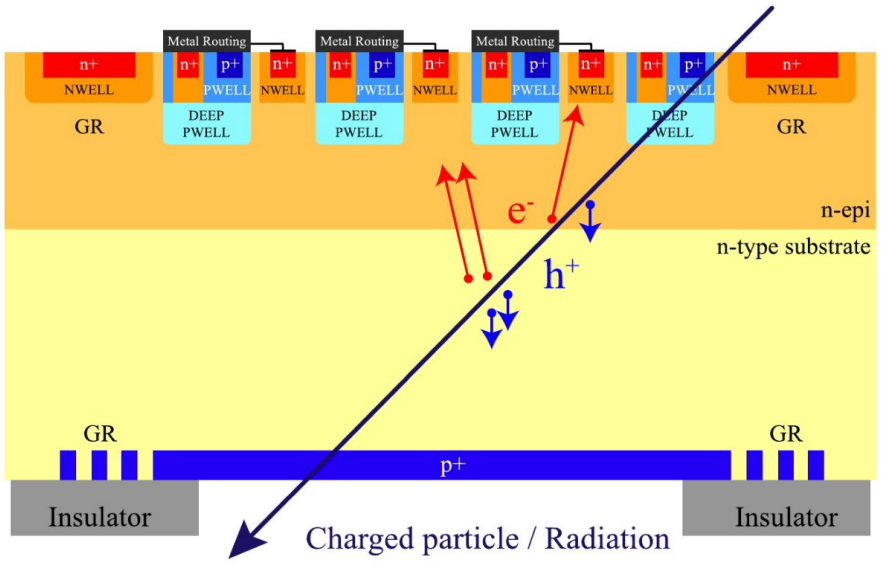
Longer drift paths and low field regions → --for timing, - rad hardness
- Need to find new ways to form fields

LFoundry 110, ESPROS, TowerJazz

Modified LF110 CMOS process

Our first DMAPS design (PhD Burkhalter) → Mothic chip
Small fill factor design
Commercial CMOS process with modification developed by INFN

- n-type substrate
- Deep p-well for isolation
- Backside implant for biasing



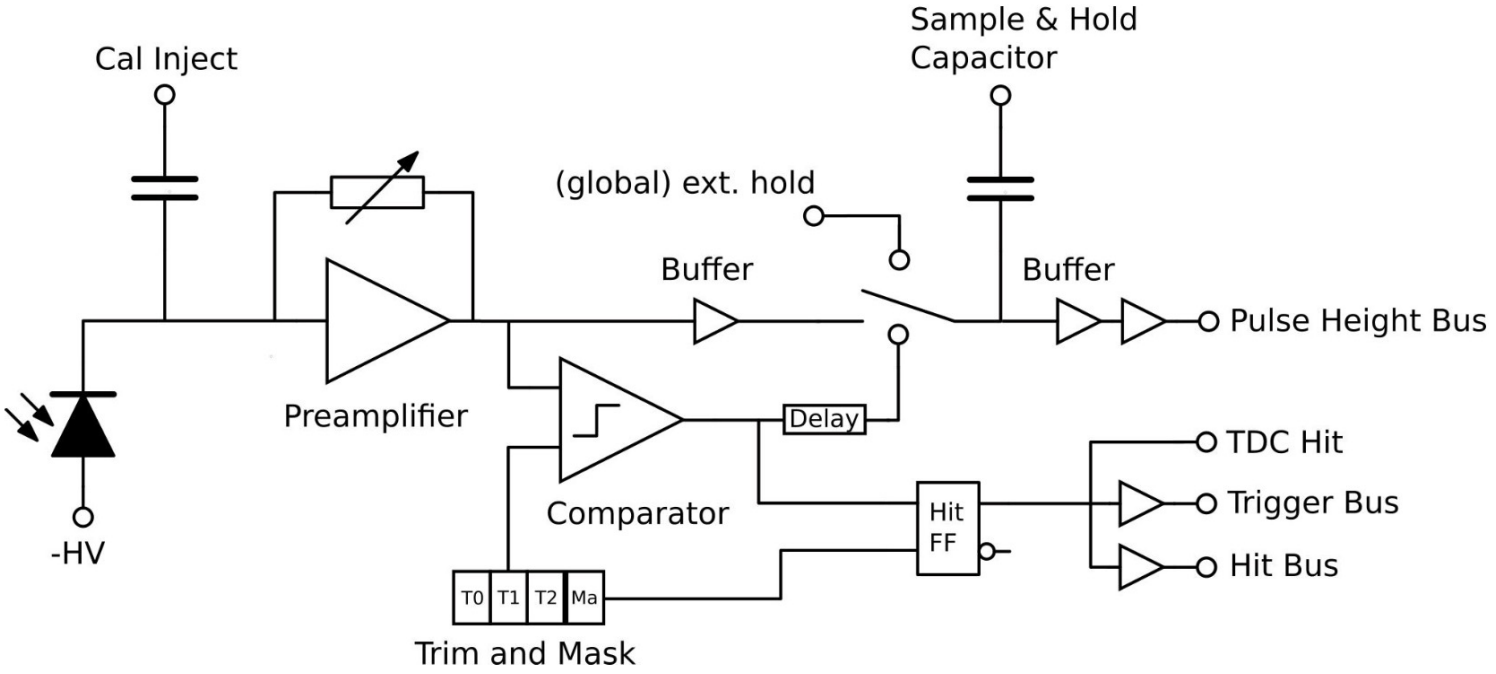
Pro:

small pixel size (50um)
Low cost development
(submission shared with INFN)

Con:

Not fully disclosed
Collection node and guard rings designed by INFN

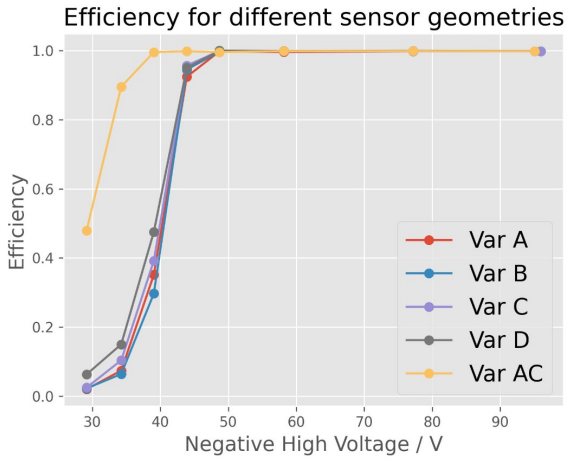
Pixel Cell

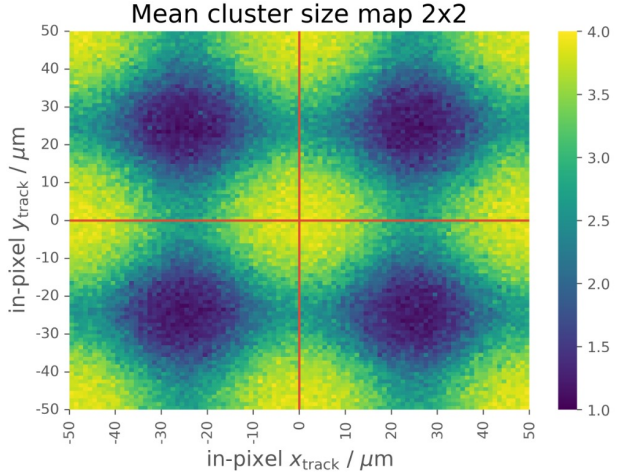


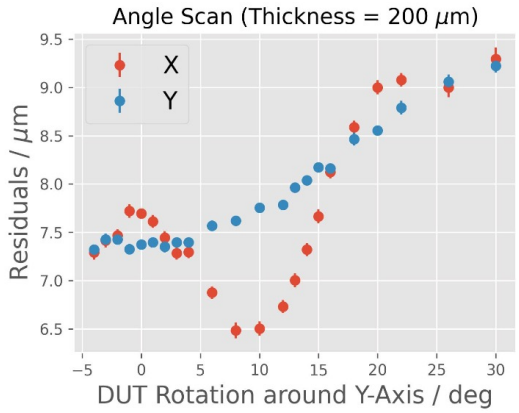
One TDC for group of 4 pixels

- No space for TDC per pixel
- Need only time per cluster anyway

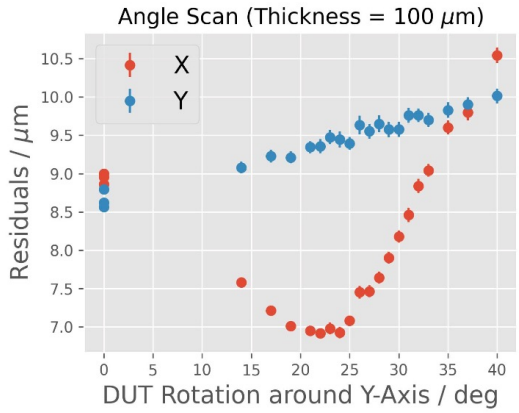
Beam test results (DESY)



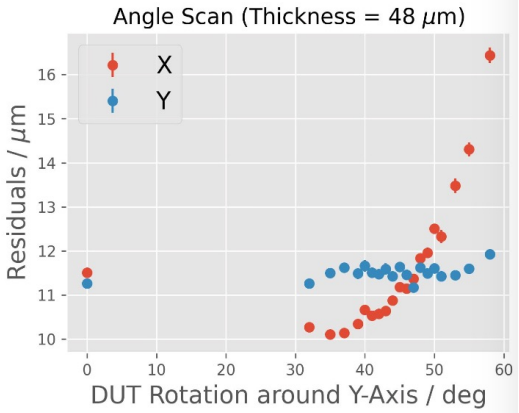




(a) 200 µm

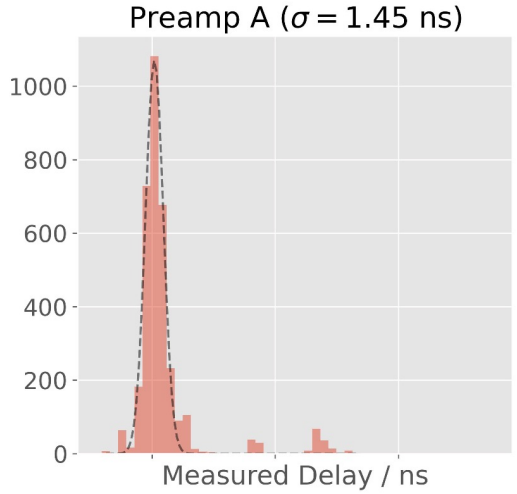


(b) 100 µm



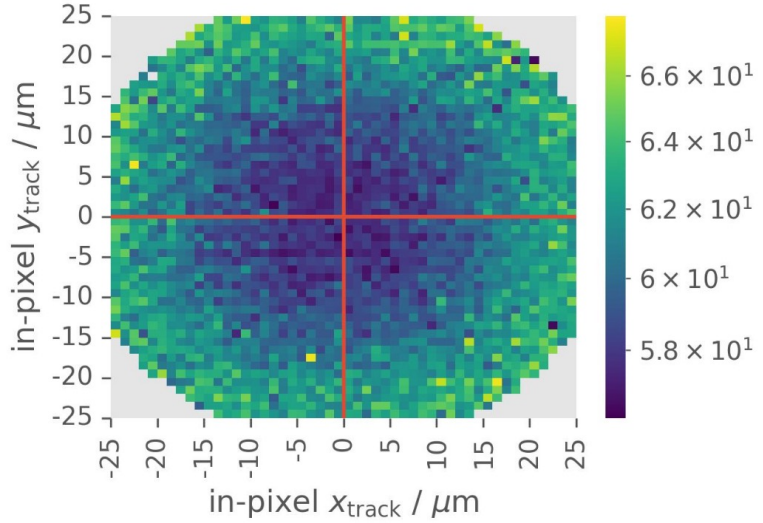
(c) 48 µm

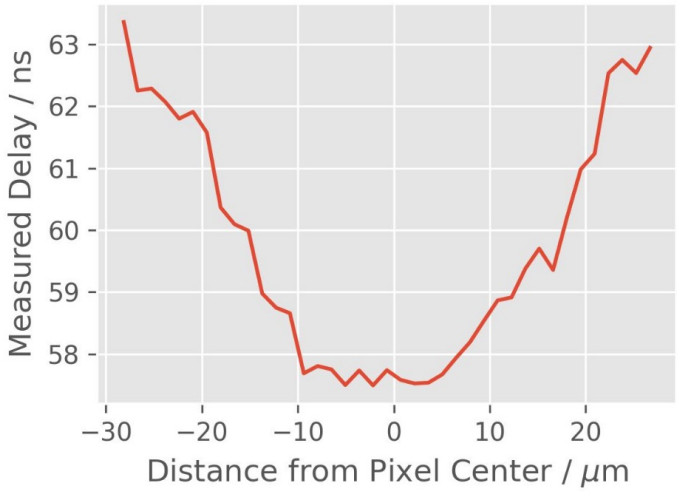
Time of arrival



First full DMAPS chip with small pixels and ToA measurement

General problem of small fill factor designs:
Non uniform fields and drift paths give rise to time walk
Can correct for that, but need tracking with sub pixel resolution





Large fill factor design in TSI

In parallel we started a design with large fill factor

The chosen technology was TSI 180 nm (HV process, same as MuPix)

Can operate in partial depletion (depletion from front)

Prototype run shared with KIT

p-iso-well is not standard in this techonolgy (p-MOS transistors)

P-substrate, resistivity ~370 Ωcm (spec)

20 × 20 pixels

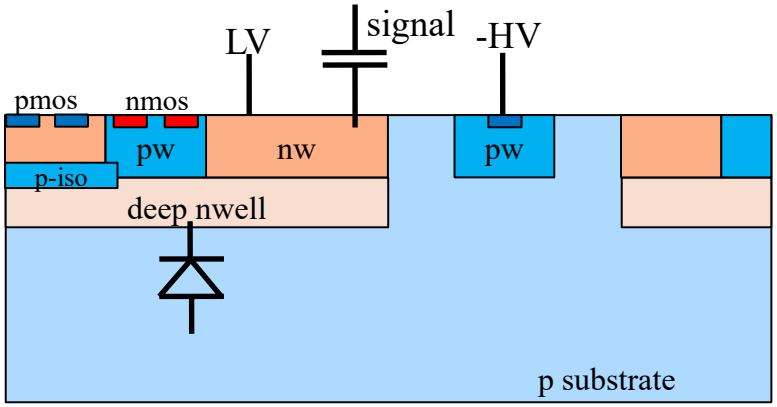
Pitch: 50µm × 100 (150) µm

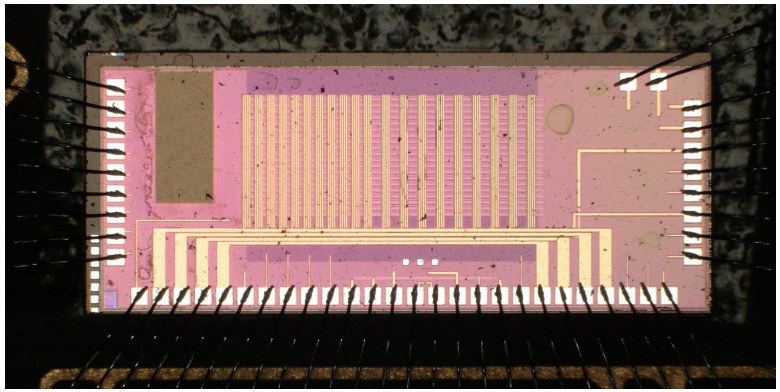
4 bit trimmable discriminatiors in each pixel

Very basic design with full frame readout

Narrow timetable:

- Submitted 05/2022
- Wafers received 12/2022
- Diced (and thinned) chips received 05/2023
- Test beam 06/2023





Sensor and frontend response

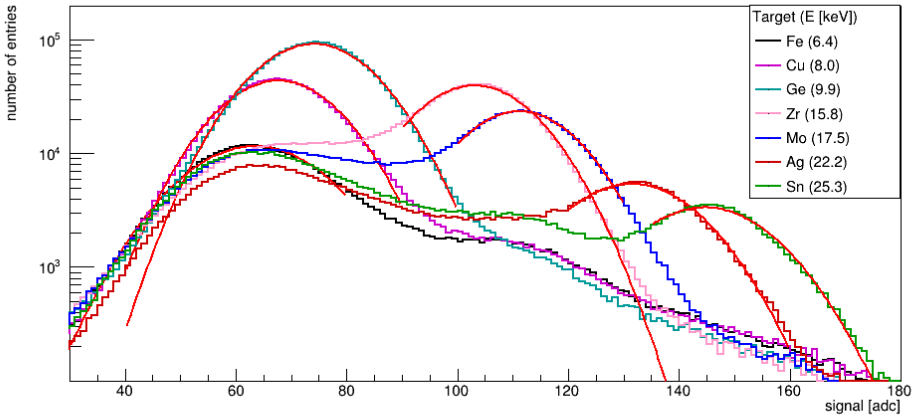
Sensor verification in X-ray box with fluorescence targets at different energies

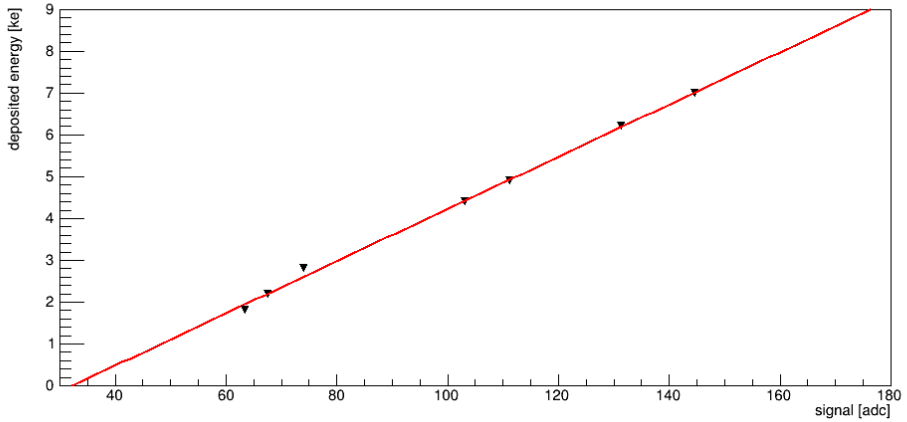
- Can clearly see Cu line
- Even Fe line, but likely the spectrum is cut into with the threshold → promising

We also took it to the DESY testbeam together with the Mothic chip

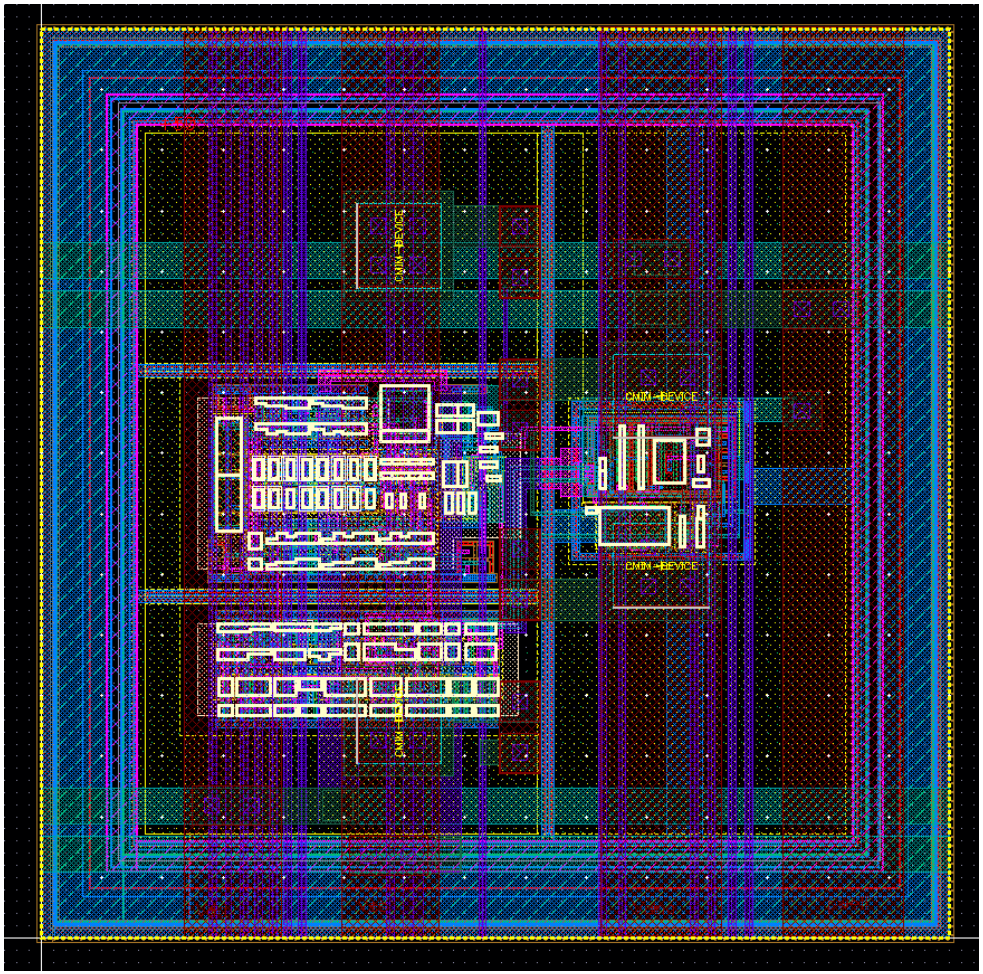
- a lot of X-talk issues observed. Found operational tricks to partially mitigate. But low data rates
- Analysis of efficiency and spatial resolution not finished. But data quality is insufficient. Chip was not understood good enough
- But clearly understood X-talk mechanisms and hence learned very valuable lessons for future designs

While planning next beam time and next iteration of design TSI went out of business on short notice in 11/2023





MAPSI 2nd iteration (→stopped)



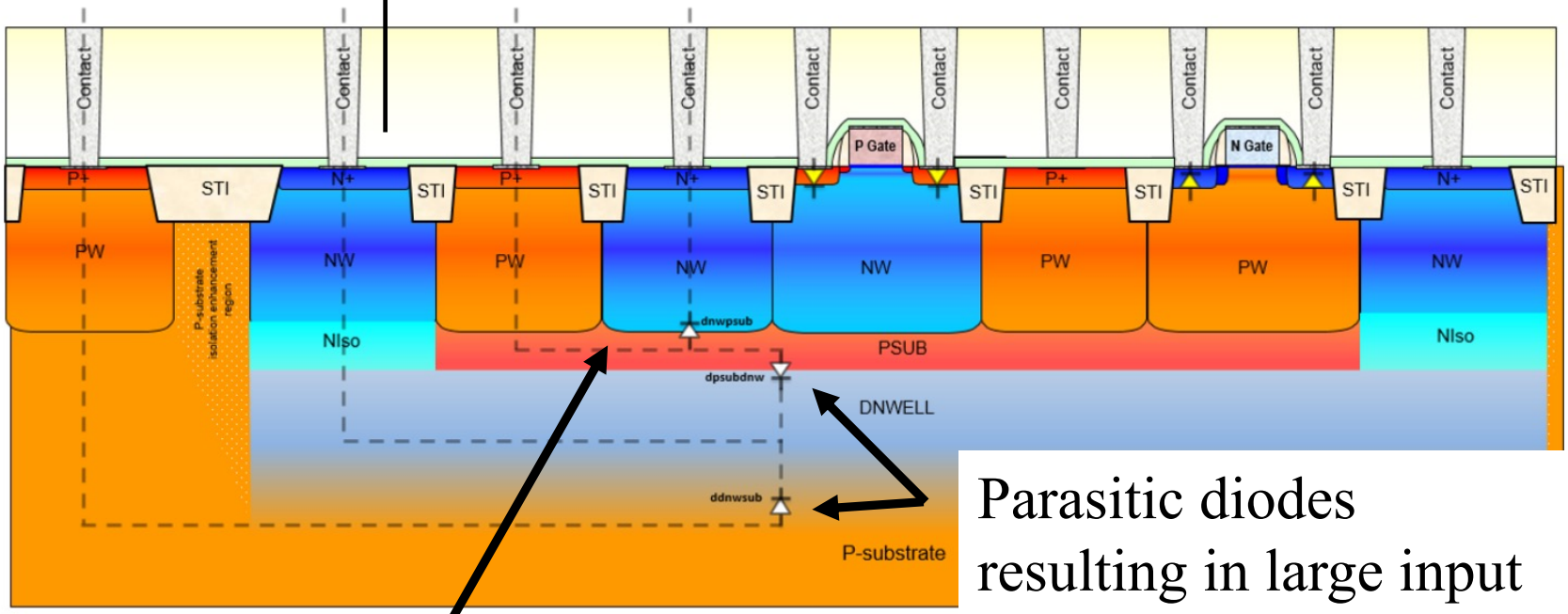
- 75um x 75um pixel
- Discriminator with global threshold and 4 local trim bits, mask bit
- Sample & hold circuit with hold delay
- Injection circuit with pixel wise selection
- Column length: 250 pixel, ~1.9cm
- Final chip will be ~2x2cm^2
- TDC per column
- Global (digital) chip simulation and readout definition ongoing

Translation to LF150

- TSI went out of business end 2023
- AMS (fully compatible to TSI) would produce it for the time being
  - NDA signed with them
  - No PDK available yet. Will not submit a design without full simulation in original PDK
  - Unclear how the availability is in the future
- Looked into LF15A
  - Very similar process
  - Used by RD50, Bonn: Monopix, Paris: Cactus
  - Only one MPW this year.
  - Needed fast decision and translation of TSI design
  - Prepared it in 4 months: but again first time submission from us. Some question marks. No large area chip, need some experience first in MPW.

LF15A

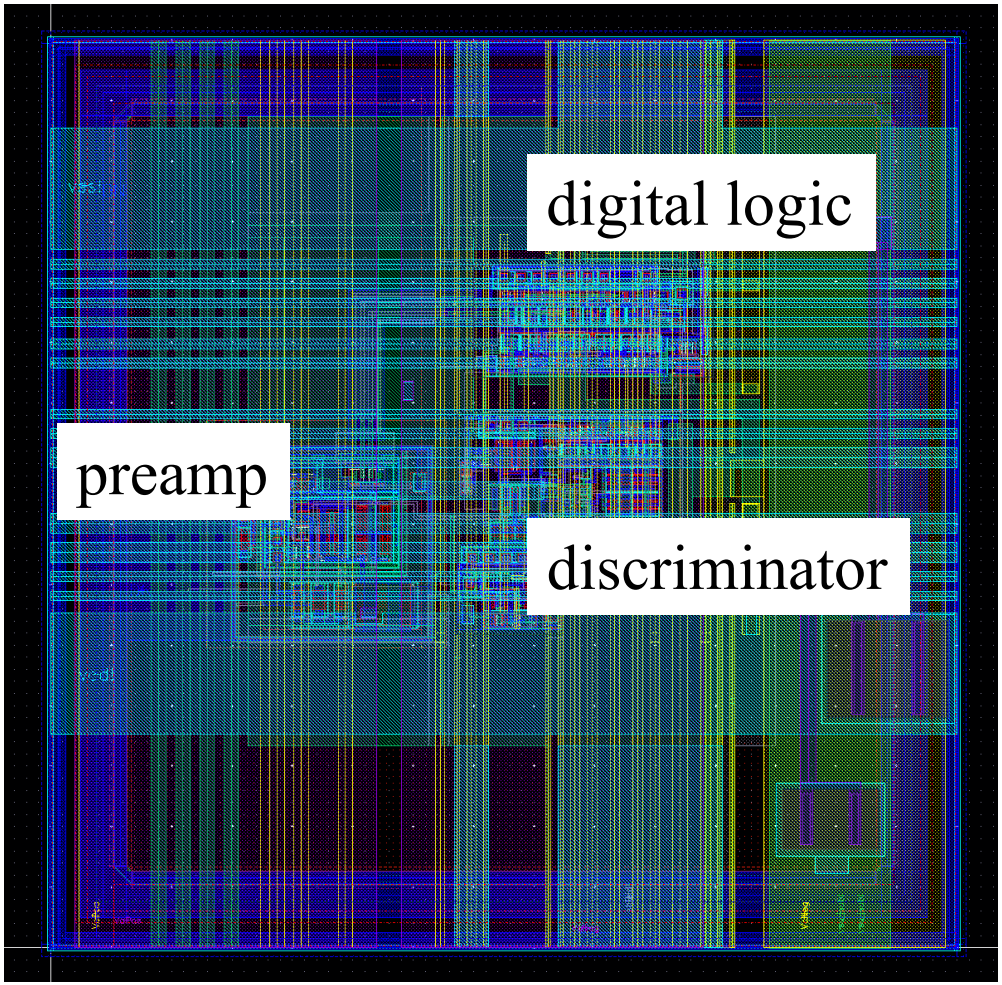
Signal/power: X-talk major issue



Parasitic diodes resulting in large input capacitance

Isolation well

LF15A: Panther



- 75um x 75um pixel
- Discriminator with global threshold and 3 local trim bits, mask bit
- Sample & hold circuit with hold delay
- Injection circuit with pixel wise selection
- Column length: 48 pixel, ~3.6mm
- TDC per column
- Digital serial data readout
- Analog pulse height and TDC „ramp“ readout

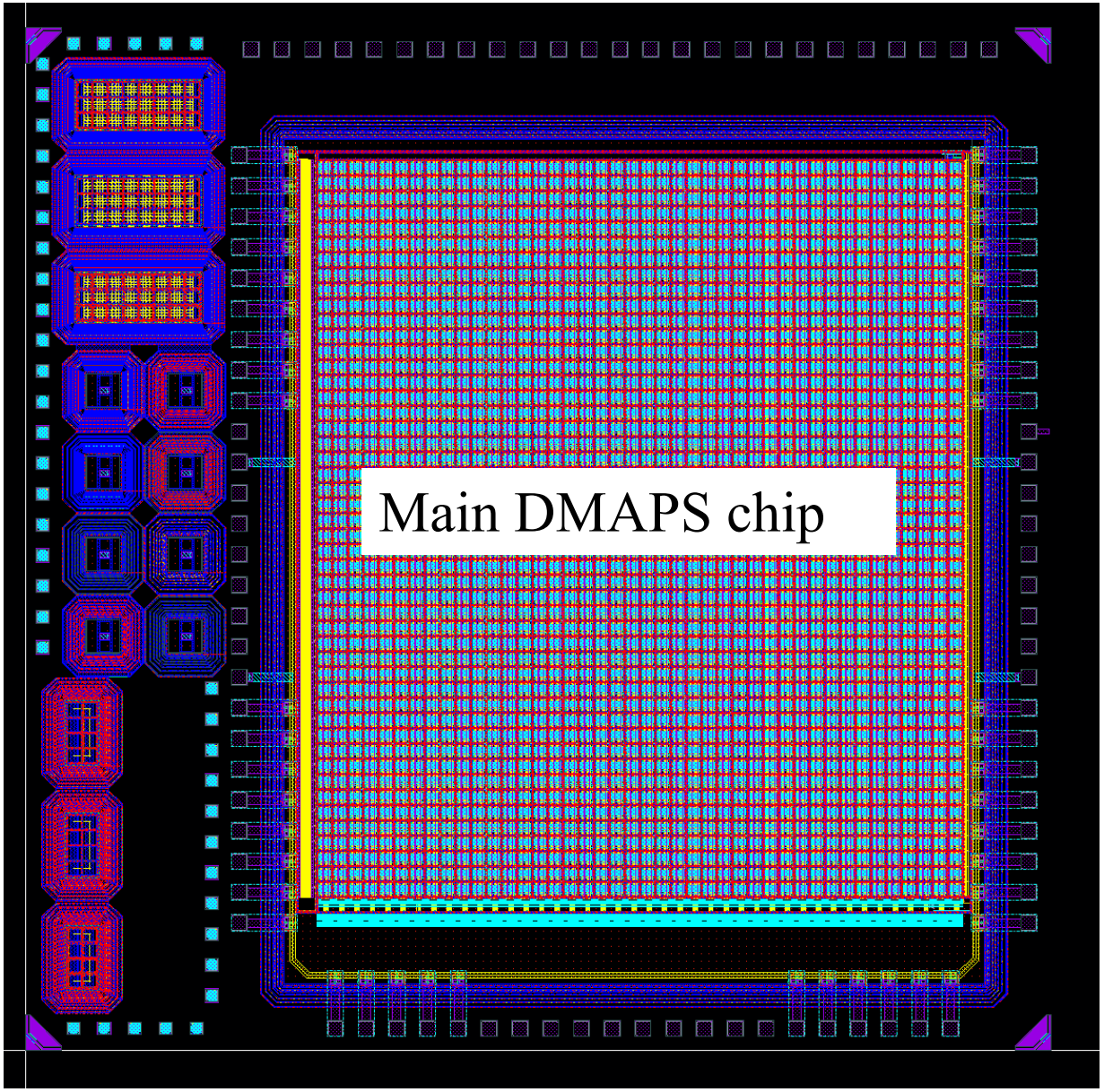
May MPW Submission

- Tape out date May 6 2024
- MPW with 5x5mm^2 area
- 4x5 mm^2 DMAPS chip with name „Panther“
- 1x5mm^2 sensor test structures
- 6 metals, deep N-well for charge collection and isolation, deep P-well for isolation
- High res wafers (~3 kOhm cm) supplied by Lfoundry
- Post processing by IBS France:
  - Thinning to 150 um:~12ke- signal (thinner sensors possible, but risk of breaking wafer increases)
  - backside p+ implant (much more uniform drift field, overdepletion possible→velocity saturation. Good for timing)
  - backside metalisation (protection from very sensitive back side)

Sensor variations

Guard ring variations

Edge TCT

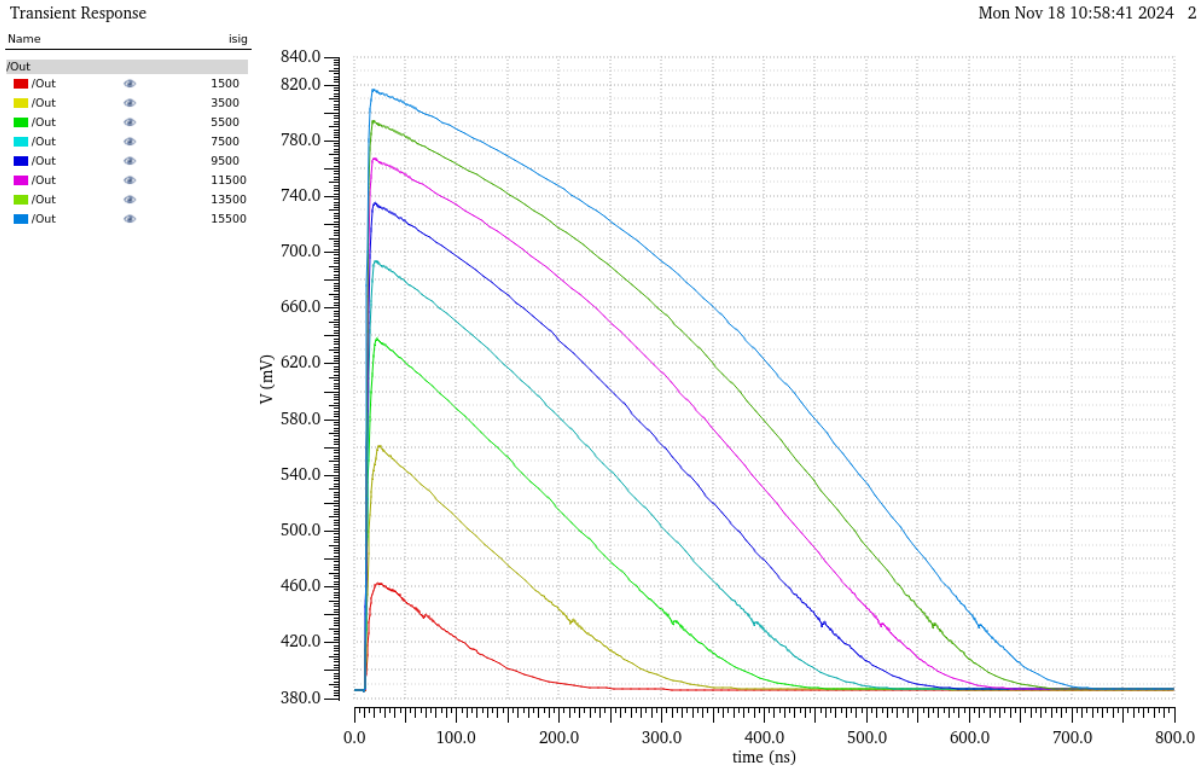


Panther chip

- 3 flavors of preamps
  - Optimized for best timing, lowest power and highest S/N
  - No universally best preamp possible. Need to choose/optimize for each specific application
- 75umx75um pixel. 48 rows, 3x14 columns
- Pixel has preamp, tunable discriminator, digital logic (kept minimal) and S&H circuit with analog PH readout
- TDC per column
- Most digital activity moved to col/row periphery. X-talk is a major issue in this technology!
- Enormous effort made to shield/decouple signals from extremely sensitive input node

Performance in post layout simulations

Output of charge sensitive amplifier I with medium power settings (~380mW/cm^2)
Gain ~ 310mV/fC for small input charges, decreasing with higher signals (which is good for timewalk correction)
Peaking time ~4.3ns
Constant current feedback (continuous reset). Baseline restored after < 1us



Time to digital converter

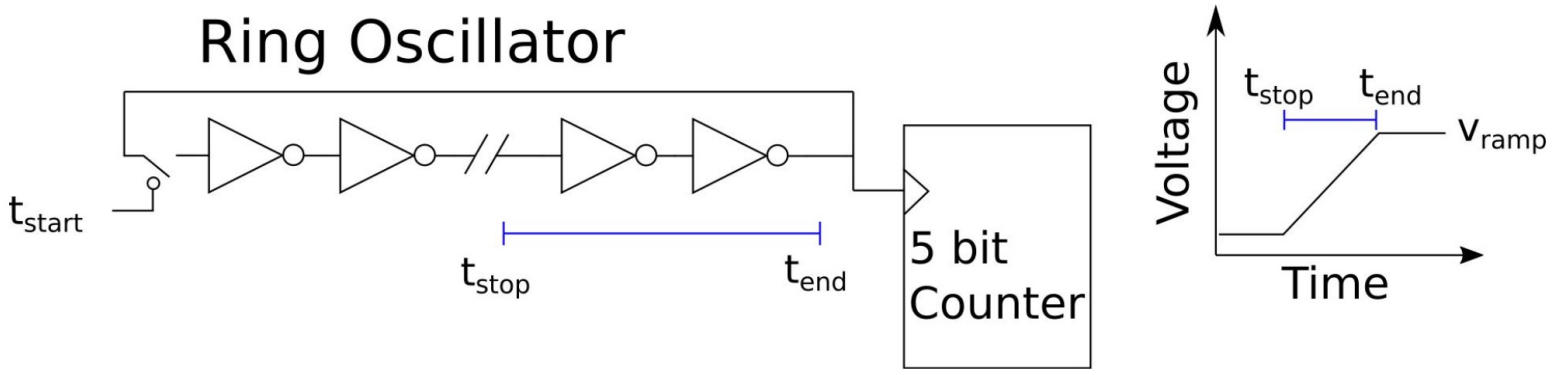
Needed for Time of Arrival (ToA) measurement

Once per column

Design developed in our group

- Coarse resolution with oscillator/counter
- Fine resolution with analog ramp (capacitor with constant current source) and analog readout

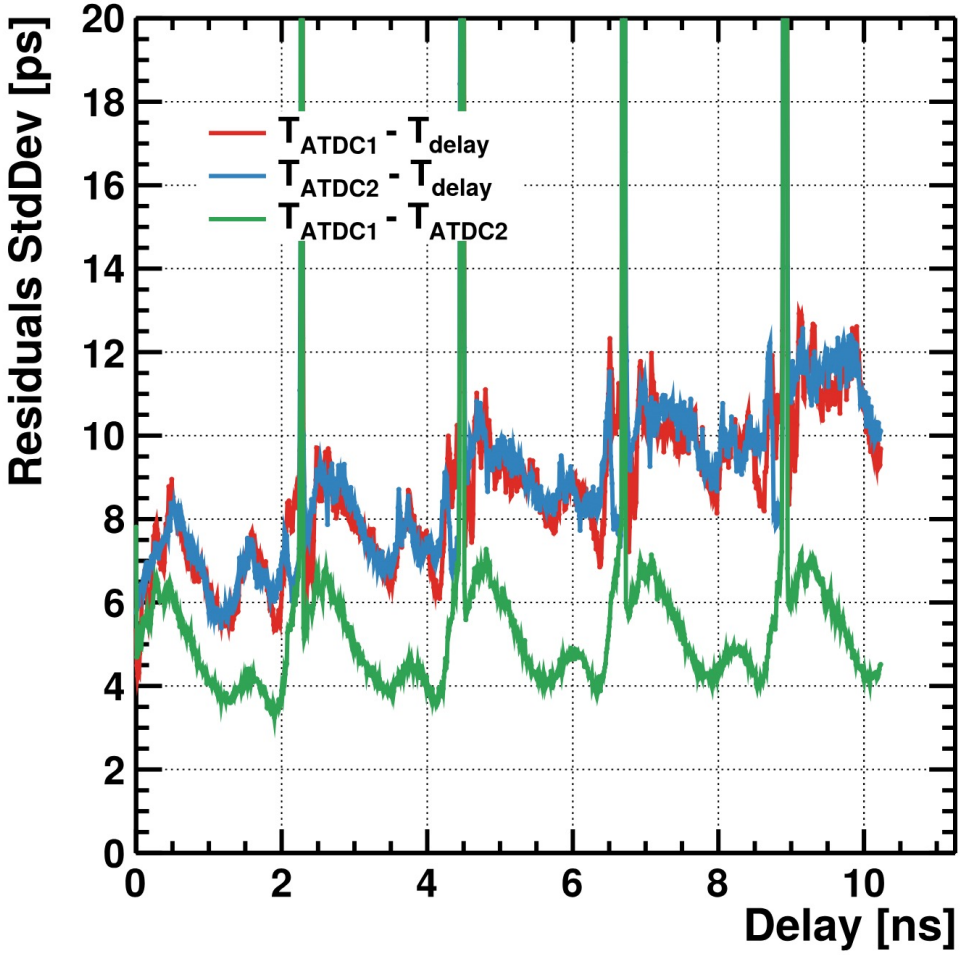
Already submitted and tested in 2 different technologies



Time to digital converter

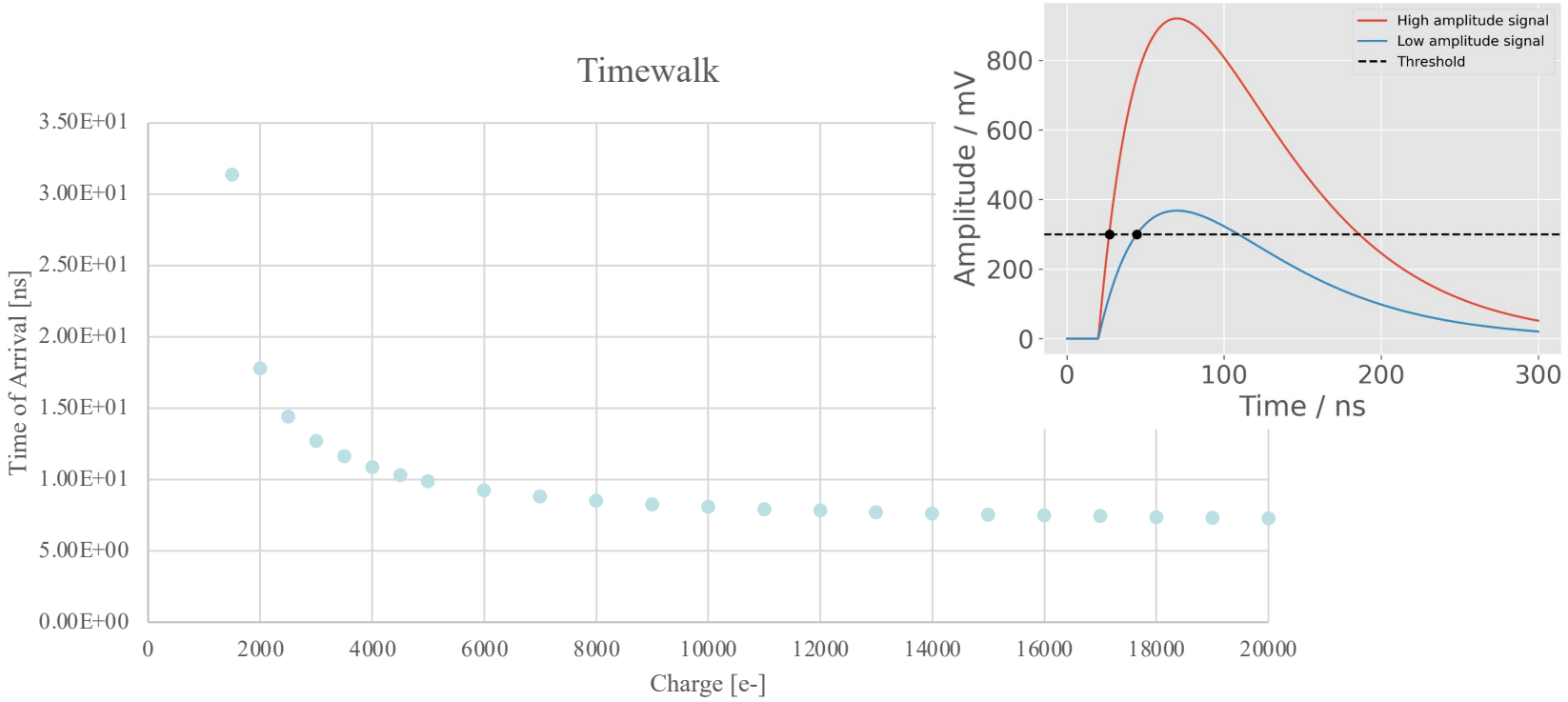
Measurement of TDC in LF 110nm (very similar to LF 150nm used for Panther)
Two identical designs ATDC1 and ATDC2
Shown are reconstructed times versus signal delay and versus each other
Resolution < 12ps

Some smaller issues recognized and understood. Has been addressed in new design. Expect at least similar precision

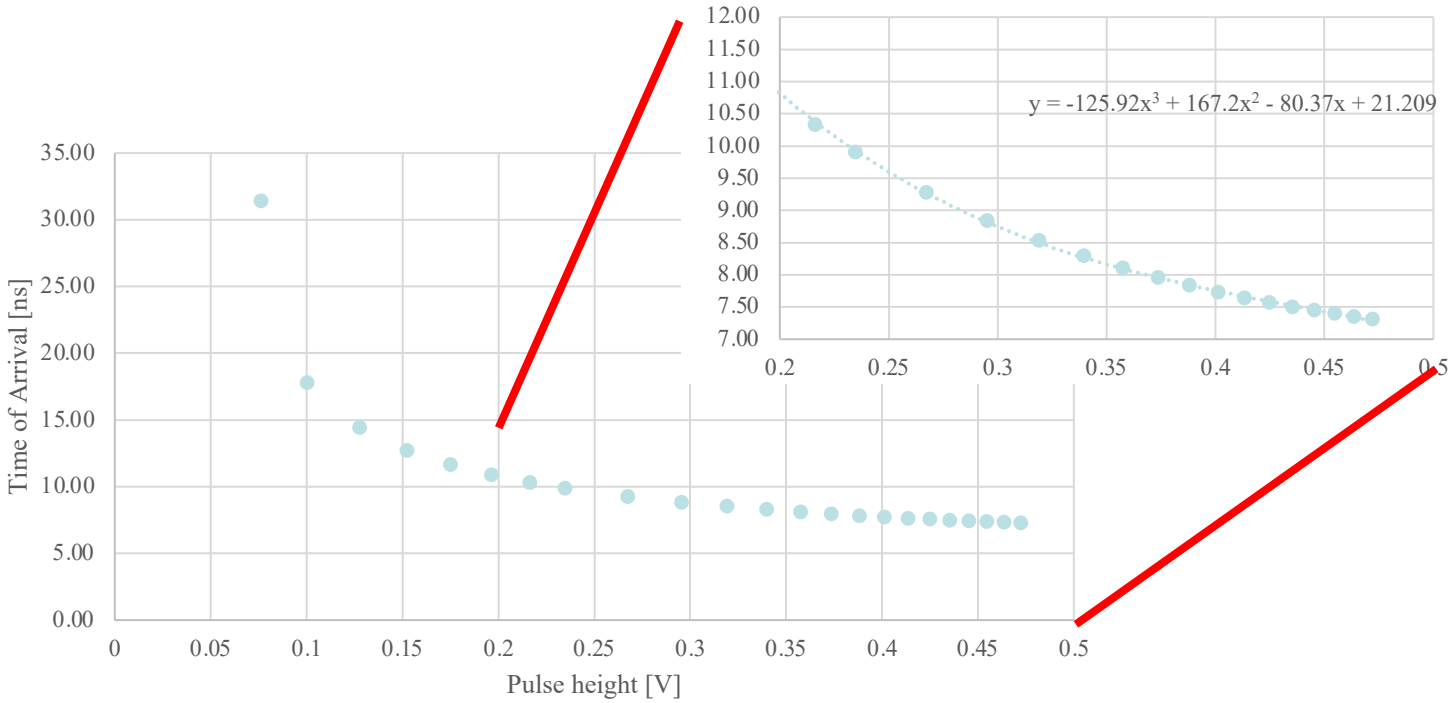


Timewalk correction (I)

Peak detection and sample and hold circuit in pixel
Analog readout of pulse height, digitization in testboard with 8 bit resolution, later on chip digitization
Needed to correct for time walk
Plot below: threshold at 1.5ke-, timewalk for signals >3ke-: ~5ns

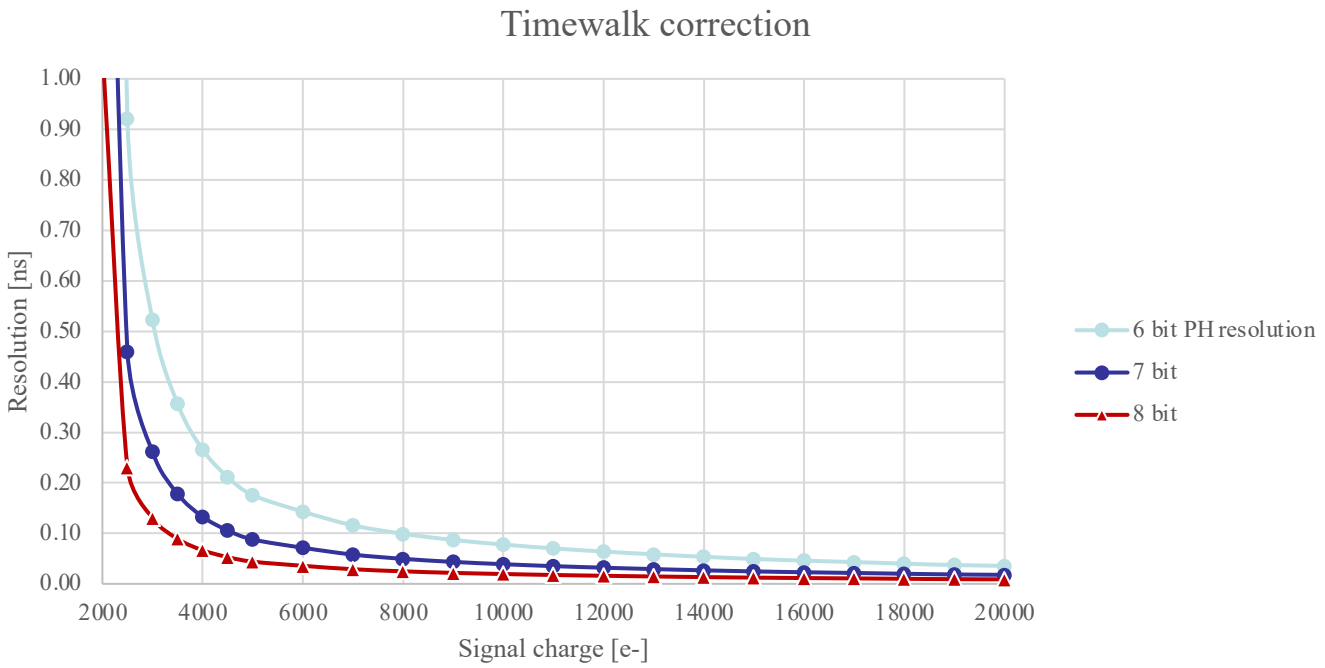


Timewalk correction (II)

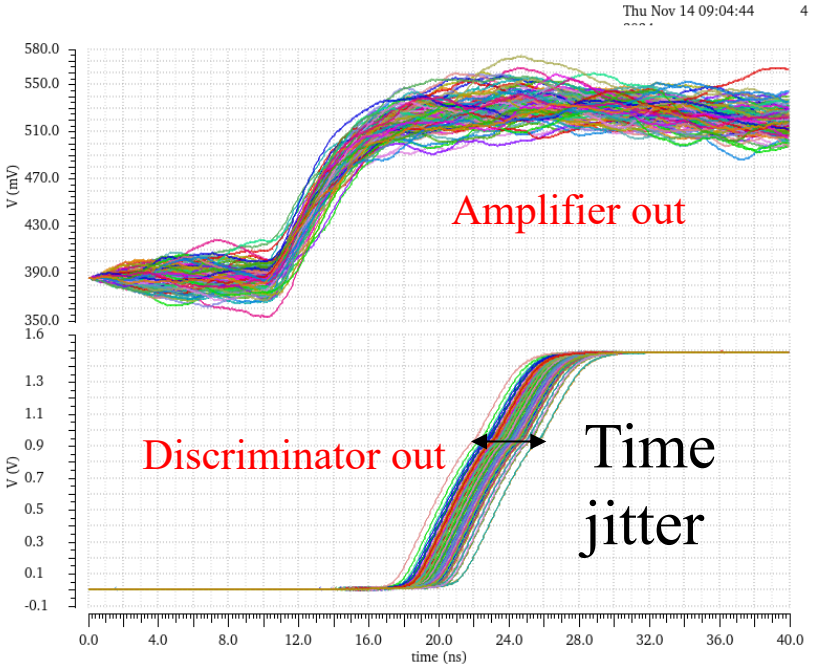


Timewalk correction (III)

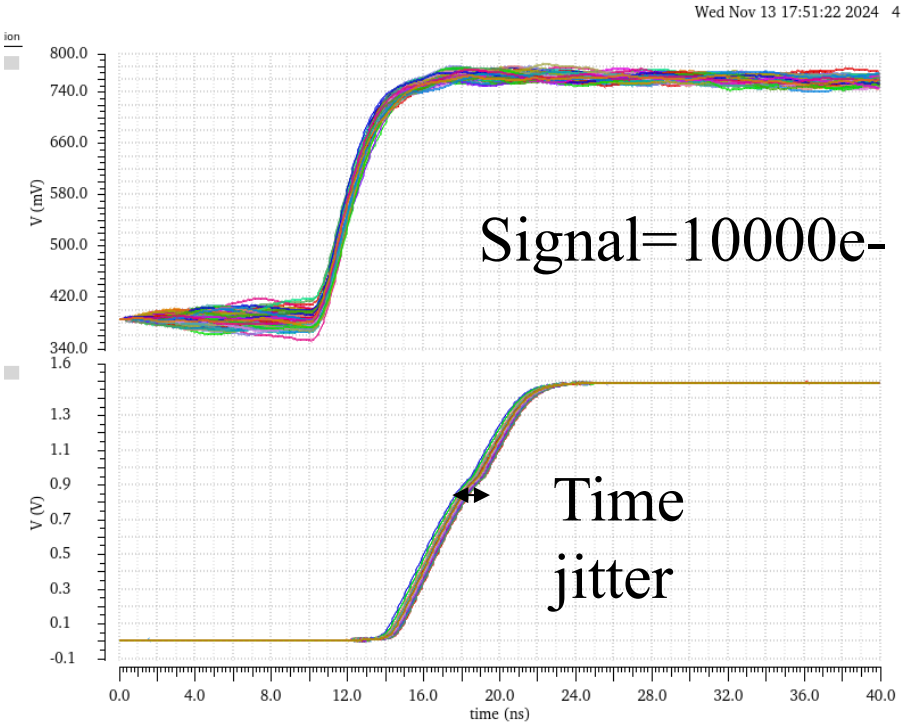
6 bit resolution for pulse height = 7.5mV resolution would be sufficient for this chip settings (correction error smaller than jitter (see next 2 slides)



Jitter (I): Transient noise simulation



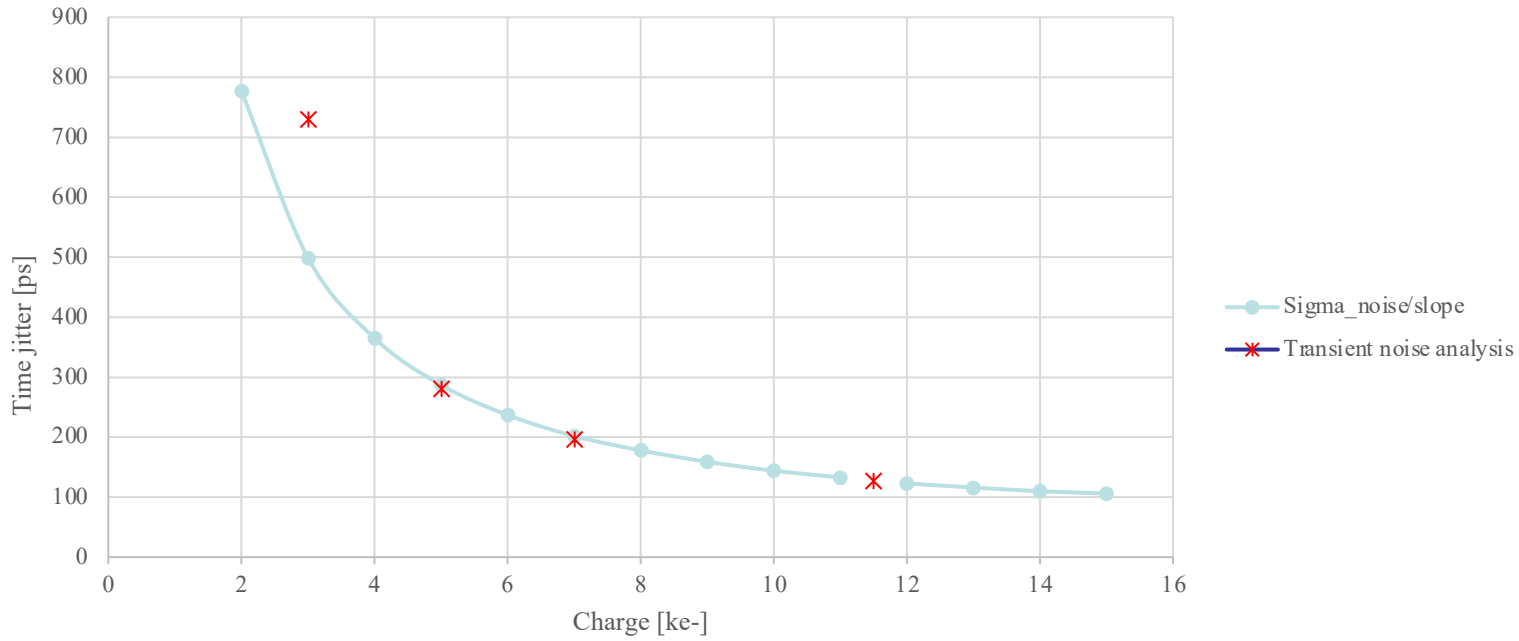
Signal=3000e-



Time jitter (II) from postlayout simulation

Two methods:

1. Noise and transient analysis: σ_{noise}/output slope
2. Transient noise analysis for selected point (slow)



Simulated timing performance

- Rely on post layout simulation. No clue how good this models reality. Will learn this soon!
- Medium power setting used for this presentation (~380mW/cm^2). Can get better performance.
- Timewalk >3ke- at threshold of 1.5ke-: 5ns
  - With 6 bit PH measurement a time resolution of <150ps is possible
- Jitter: estimated as $\sigma_{noise}/(dv/dt)$
  - 6ke- (half MIP in 150um): Jitter <240ps
  - 11.5ke- (MIP in 150um): Jitter < 130ps
- Signal distortion from fluctuation of charge deposition/ drift field distortion: not known yet. Needs to be measured.
- Signal delay difference in column <1ns, can be calibrated

Applications

- Development of dedicated DMAPS for an experiment is a huge effort and very expensive
  - Small experiments often do not have the resources
- Requirements are often quite similar in terms of spatial and temporal resolution
  - But important differences like power budget, material budget, data rate, radiation tolerance…
- Our idea is to develop a DMAPS which could fit the needs for many different applications
  - Also outside the field of particle physics
  - Likely some compromises are needed
  - Detailed studies and simulations are needed

Applications

We are looking into the following possible applications

- MuSR conventional and micro channeling
- PIONEER: DTAR or tracker
- MuEDM phase II
- Muography (imaging with athmospheric particles (mostly muons). Patent filed.
- PET (with ETHZ)
- Maybe your experiment?

μSR

μSR limited in rate to <40kHz due the need of pileup supression

- No tracking or vertexing currently possible
- Would not profit from HIMB rate increase
- Cannot measure small (mm sized) samples

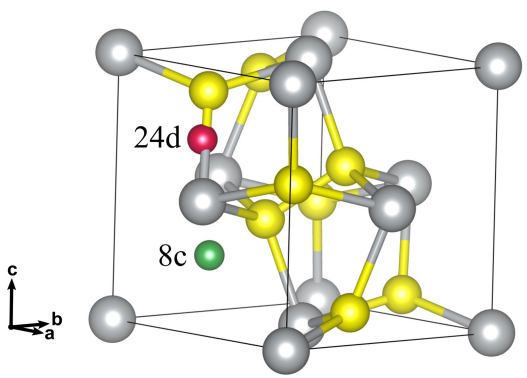
Measurements have been performed with MuPix chips for tracking/vertexing

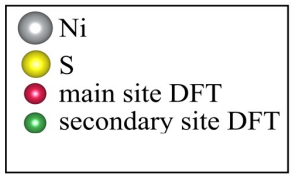
- Very promising results, but
- MuPix no longer available (TSI out of business)
- Time resolution of MuPix not sufficient, still need time reference detector
- Goal would be to reach the needed time resolution with the DMAPS

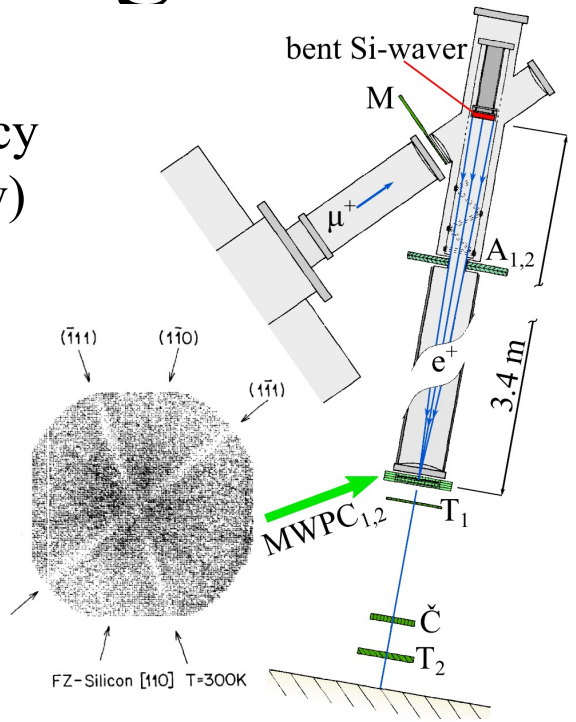
Other than standard vertex based μSR one could do micro channeling experiments to resolve muon stopping sites inside the crystal

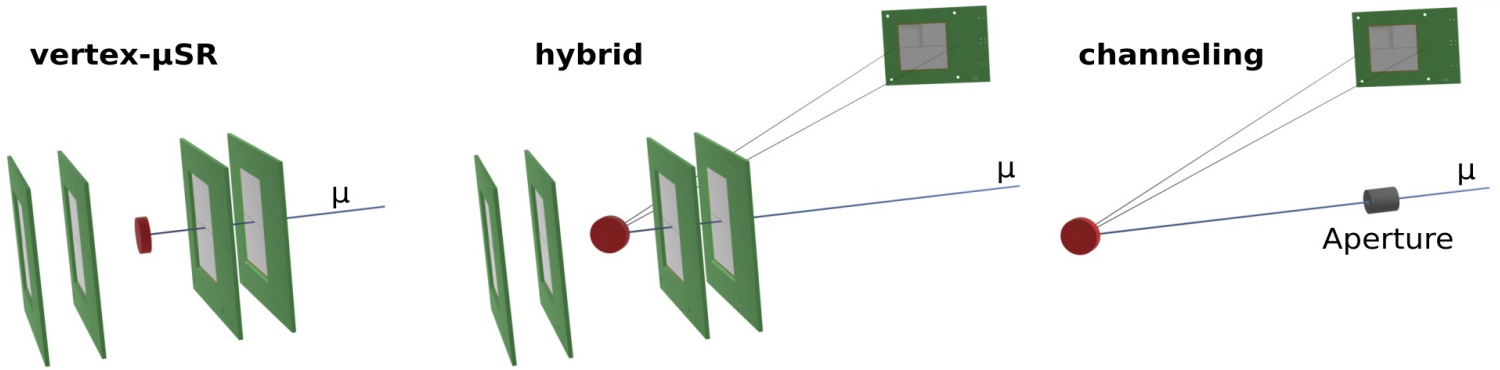
Micro Channeling

Proposal submitted with Jonas Krieger
Panther ev. reaches time resolution to do frequency resolved micro channeling measurement (to show)





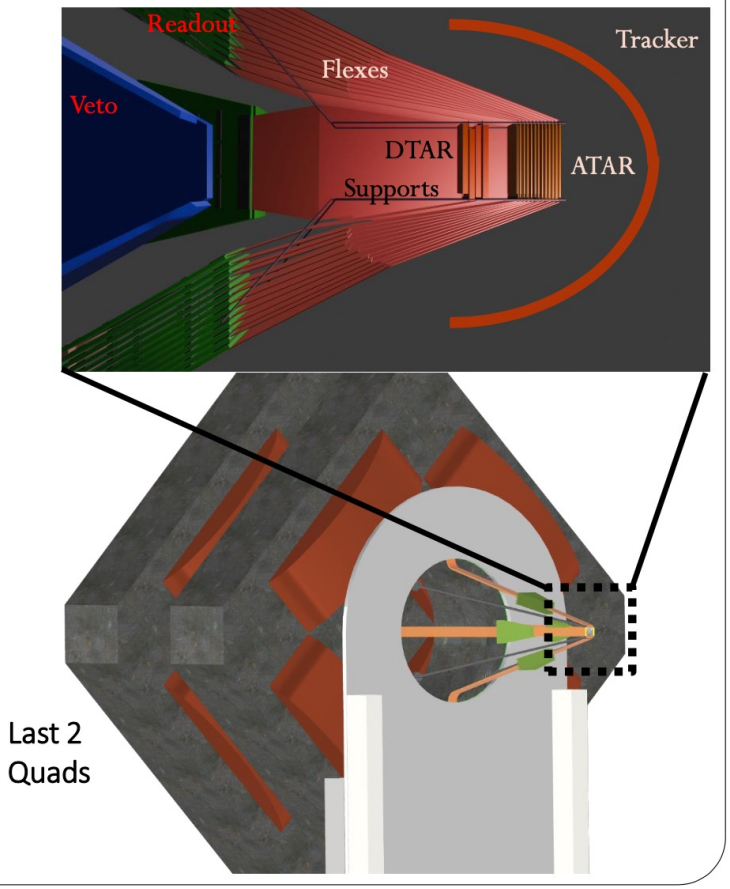




PIONEER

PIONEERS's target region

- PIONEER's target region is composed of
  - Veto counter, negating particles going to the calorimeter not passing through the active region
  - DTAR (Degrader TARget), slows down Pions, made of few thick active layers
  - ATAR (Active TARget), high granularity and timing precision, detects pion decay mode via topology and energy deposition
  - Tracker to track exiting positrons into the Calorimeter
- DTAR and ATAR are supported by rods and frames
  - Read out through flexes that bring the signal out of the active region
  - Readout chip in boards outside of the active region
  - Digitizers outside of the Calorimeter region



Veto, DTAR, Tracker: Could use Collaboration!

Slide from David Hertzog

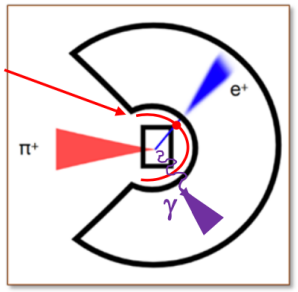
PIONEER

Slide from David Hertzog

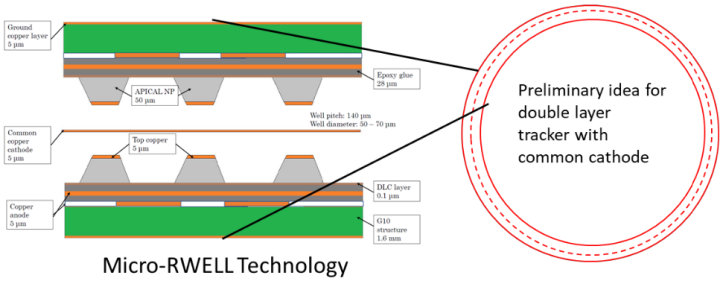
Concept of the "Tracker"

Could use Collaboration!

What should go here?



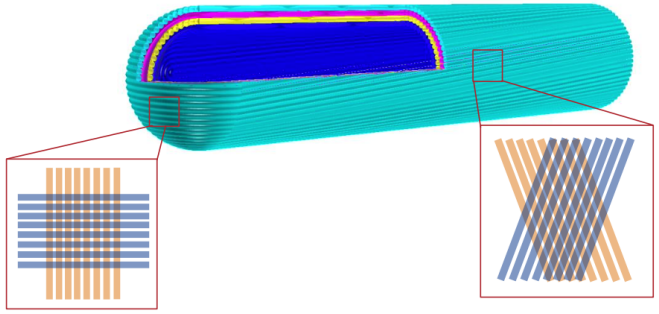
- Establish connection between ATAR and Calo for charged tracks (or veto for gammas)
- Must be thin, fast, good spatial resolution, uniform and high acceptance
- Possible used in some triggers



Micro-RWELL Technology

- High gain (~ 10^4)
- Good spatial resolution (<100 μm)
- Good time resolution (~ 5.7 ns)
- High rate capability (~ 1 MHz/cm^2)

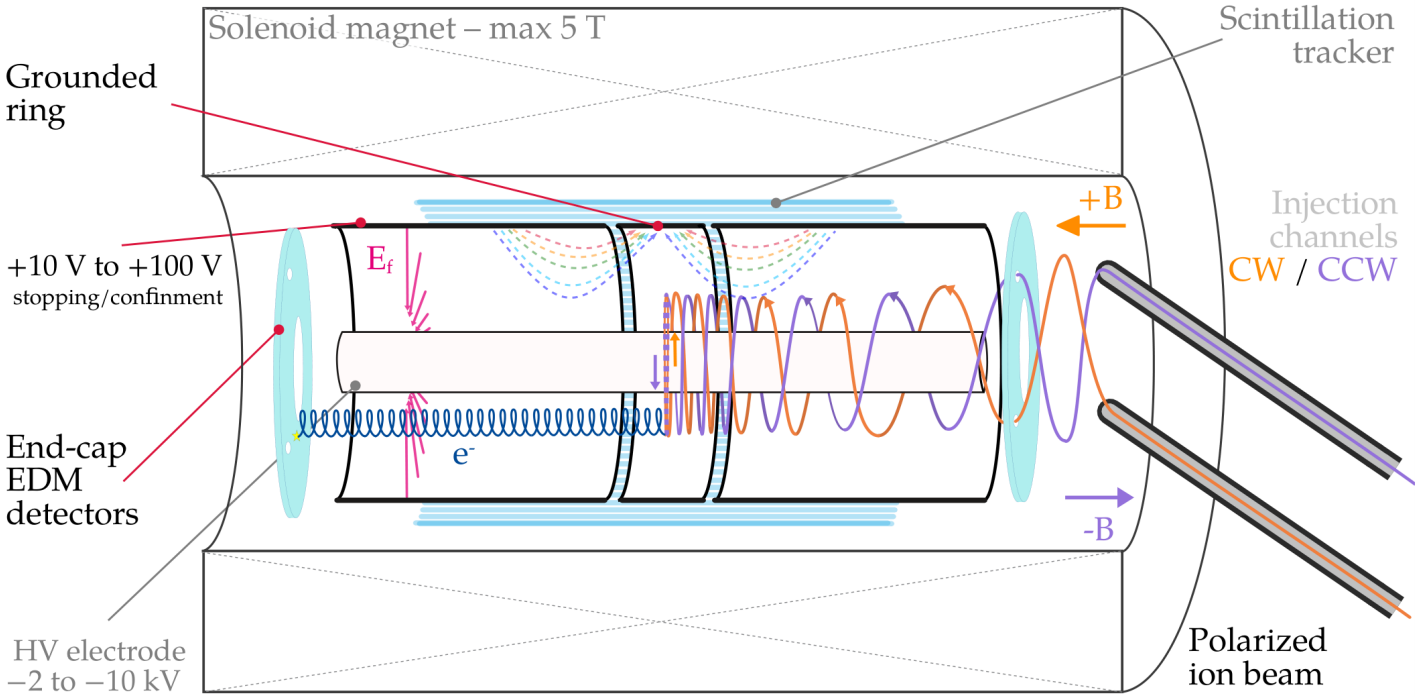
Layered SciFi Tracker



- SiPM readout of fibers
- Modest spatial resolution (<100 μm)
- Excellent time resolution (< 1 ns)
- High rate capability

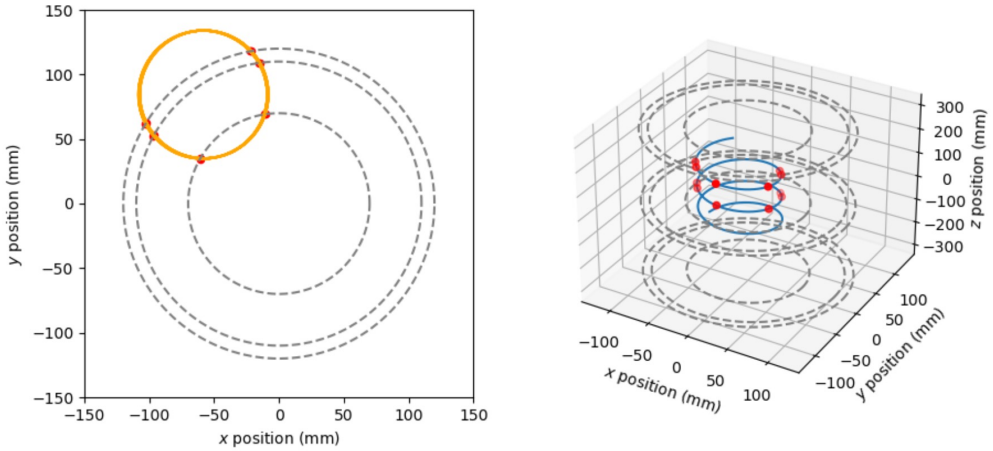
Specs seem relaxed for DMAPS. Could be a good alternative.
Shape is challenging → overlapping chips. Material budget?
Simulations needed → started at PSI (Tilman)

MuEDM Phase II



Picture shows Phase I configuration. We would aim for phase II

MuEDM



Study on spatial and temporal resolution from Johannes Jaeger
Still Phase I configuration. Phase II conception not yet stable (in contact with Chavdar)
3 tracking layers with 100um Si
Conclusion in short: pixel size <100um, time resolution <100ns
Cooling and material budget will be the main challenge
Detailed simulations needed

Outlook

- We will have the chips back by the end of the year (wafers are at company doing back end processing)
- Hopefully it works as expected. X-talk and „collective phenomena“ could be a major issue.
- If we really reach a threshold <2ke-, X-talk is under control, simulation models and parasitics describe reality well we could continue develop a large area chip for real applications
- Now we have started to find applications and understand the specifications exactly. Detailed physics simulations are needed and is work in progress.
- Then we can optimize the chip for performance/costs.
- Any suggestions or interests from you are very welcome.