Contribution ID: **106** Type: **Invited Talk**

Analytical model for the switching voltage and gain coefficient of a CMOS inverter with nanochannel 2D transistors

Thursday, November 7, 2024 9:15 AM (45 minutes)

The study presents an analytical model for the switching voltage and gain factor of a CMOS inverter with 2D nanochannel transistors. The derived expressions enable the modeling of these two fundamental parameters of the device, which serves as the foundation for logic elements in contemporary nanoelectronics. The feasibility of creating efficient inverters with a high gain factor based on transistors with channels made of 2D monolayers of transition metal dichalcogenides and arrays of carbon nanotubes has been confirmed. It was demonstrated that the gain factor is restricted by the drain induced barrier lowering (DIBL) effect, which is undesirable for FETs (when DIBL trends to zero the gain factor becomes infinitely large).

Type of presence

Presence online

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Session Classification: Optics and High Technology Material Science: Plenary