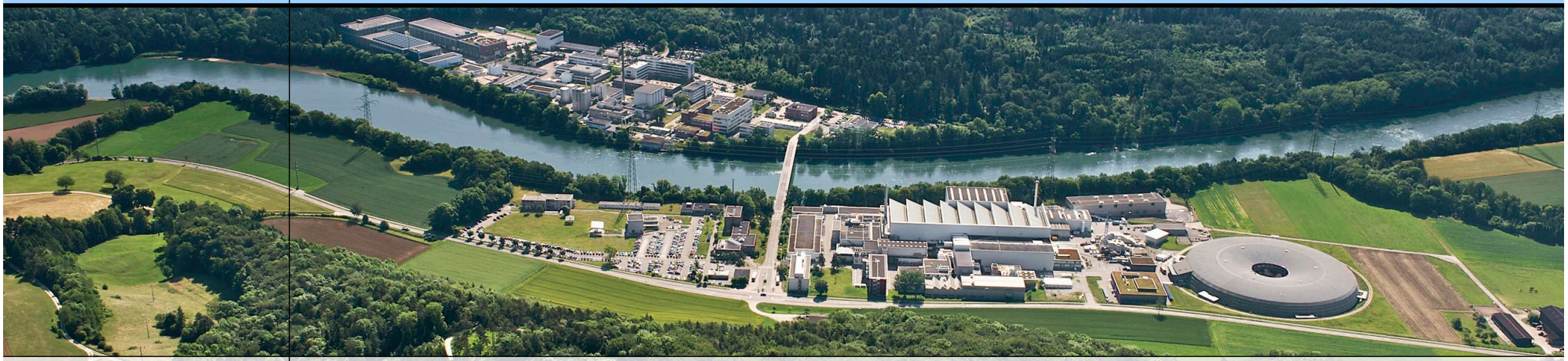
PAUL SCHERRER INSTITUT

PSI



Wir schaffen Wissen – heute für morgen

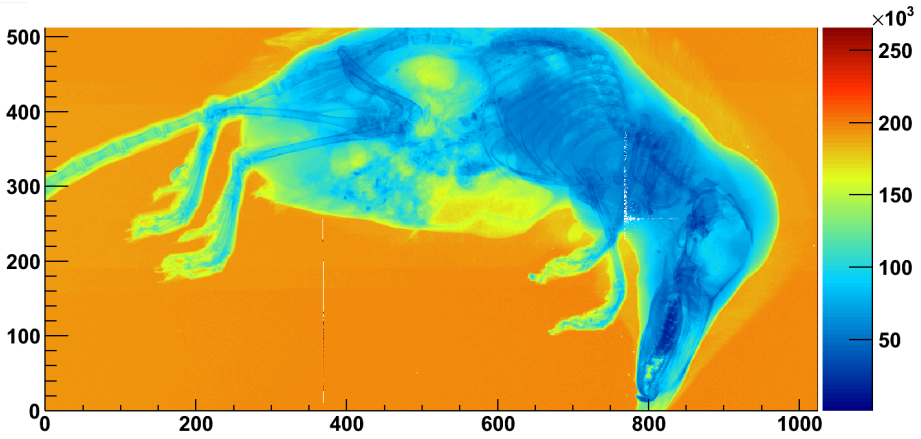
Paul Scherrer Institut

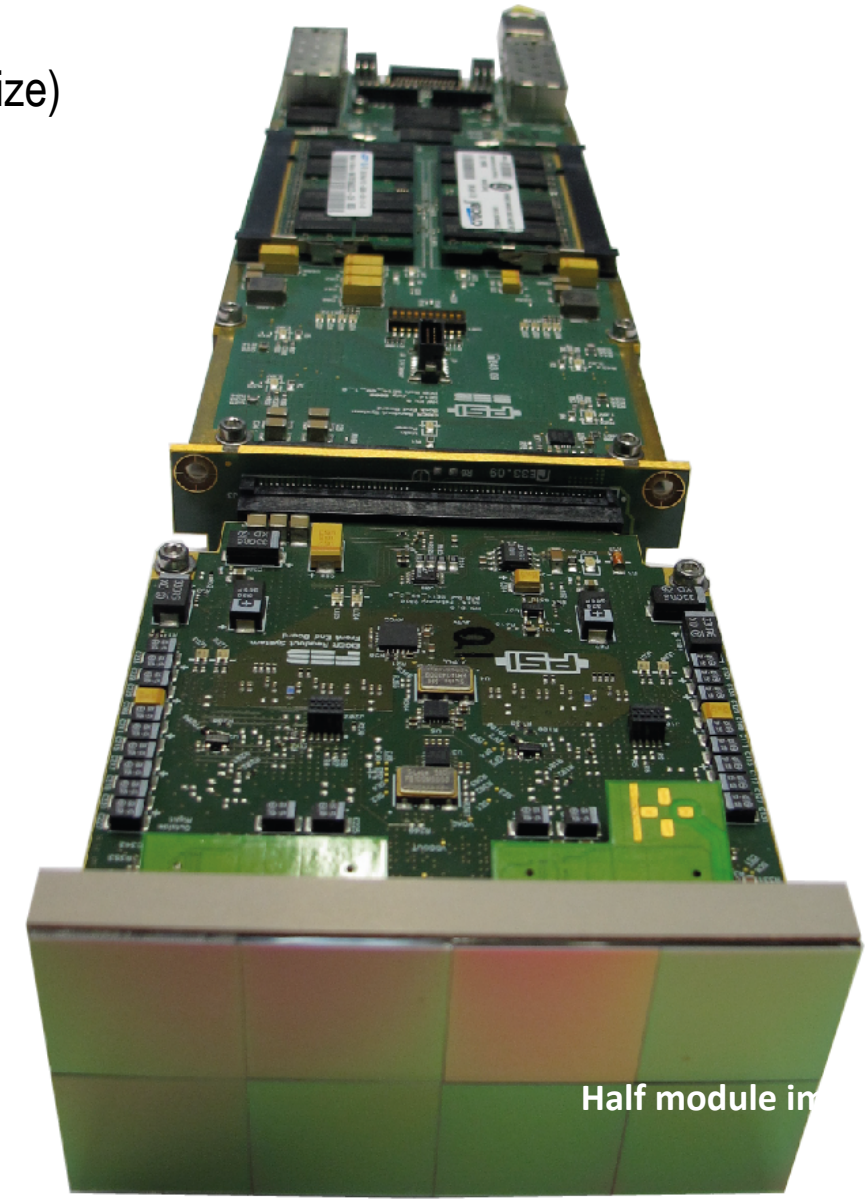
Beat Henrich

EIGER: The PSI detector developments

EIGER, next generation pixel detector

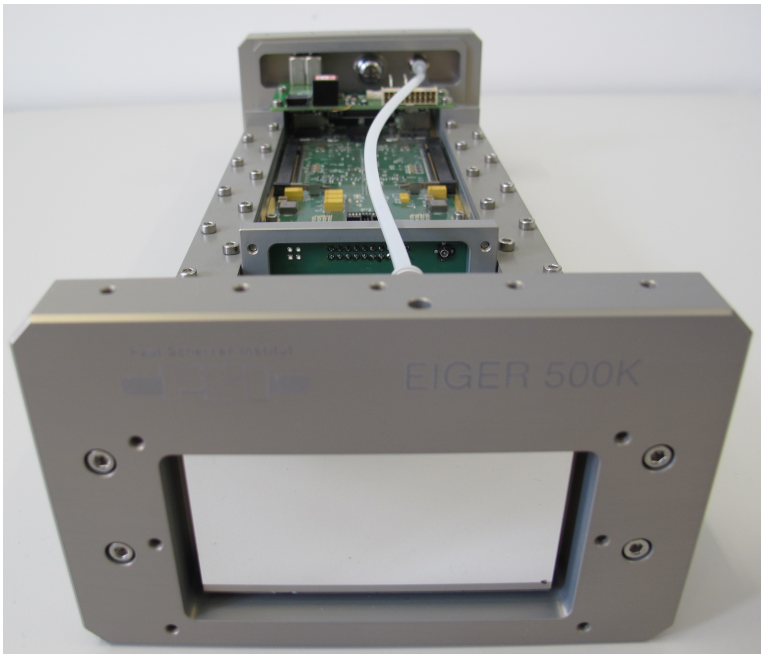
- Single photon counting pixel detector
- Sensitive area of 38 X 77 mm^2 (about Pilatus size)
- 524k pixel module
  - 2 x 4 chip array
- Maximum frame rates
  - 23 kHz in 4 bit mode
  - 12 kHz in 8 bit mode
  - 8 kHz in 12 bit mode
- Maximum data rates on the readout boards
  - 25 Gb/s for a half module
  - 50 Gb/s for a module
- On board in hardware data processing
- 8 GB of memory on a module
  - four - 2 GB RAMs per module
- Two 10 GbE data links per module



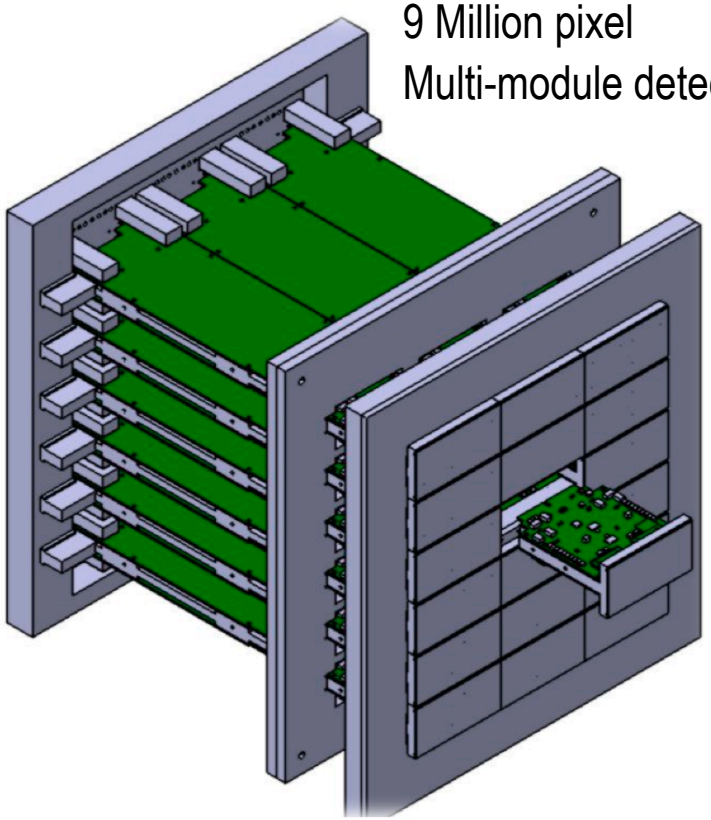


EIGER systems

500k single module



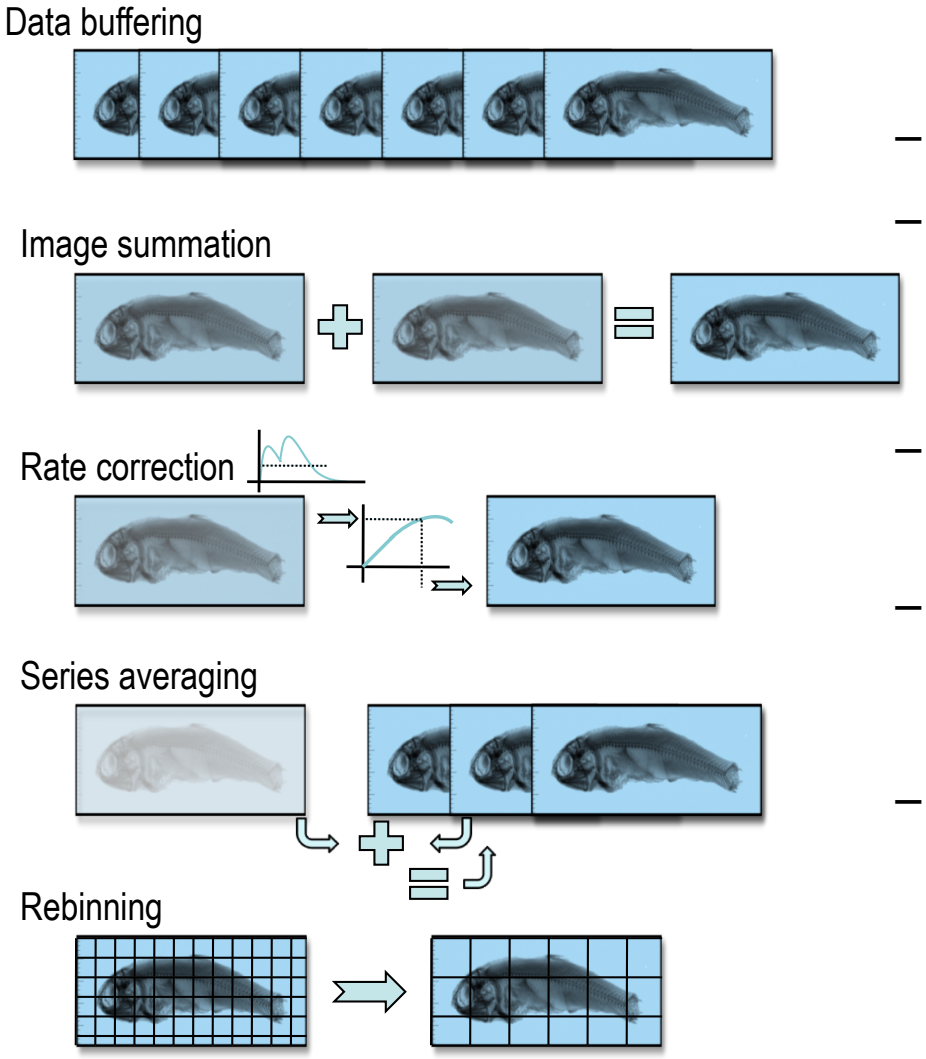
9 Million pixel
Multi-module detector



	Number of pixels	On board storage (frames/4 bits)	Data rate[1] @ 12 kHz	Data rate[2] @ 1kH	Data rate[3] @ 100 Hz	Data rate[4] @ 10 Hz
Module	524 k (512 x 1024)	~32,740	50.3 Gb/s	6.29 Gb/s*	839 Mb/s*	168 Mb/s*
9M Detector	9.44 M (3072x3072)	~32,740	906 Gb/s	113 Gb/s	15.1 Gb/s*	3.02 Gb/s*

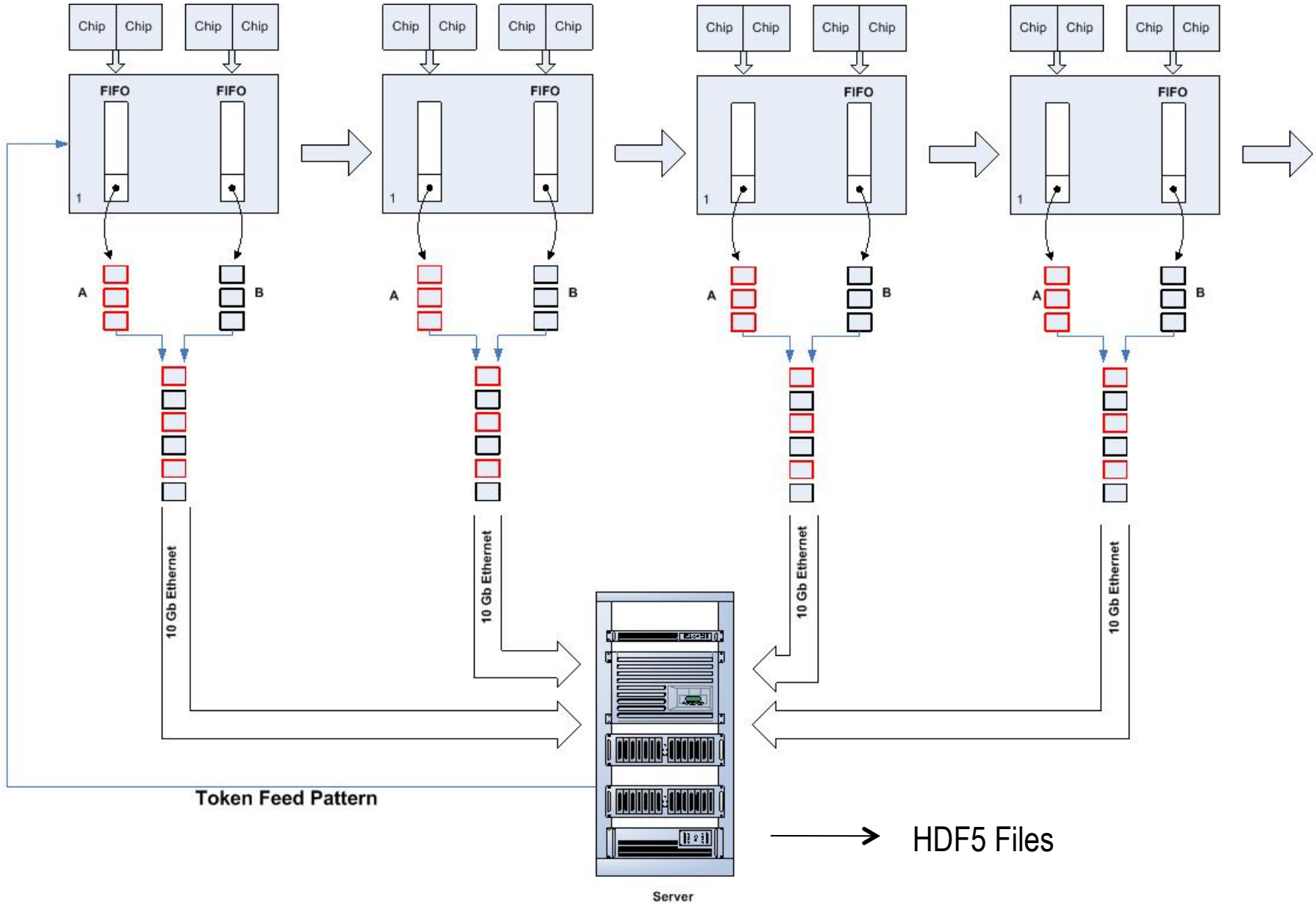
1) 8 bit, equivalent to ~4@23 kHz and 12@8 kHz. 2) 12 bit. 3) 16 bit. 4) 32 bit. *) Foreseeable continuous storage rates (~20 Gb/s).

On board data processing (in firmware)



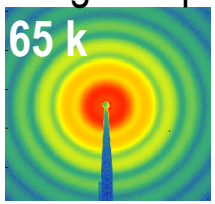
- On board data processing is in parallel on multi-module systems
  - independent of the detector size
  - reduces a modules tens of Gb/s at the source
  - or a 9Ms, hundreds of Gb/s at the source
- Data buffering
  - on board memory for 32 k frames per 4 counter bits
- Image summation
  - extends the dynamic range from 4096 to $4x10^9$
  - ~1 k sub image frame rate (4 M counts/pixel/s)
  - transparent to the user
  - makes high flux continuous data taking possible
  - reduces the quantity of data at the source
- Rate correction
  - performed on sub-frames @ kHz frame rate
  - more precise, less sensitive to rate fluctuation
  - real-time processing
- Pump and probe series averaging
  - high frame rate exposure series summing
  - alternating pumped and un-pumped
  - no data transfer dead time between series
  - huge reduction of the quantity of data at the source
- Data reduction
  - 2x2 pixel rebinning
  - SAXS ring intensity averaging (planned)
  - data compression (in thought, question of HDF5 compatibility)

Readout Architecture

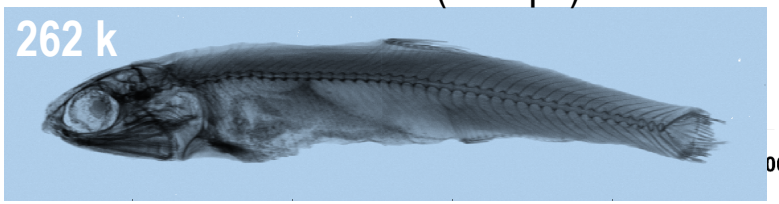


Summary for EIGER

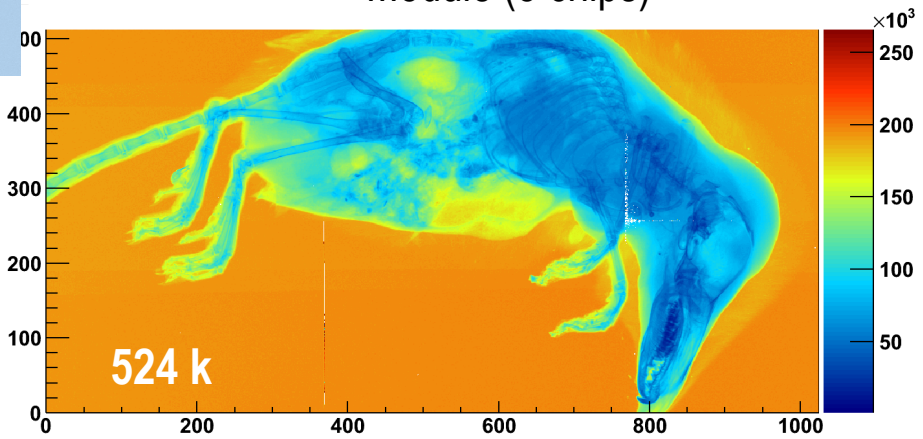
Single chip



Half module (4 chips)



Module (8 chips)



- First results
  - characterization of the chip
  - the first demonstration experiments
- Single module system @ cSAXS
  - in the first half of this year
- High performance 9M Eiger @ cSAXS
  - on board memory (288 GB RAM) or 2.5 sec @ highest data rates
  - 100 Hz continuous operation and data to disk
  - IT infrastructure and data storage (Heiner Billich)
- Licensed to Dectris
  - many systems around the world
- Dectris 16M Eiger @ PX
  - collaboration between Dectris and PX beamline
  - we are working closely with Dectris to develop a common data file structure (HDF5)
- Collaboration with the ESRF
  - Single module systems
- Single module system at the surface diffraction station (Material Science)