

The FSP camera system

The FSP camera System is the first 36 μm , 1 MPixel pnCCD camera system developed for use in X-ray microscopes.

The camera system is based on a fully depleted, backside illuminated 1 k x 2 k pnCCD. Standard use case is the split frame, framestore operation providing a field of view of 1k x 1k pixels of 36 μm size. Depending on the target noise requirement, framerates of 400 Hz can be achieved in this mode.

All required voltages are derived from a single 12 V supply. The system utilizes an integrated controller based on a state-of-the-art Xilinx SoC, which allows for comprehensive housekeeping, intelligent sequencing and user-defined data preprocessing functionality. Output data to mass storage is provided as UDP data stream using a dual 10 GBit Ethernet optical link. A single PC via a standard GBit Ethernet connection control the system. For its system design, a modular approach was chosen. We designed most components to be interchangeable in order to ease maintenance and speed up repair time, thus reducing instrument downtime.

In the first iteration, the pnCCD and its 4 Hybrid PCBs and the required mechanics are placed inside the Vacuum as a detector plane Array (DPA). The Hybrids mount Veritas I readout ASICs, phi-drivers passive components for voltage conditioning as well as components for monitoring the system status. The (DPA) is connected to the peripheral electronic assembly (PEA) via flexible cables. The PEA includes, among other components, the Brain of the system, which is formed by the central Mercury XU1 providing a Zynq System on a Chip (SoC). For digitization, we use a multi channel ADC card equipped with four 8 channel ADCs.

The system is currently put together and a first test at our lab is planned in the course of the next months.

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