

**FACULTY OF
NUCLEAR SCIENCES
AND PHYSICAL
ENGINEERING
CTU IN PRAGUE**

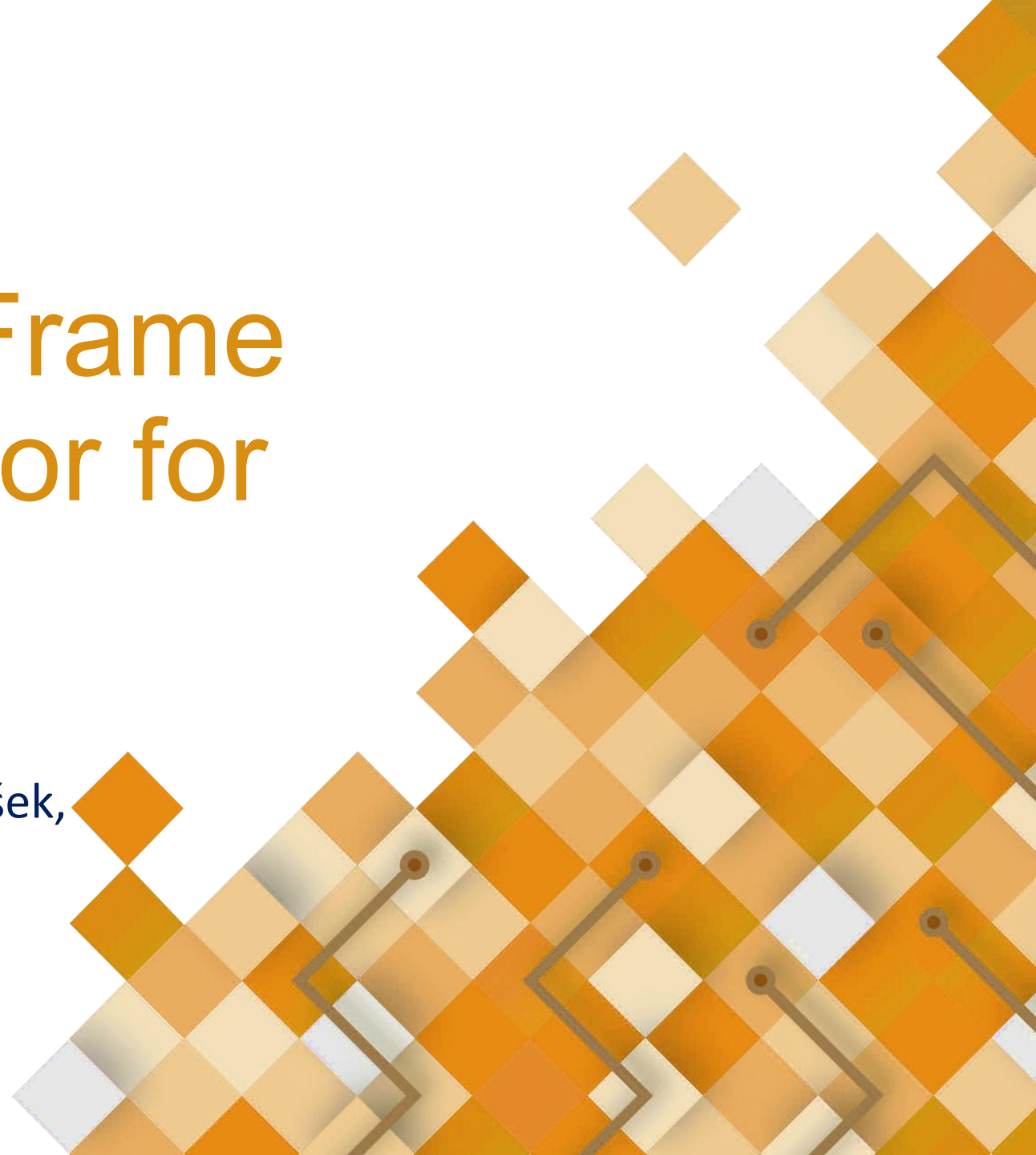
FASXCAM - High Frame Rate MAPS Detector for Soft X-rays

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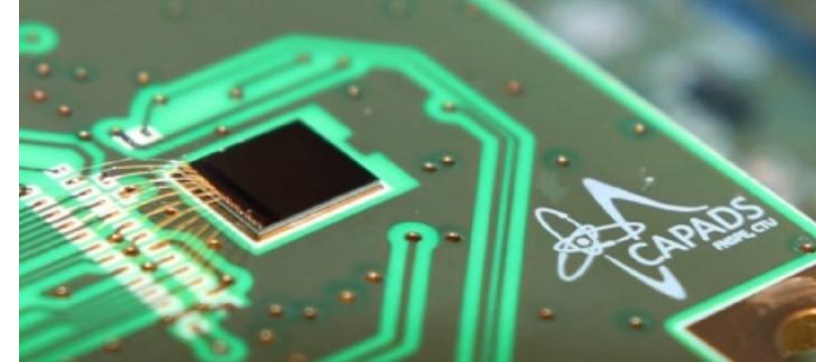
**Faculty of Nuclear Sciences and Physical Engineering
of the Czech Technical University**

X-ray Sensor Joint Workshop 2026, Zurich

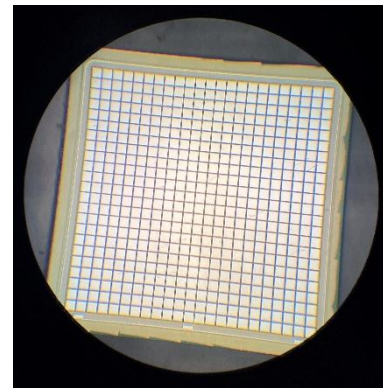


CAPADS TEAM @ FNSPE CTU IN PRAGUE

- Measurement of ionising radiation
 - Radiology, dose rate measurement, spectroscopy and space weather
 - **Since 2012** (beforehand CERN R&D)
 - **MAPS, SiC segmented LGADs**
- **Technologies:**
 - Onsemi - Proprietary sensors (Si, SiC - own process flow)
 - LFoundry 150 nm CMOS (LF150)
 - AMS 180 nm CMOS (C18, aC18)
 - TSI 180 nm CMOS (H18)
 - **X-FAB Sol 180 nm (XT018)**
 - **TSMC 65 nm CMOS LP**
- Quantum optics projects, astrometry



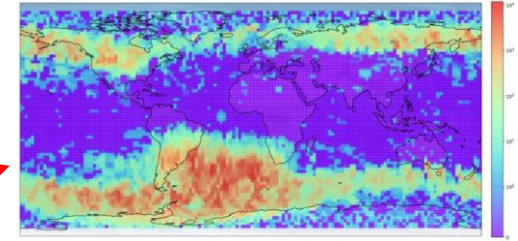
Segmented SiC LGADs



FOCUS ON APPLICATION
ASICs: over 30 tapeouts (4 ERs)
Sensors: silicon (20 ERs)
CZT (prototyping)
SiC (prototyping)

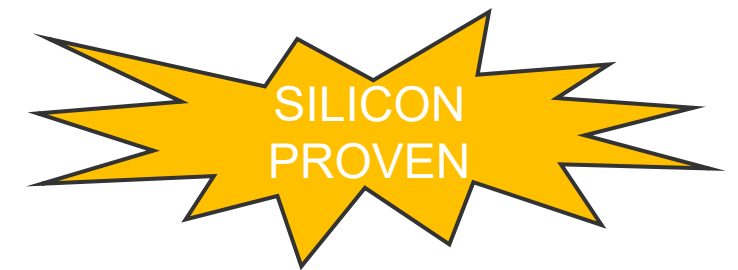
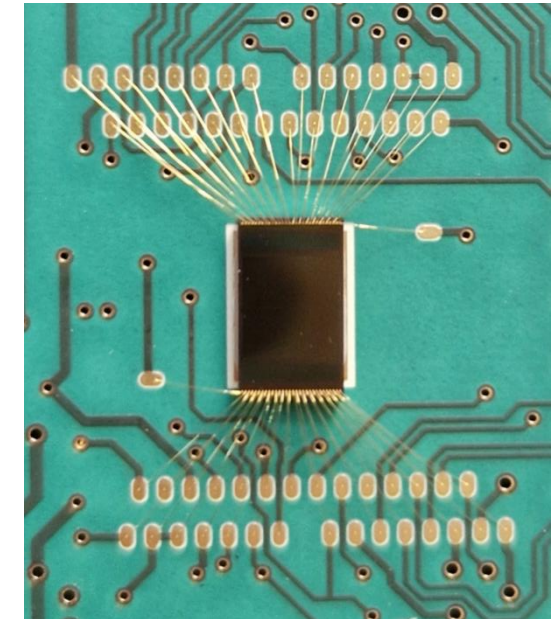
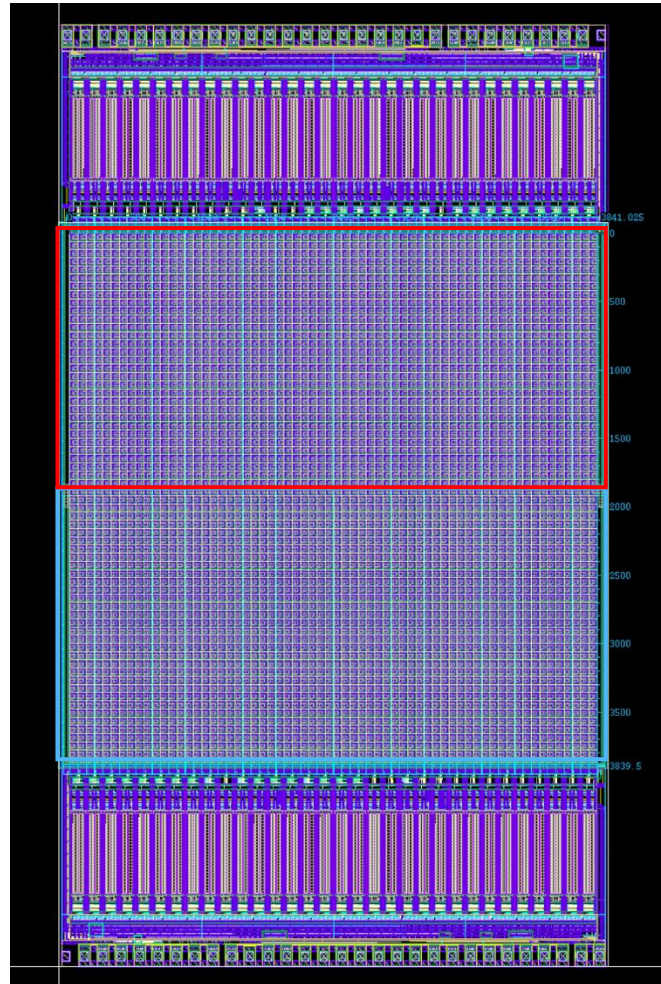
Motivation for FASXCAM detector

- MAPS sensor for high-speed monitoring of X-ray events in plasma (abbreviation **FAStXrayCAMera**), monolithic detector on the same substrate as signal processing electronics.
- Design focus: reliable high-rate operation in real experimental environments.
- Evolution of our previous generations of MAPS detectors SPACEPIX (satellite mission VZLUSAT2) and SMARTPIX
 - Faster readout - removed SPI mode, faster LVDS @ up to 400MHz with CLK_OUT for phase alignment
 - Reduced per pixel dead time by adding rolling shutter mode
 - Improved internal reference stability for ADCs
 - Optional external voltage reference (already used in practical application)
 - Bug fixes



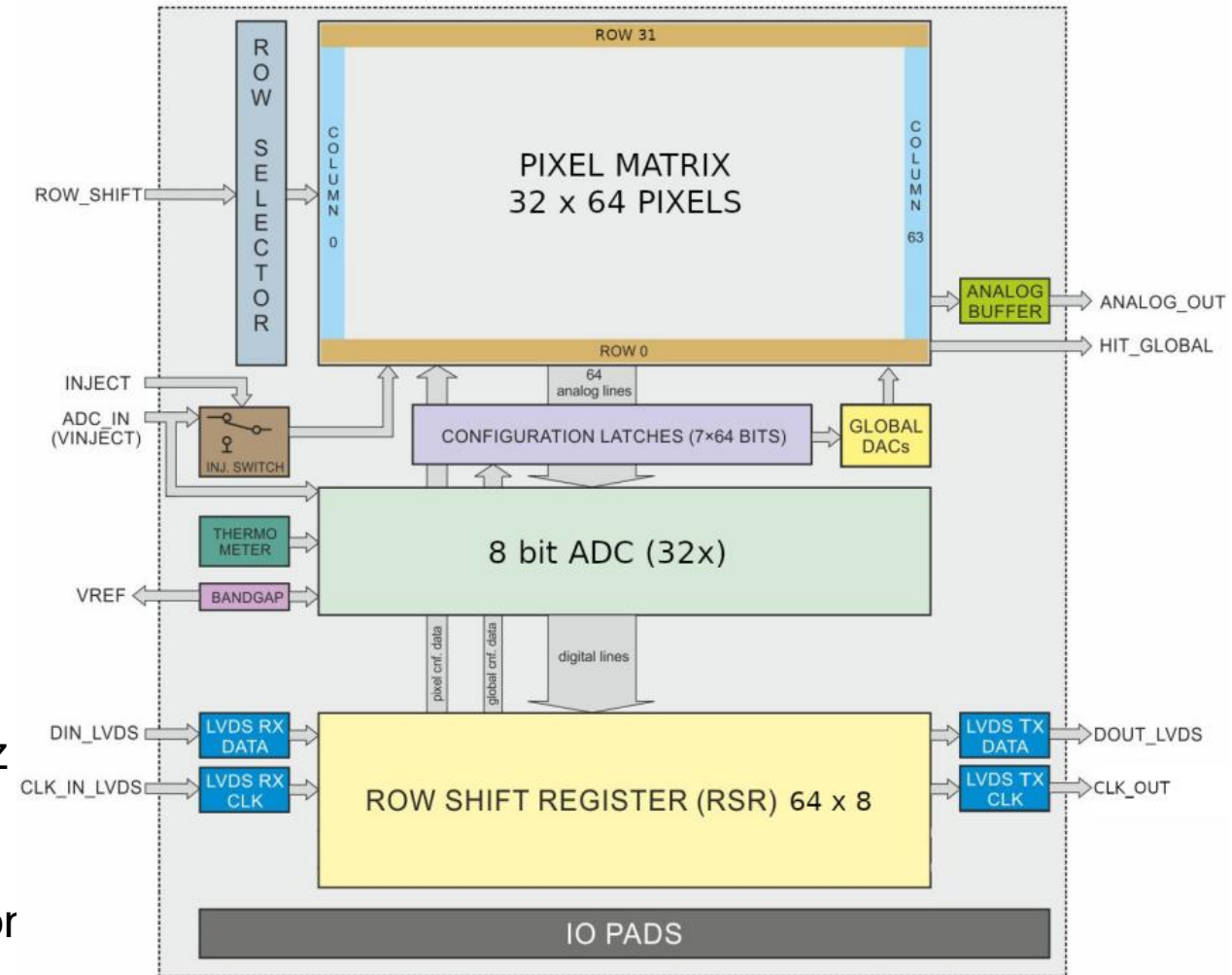
Specifications

- Two 32x64 pixel chiplets for increasing data transfer
- Pixel area $\sim 60\mu\text{m} \times 60\mu\text{m}$
- Sensitive matrix area $3840 \mu\text{m} \times 3840 \mu\text{m}$
- Energy range 2.9 keV to 21.6 keV (0.8ke to 6ke in Si)
- SAR ADC with 8-bit resolution
- Shutter mode: frame and rolling
- BIAS -150V
- External charge injection (0.6fF cap) for a calibration/test
- Global HIT signal
- Analog output
- ADC/DAC input/output for calibration
- 400 MHz LVDS bus
- Max. $\sim 15000 \text{ FPS @ } 400 \text{ MHz}$
- On-die thermometer
- Power supply 1.8V, max. 45mA / chiplet



Operation principles

- MAPS imaging chip – pixel detection matrix and processing at the same substrate
- Analog pixel frontend with CSA, discriminator and HIT event generation
- Conversion via 8-bit SAR ADCs, 2 columns / ADC, saving space and power dissipation
- Configuration
 - Global for ADCs
 - Individual per pixel (threshold for HIT detection)
- LVDS communication via shift register up to 400MHz CLK
- Supports ADC/DAC inputs and outputs (for calibrator voltage reference output, charge injection for calibration, temperature sensor)



Analog pixel front end

- **Charge integration**

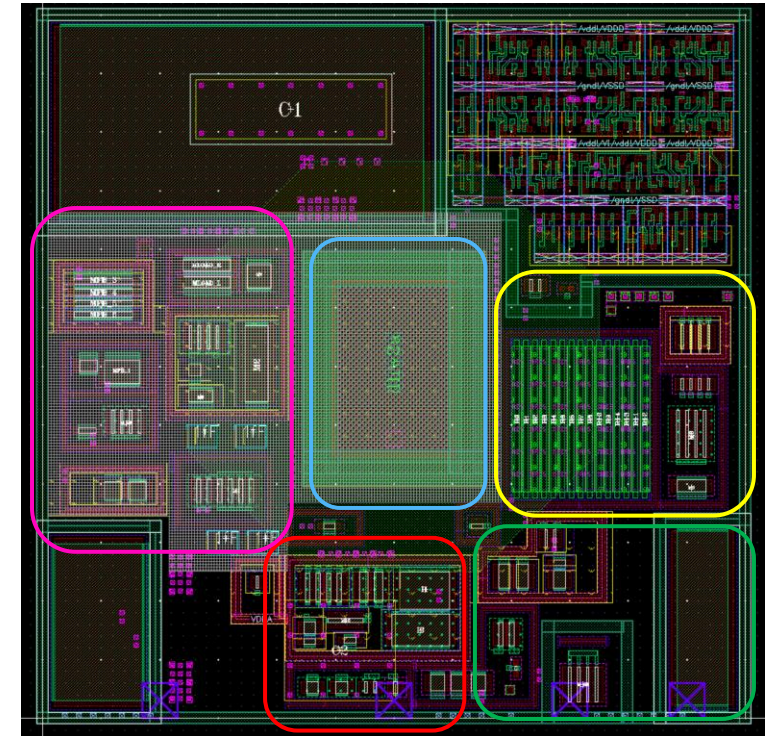
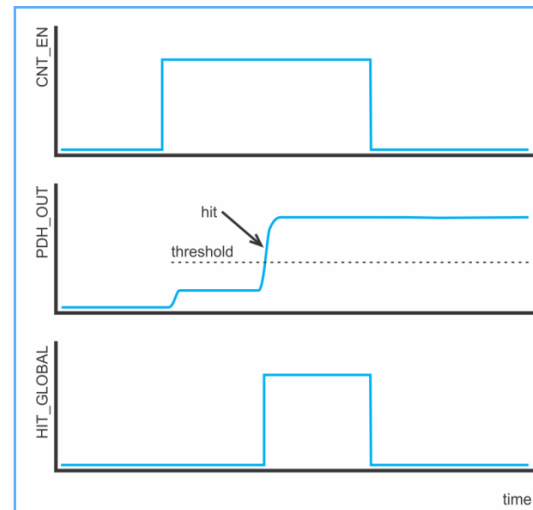
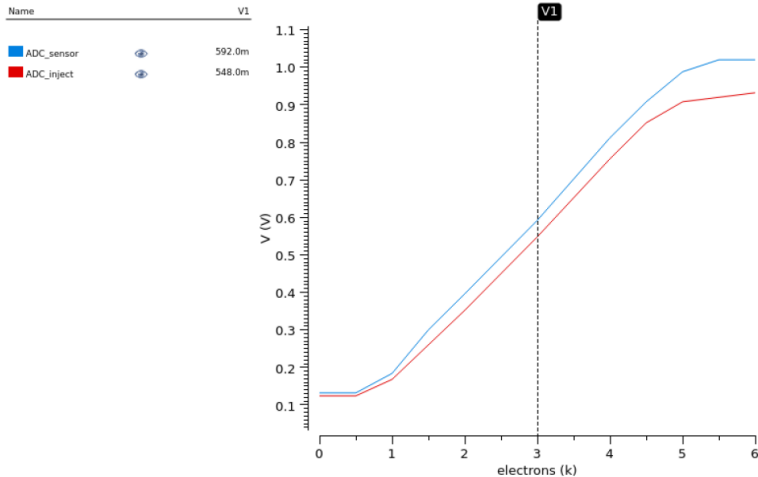
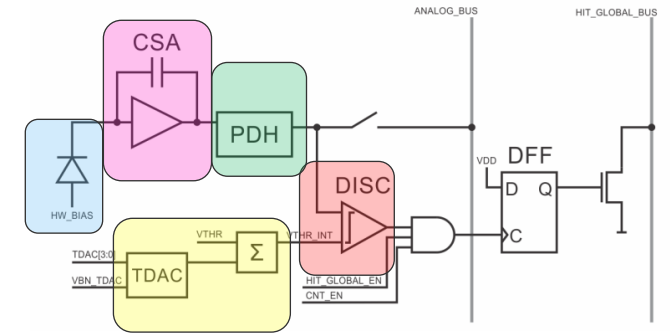
Charge generated in the sensor diode is integrated by a pixel-level front end circuit.

- **Peak Detector Hold (PDH)**

Stores the maximum peak charge (energy of the event) during exposure

- **Per-pixel thresholding**

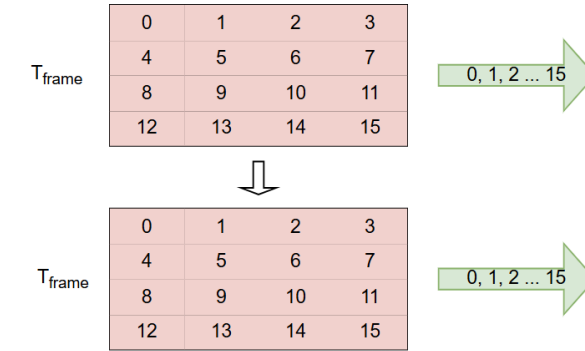
Local discriminator compares stored energy to a programmable threshold and sets the HIT signal.



Sampling modes

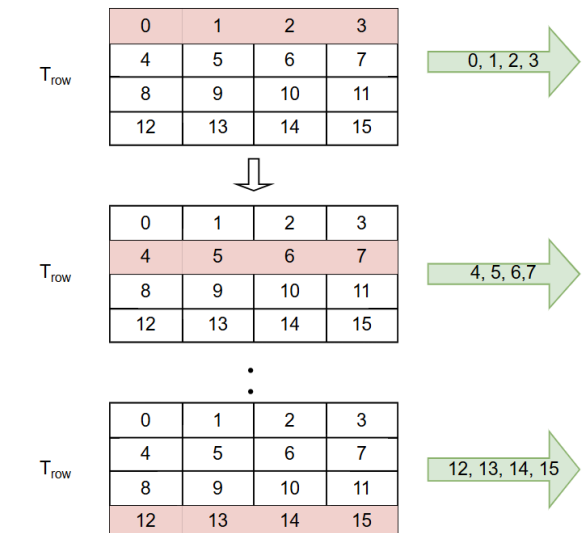
Frame mode

- Exposure separated from digitization and readout
- Precisely defined exposure time
- Good position and timing resolution
- Minimal analog–digital cross-talk during exposure



Rolling shutter mode

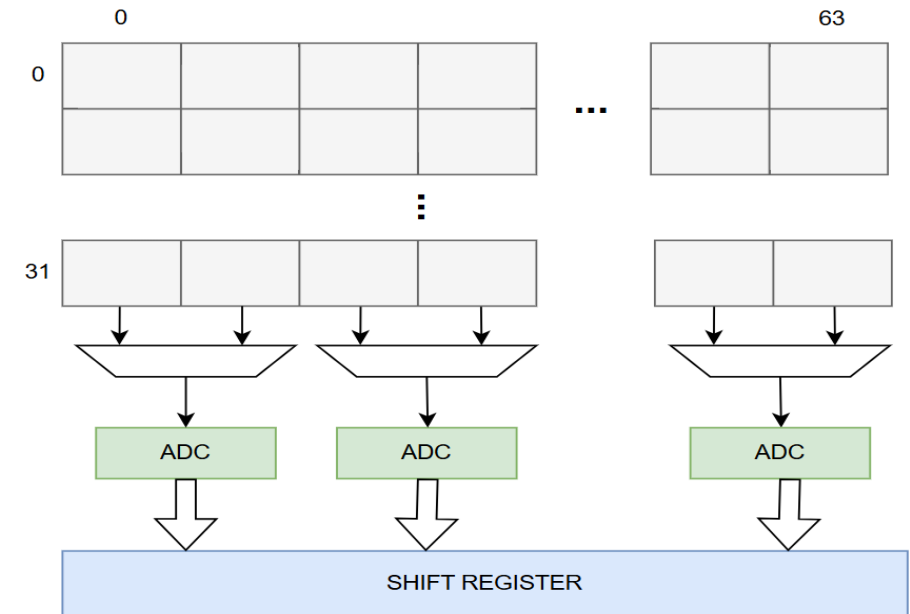
- Exposure during digitization and readout
- Minimal dead time
- Worse position and timing resolution
- Analog–digital cross-talk during exposure



Pixel dead time:
 $T_{\text{row}} < T_{\text{frame}}$

Data acquisition

- **Row-by-row digitization**
Pixel values are digitized one row at a time
Same mechanism used in frame and rolling shutter modes.
- **Column conversion**
Two columns share one ADC, 32 ADCs for 64 pixels.
Enables high throughput without global analog bottleneck.
- **Frame formation**
Digitized rows are stored in a shift register.
Complete frame is streamed via LVDS interface.

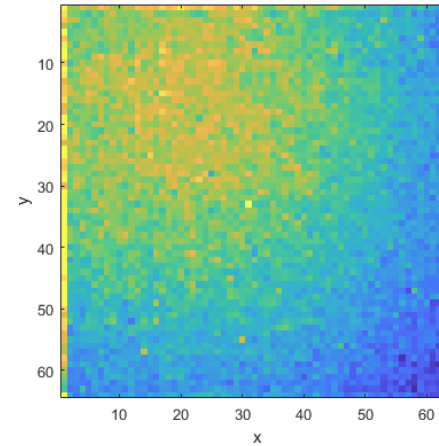


Calibration & characterization

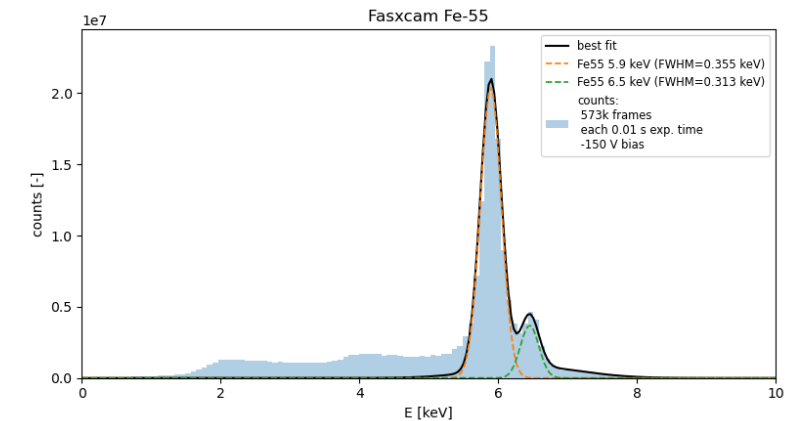
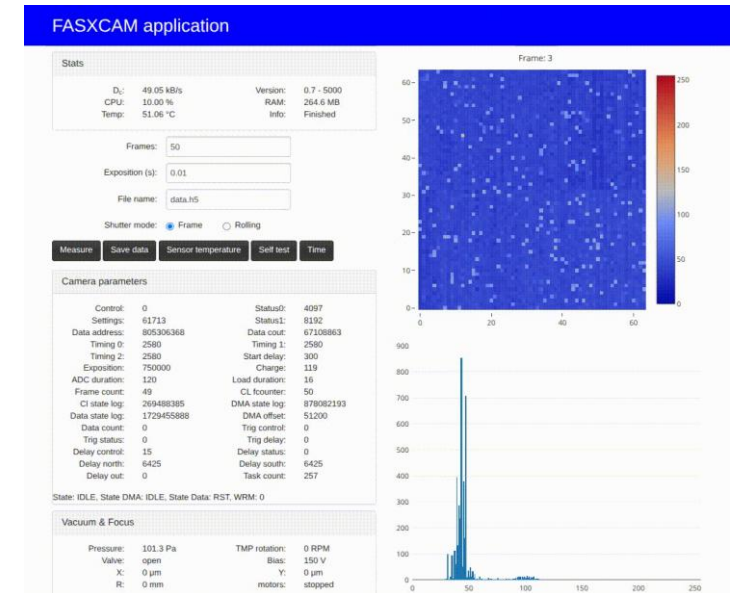
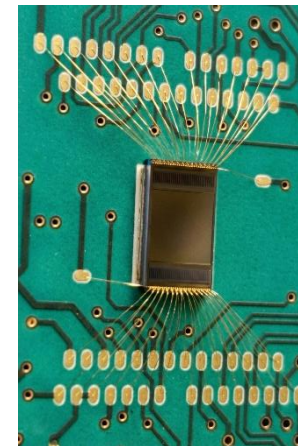
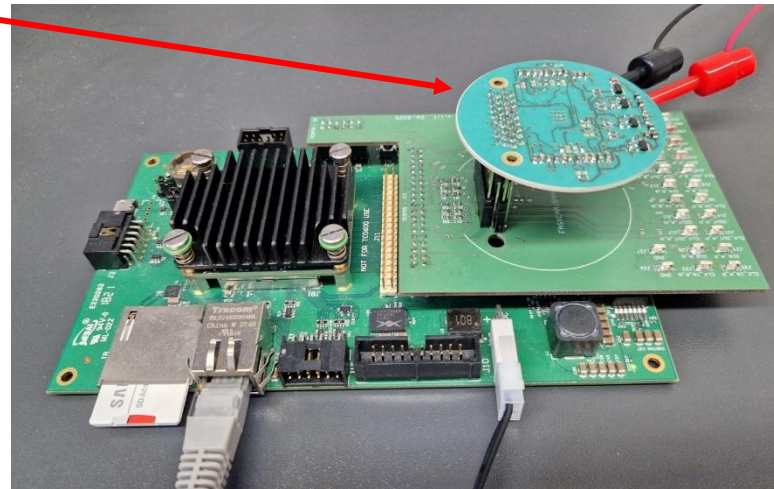
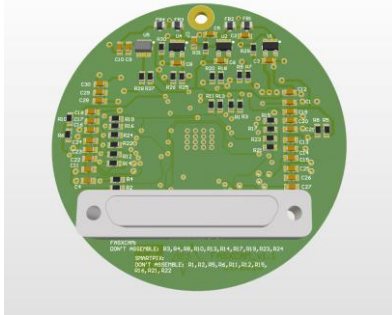
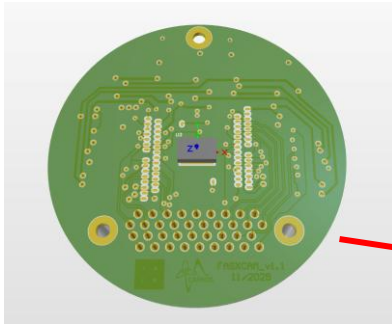
- **Characterization and calibration is currently work in progress.**
- Manufacturing variations
- Calibration done by charge injection and defined radiation sources
- ADCs and front-end electronics biasing need to be properly adjusted
 - FASXCAM supports hardware configuration
- Noise components and offset must be evaluated
 - Done in post processing
 - Pedestal calculation and subtraction
 - Common node noise correction
- QE and noise TBD. Noise estimation 20 to 50 electrons.

Test application

Prototype of a readout setup developed by Institute of Plasma Physics and CAPADS group at FNSPE CTU.

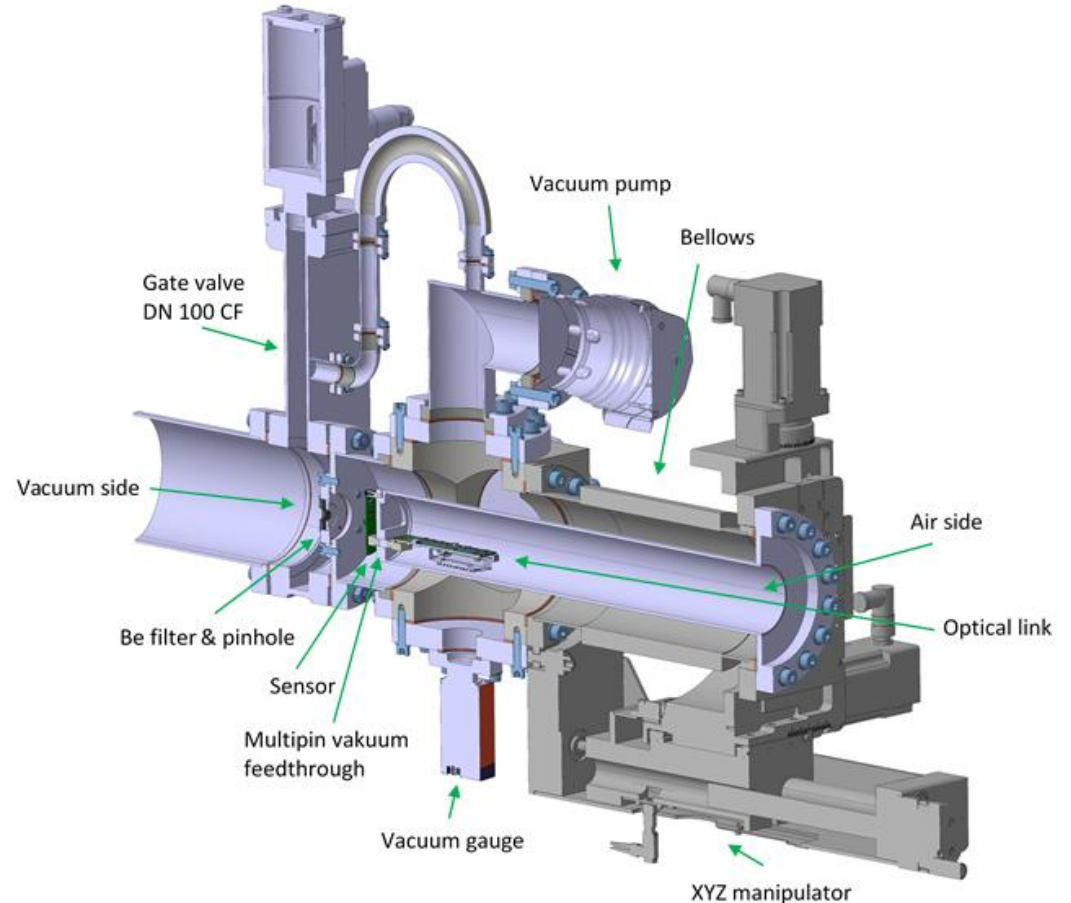
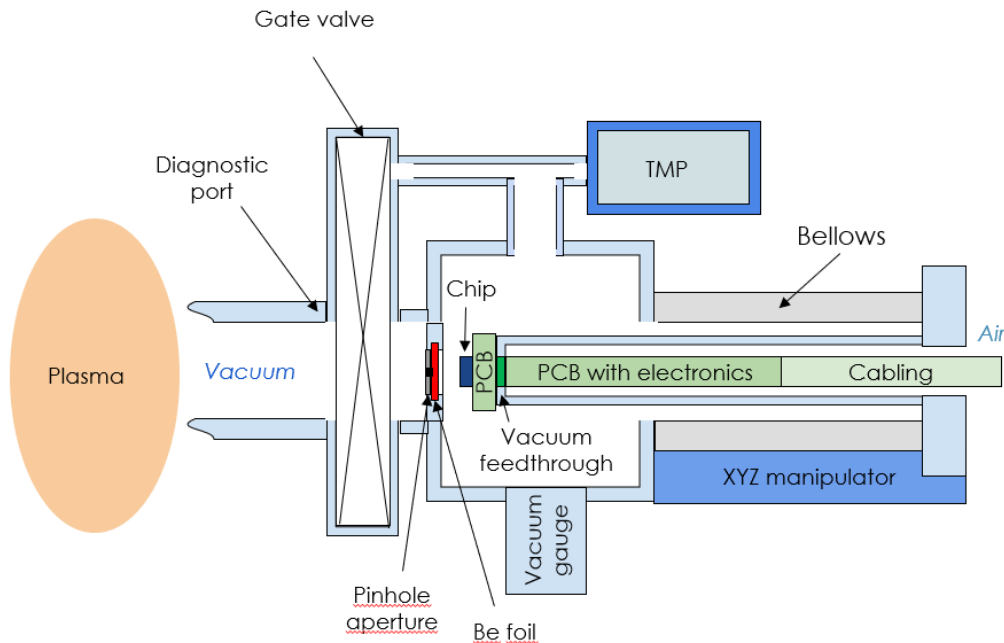


A circular board with the FASXCAM detection chip and auxiliary components (voltage regulators, voltage references). This board will be used in the final solution for the vacuum environment



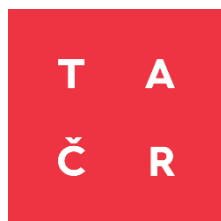
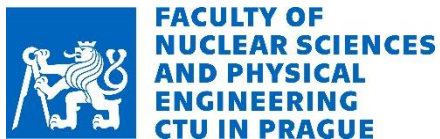
Planned research application

Ultra-fast soft X-ray sensorics for spectral monitoring of high-temperature plasmas



Project by Institute of Plasma Physics of the Czech Academy of Sciences

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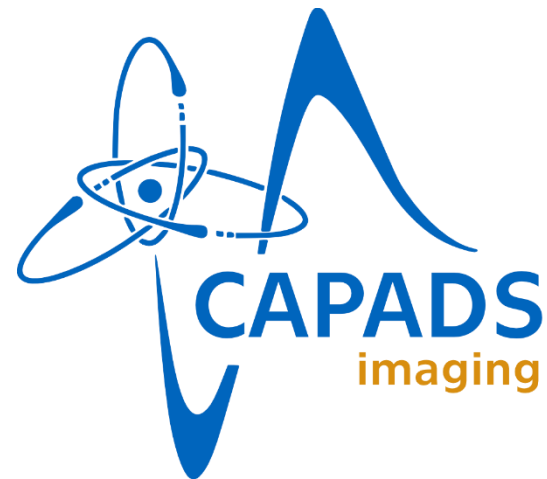
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Thank you for your attention!



<https://capads.fjfi.cvut.cz>