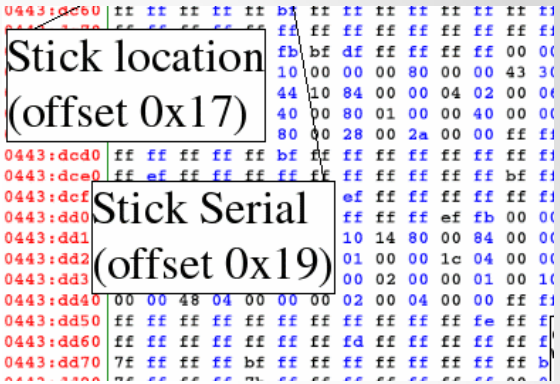
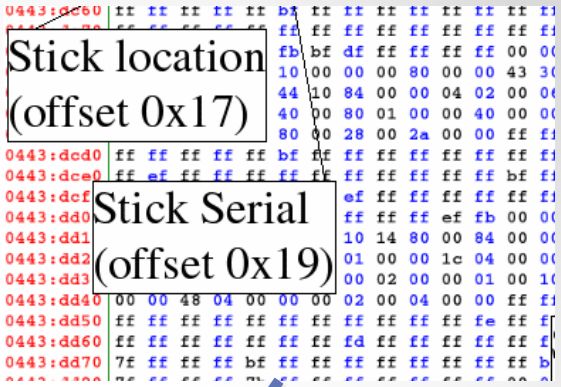


Mu3e Data Acquisition Ideas

Dirk Wiedner

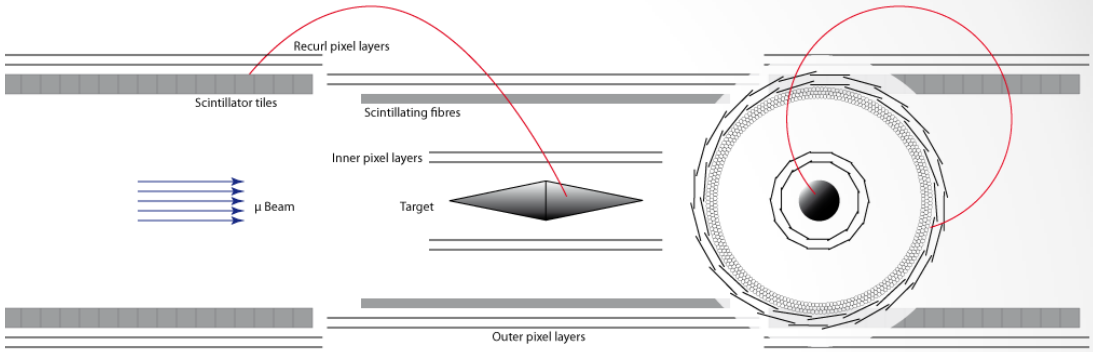
July 2012

Outline



- Readout Requirements
- Occupancies
- Pixel Readout Scheme
- Data Link Scheme
- Summary

Silicon Pixel Detector

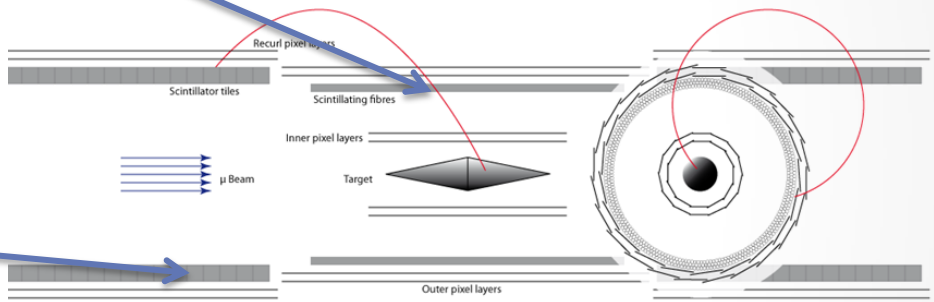


- Inner double layer
  - 12 and 18 stripes of 1 x 12 cm
- Outer double layer
  - 24 and 28 stripes of 2 x 36 cm
- Re-curl layers
  - 24 and 28 stripes of 2 x 72 cm
  - Both sides (x2)

180 inner sensors
4680 outer sensors

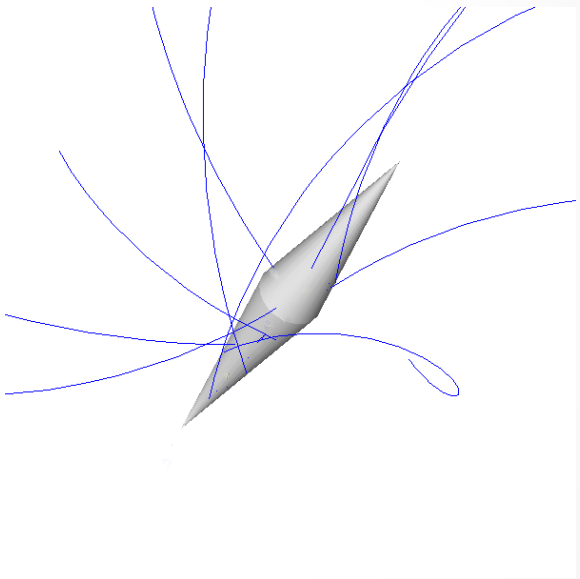
Timing Detectors

- Scintillating fiber hodoscope
  - 250 µm fibers
  - 5 layers
  - ➢ O(7500) fibers
- Timing tiles
  - 1 x 1 cm tiles
  - O(7000) tiles
- DRS5 readout



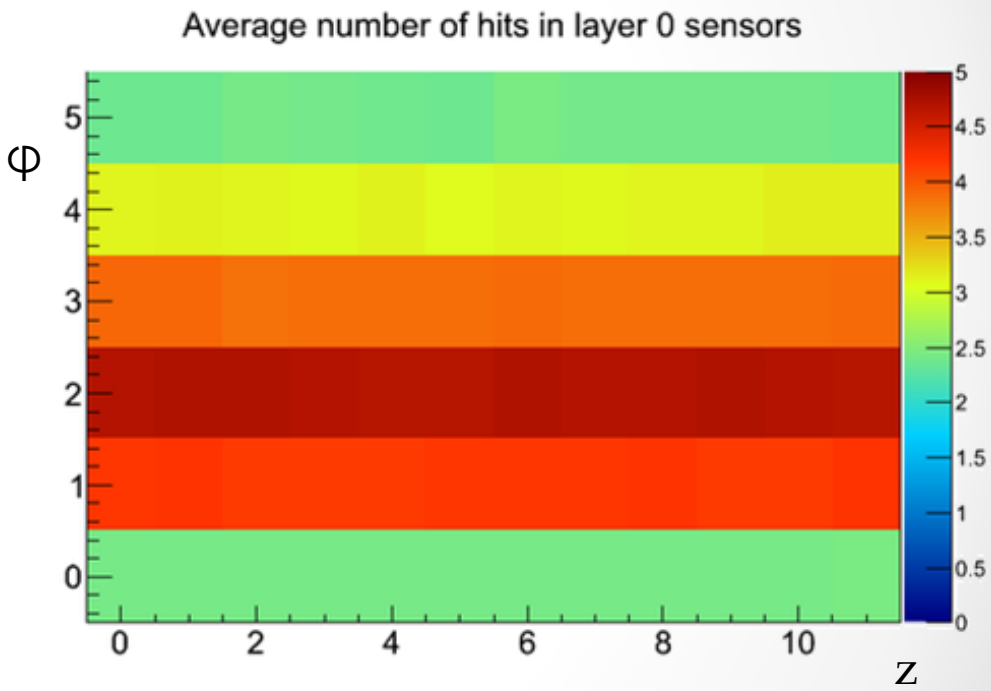
Readout Requirements

- 2.5 GHz muon decays
- 50 ns readout frames
- O(5000) pixel chips
  - 800 Mb/s readout links
- O(7500) fibers
- O(7000) timing tiles
  - DRS readout
- Online filtering



Maximum Occupancies

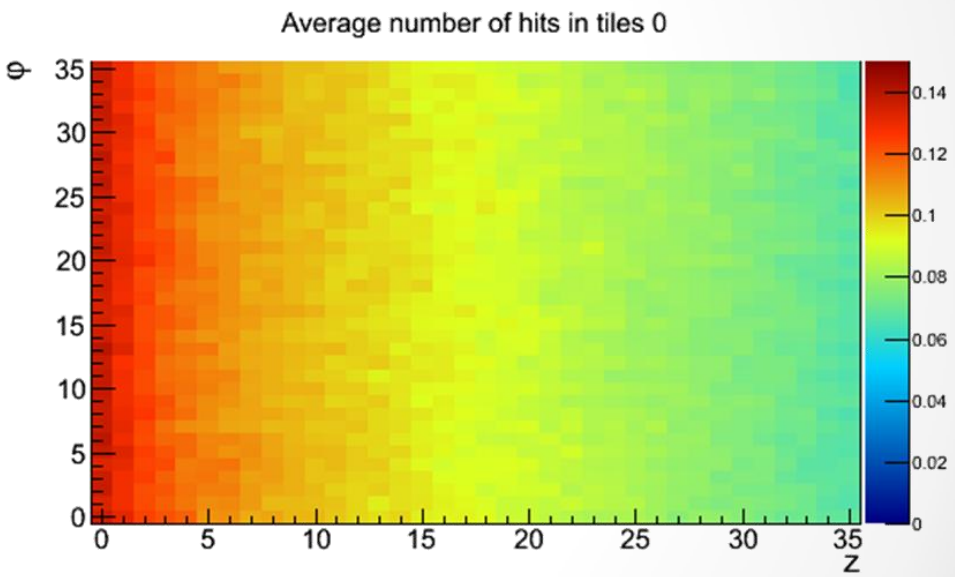
- All numbers per frame of 50 ns
- Vertex detector
  - 5 hits per sensor
- Central silicon tracker
  - 2 hits per sensor
- Recurl stations
  - 1 hit per sensor
- Fiber hodoscope
  - 0.24 hits per fiber
- Timing tiles
  - 0.14 hits per tile



Vertex occupancies

Average Occupancies

- All numbers per frame of 50 ns
- Vertex detector
  - 2 hits per sensor
- Central silicon tracker
  - 0.6 hits per sensor
- Recurl stations
  - 0.13 hit per sensor
- Fiber hodoscope
  - 0.16 hits per fiber
- Timing tiles
  - 0.09 hits per tile

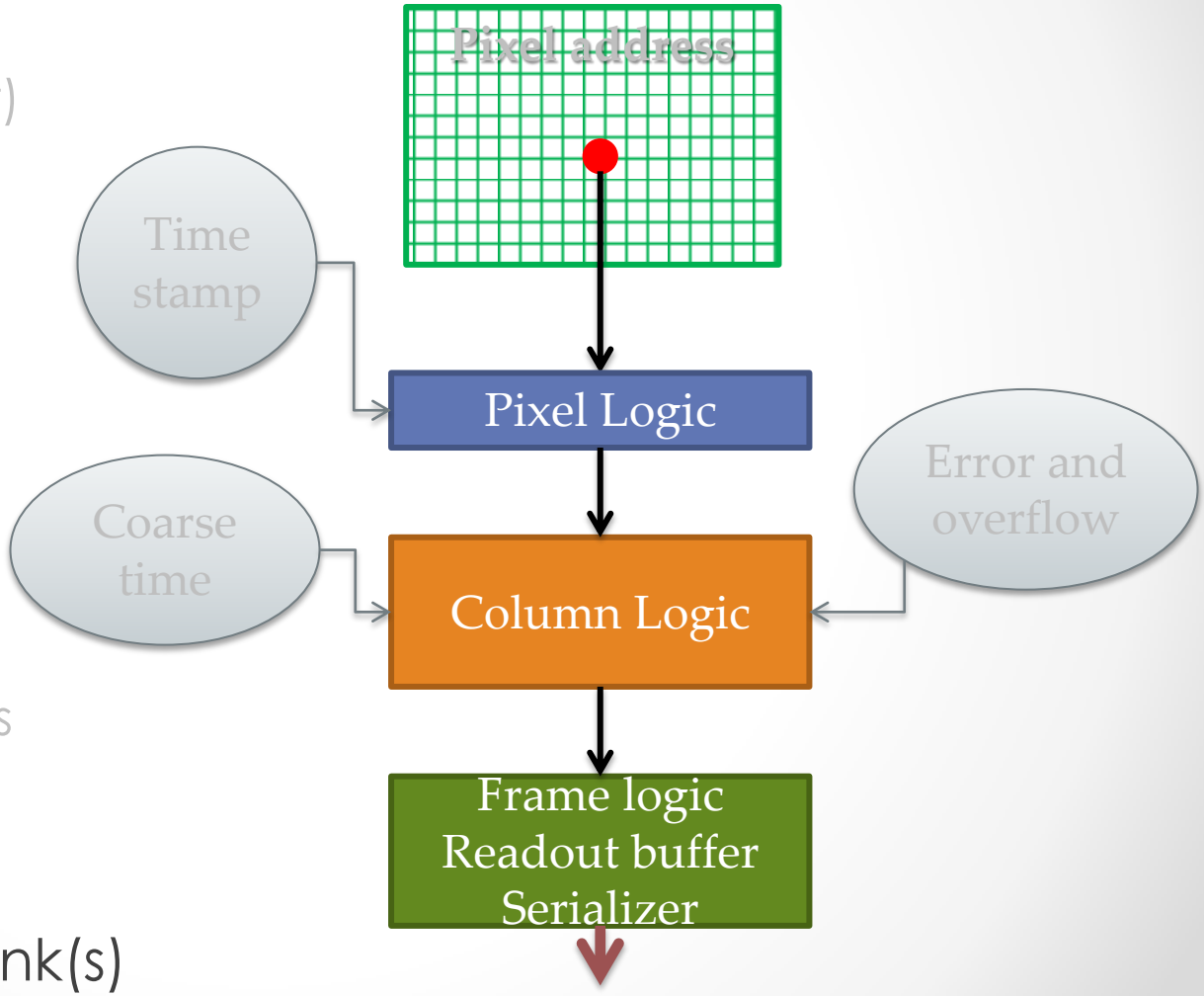


Tile occupancies

Pixel Readout Scheme

Pixel Readout Scheme

- Pixel logic
  - Pixel address (8 bit)
  - Fine time (4 bit)
  - 50 ns frames
- Column logic
  - Pixel data
  - Column address
  - Coarse time
  - Error bits
- Frame logic
  - Super Frame
  - Contains 16 x 50 ns readout frames
  - + Sensor header
- Readout buffer
- Serializer and fast link(s)



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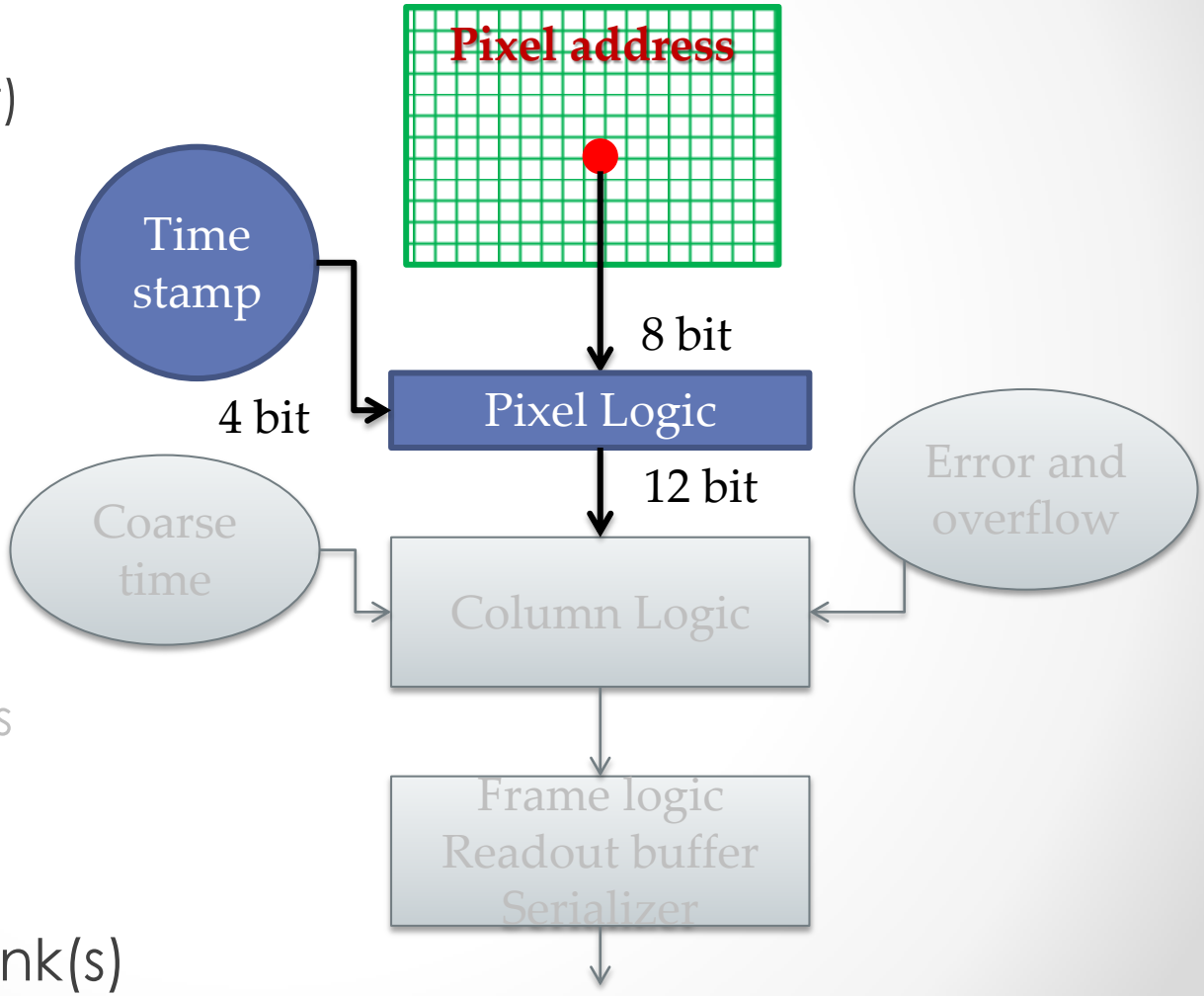

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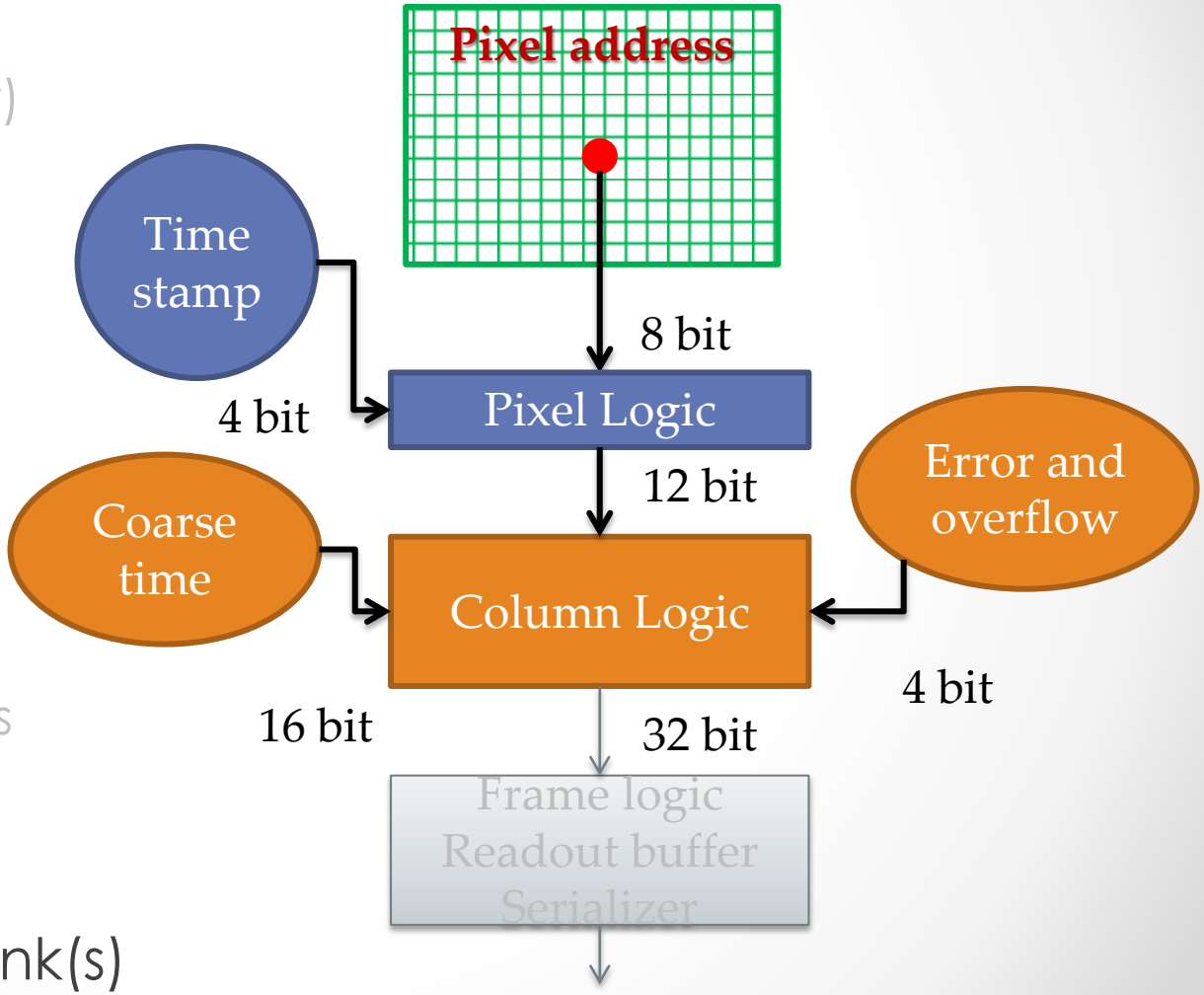

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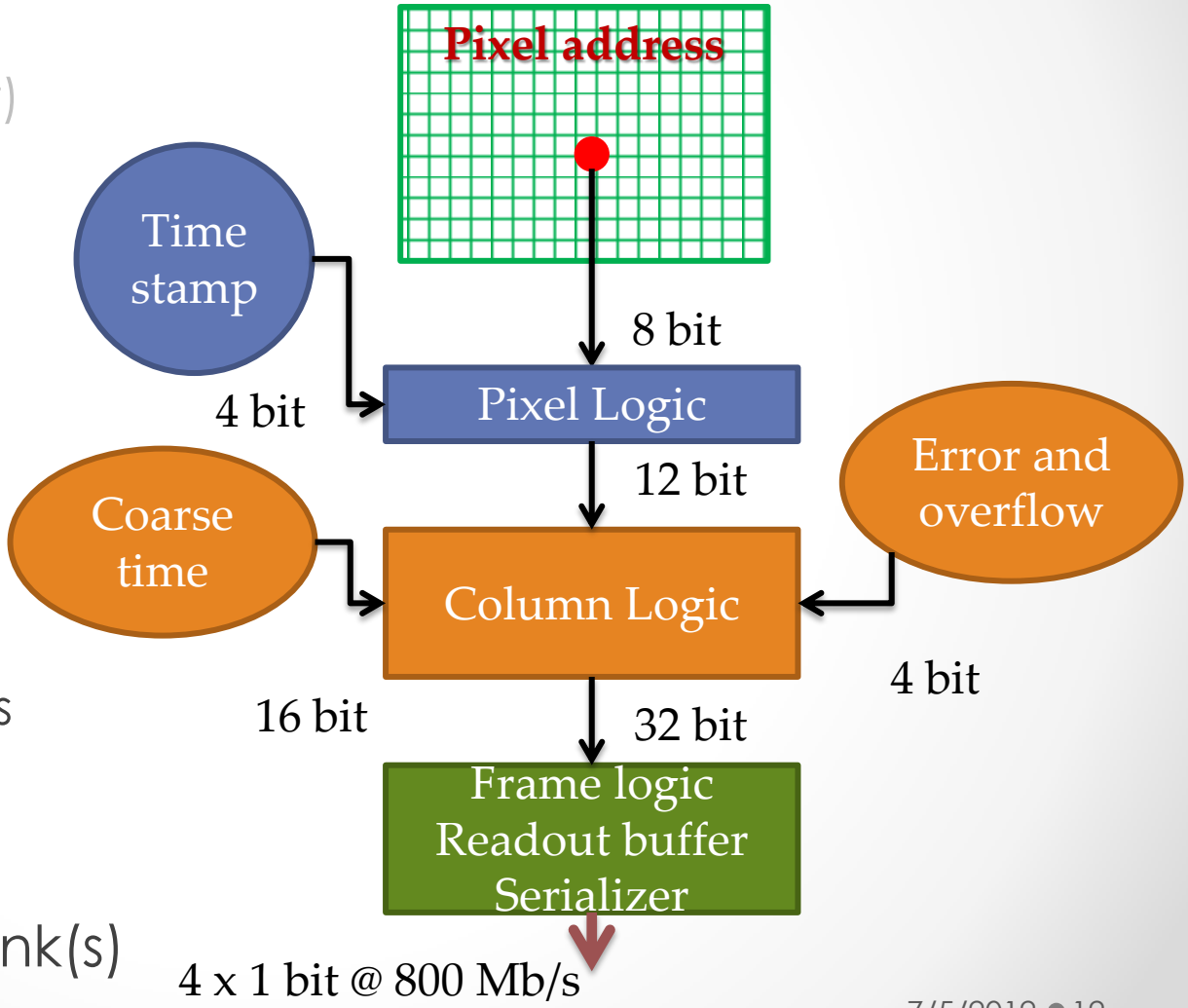
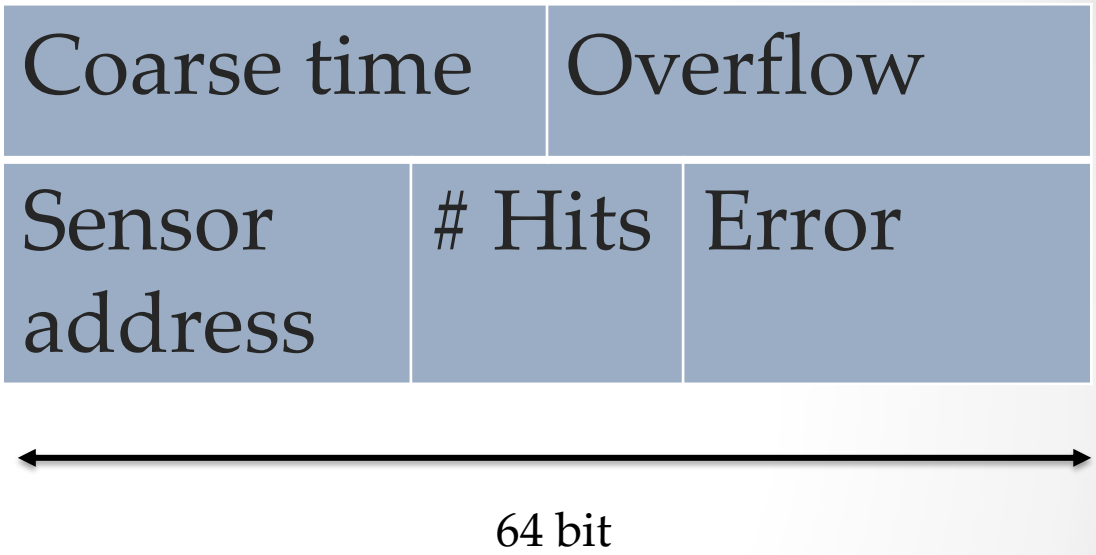


Super Frame Header

- Coarse time
  - 16 bit
- Sensor address
  - 16 bit
- Number of hits
  - 10 bits
- Sub-frame overflow
  - 16 bit
  - If more than 63 hits per frame
- Error propagation
  - 6 bits
- 64 bits in total



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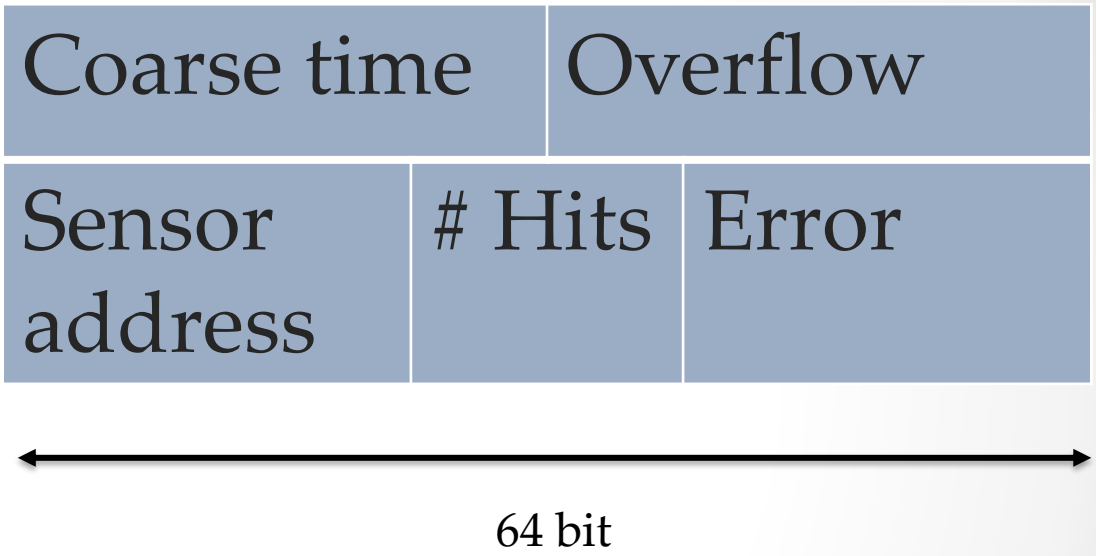


Super Frame Data

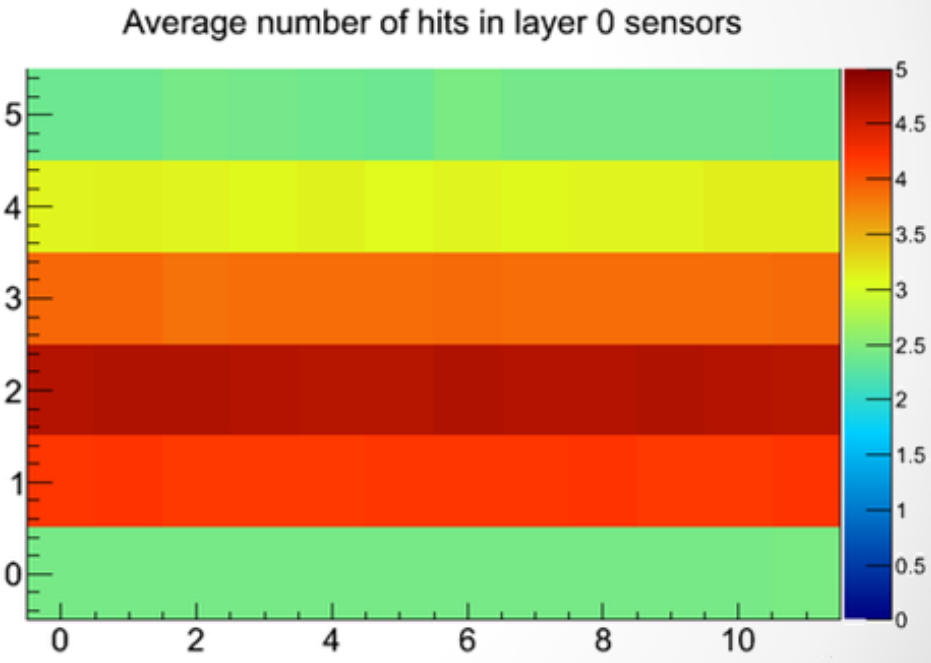
- Data from 16 frames
  - 0.8 µs interval
- Fine time 4 bit
- Pixel address 16 bit
  - 8 rows
  - 8 columns
- Maximum of 1008 hits
  - Maximum of 20160 bits

Header			
Fine time	row	column	…
Fine time	row	column	…
…	…	…	…
Fine time	row	column	…

16 x 20 bit

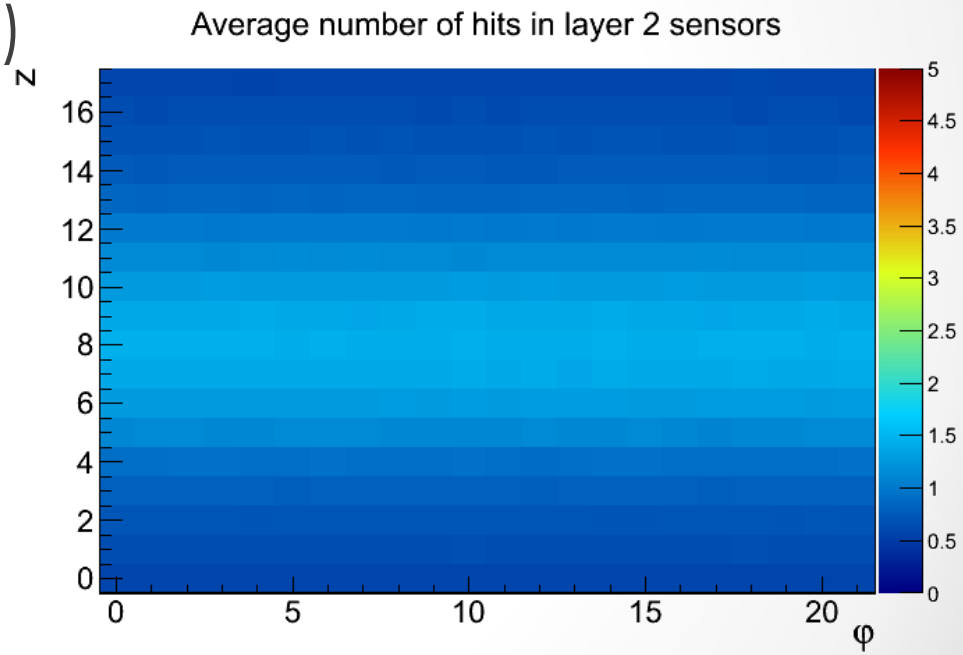
Number of Links Vertex

- Hottest region (average)
  - 5 hits per sensor / frame
- ➢ Super frame size:
  - 80 hits per super frame
  - ➢ 1664 bits average
- ➢ 2.6 Gb/s required
- i.e 4 x 800 Mb/s links per sensor



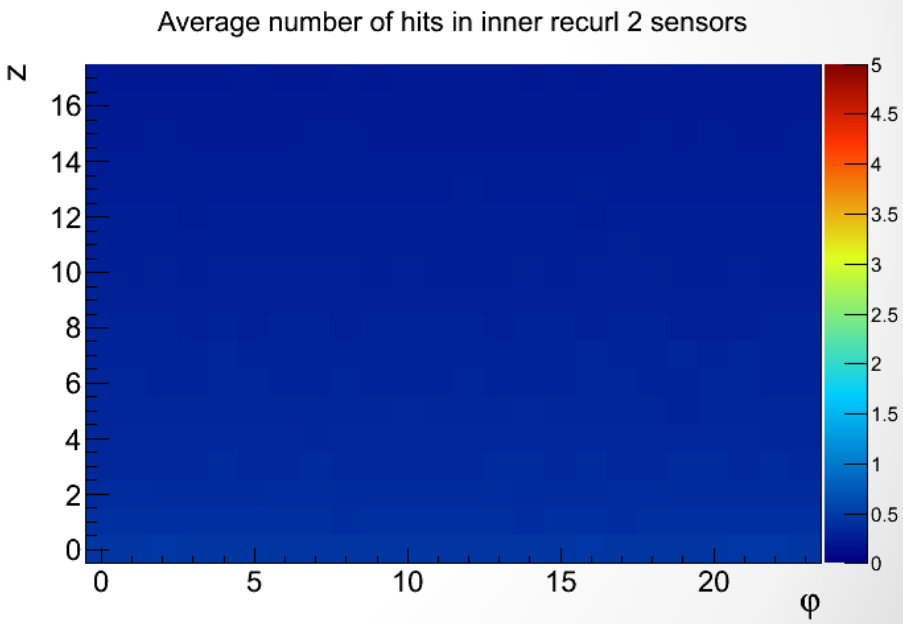
Number of Links Central Silicon Tracker

- Hottest region (average)
  - 2 hits per sensor / frame
- ➢ Super frame size:
  - 32 hits per super frame
  - ➢ 704 bits average
- ➢ 1.1 Gb/s required
- i.e 2 x 800 Mb/s links per sensor



Number of Links Recurl Stations

- Hottest region (average)
  - <0.25 hits per sensor / frame
- ➢ Super frame size:
  - 4 hits per super frame
  - ➢ 144 bits average
- ➢ 0.225 Gb/s required
- i.e 1 x 400 Mb/s links per sensor

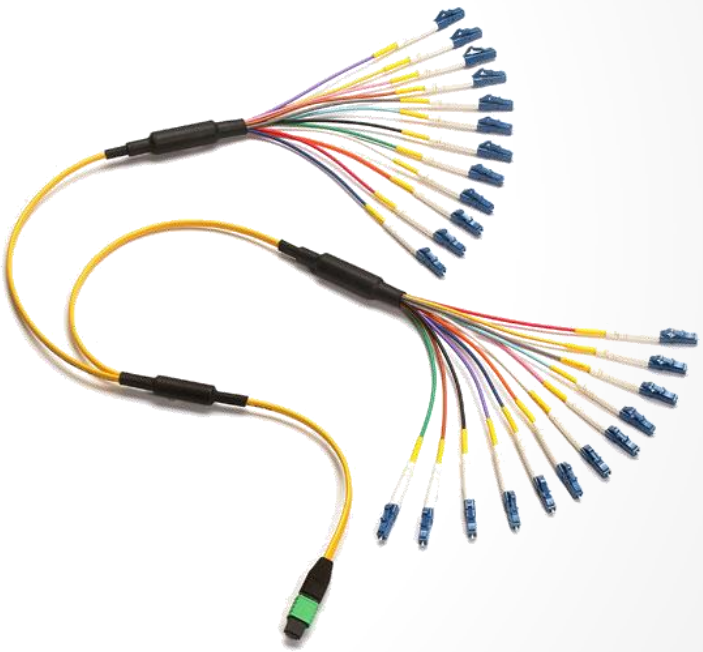


Data Link Scheme

…

Link Overview

- Front end links
  - Pixel sensor to on-detector FPGA
    - 400 – 800 Mbit/s
    - LVDS
  - Timing readout
    - See Stefan Ritt
- Optical links from detector
  - On-detector FPGAs
  - … to off-detector readout boards
  - 5 Gbit/s
- Optical links in counting room
  - Off-detector read out boards
  - …to PC Farm



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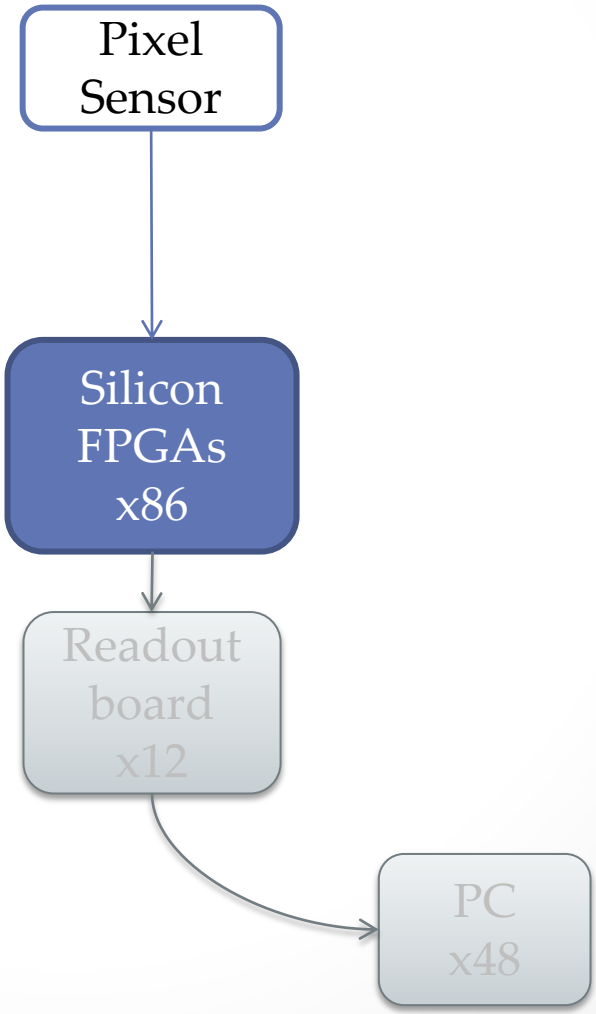

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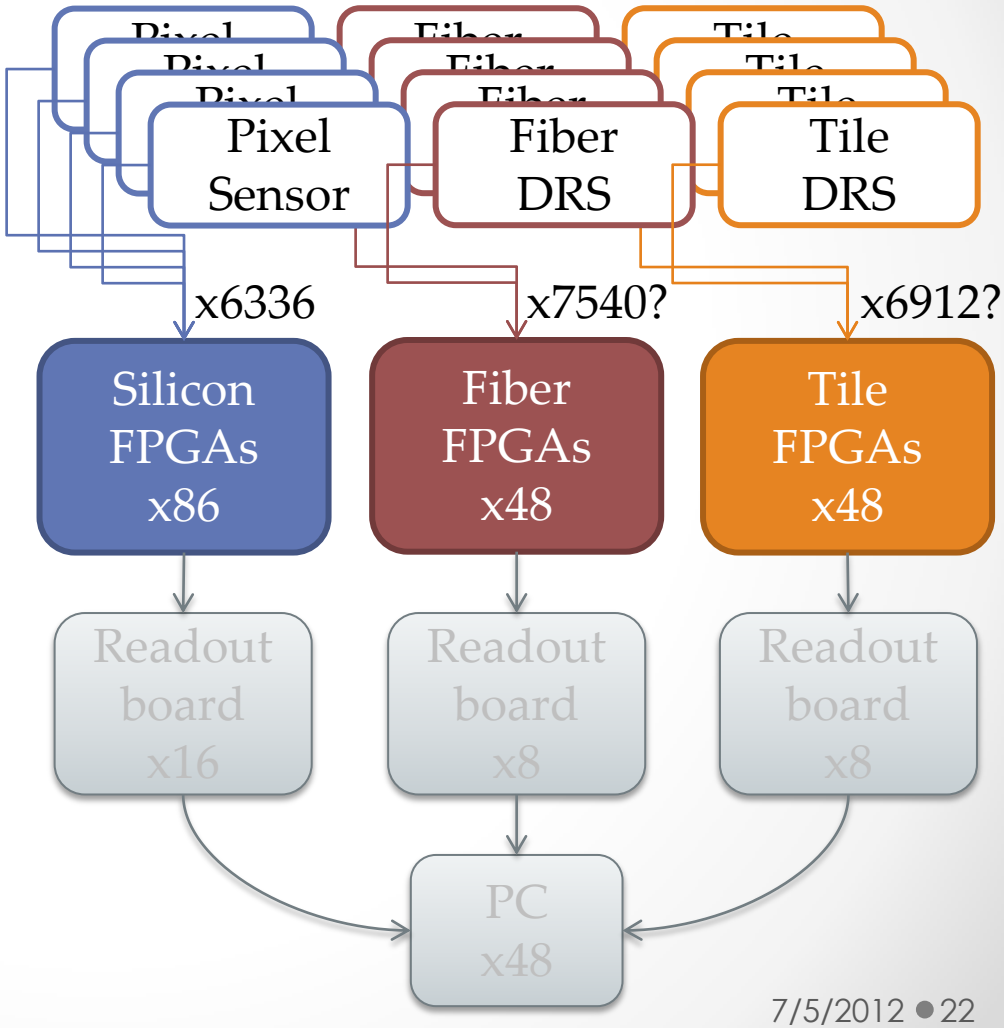

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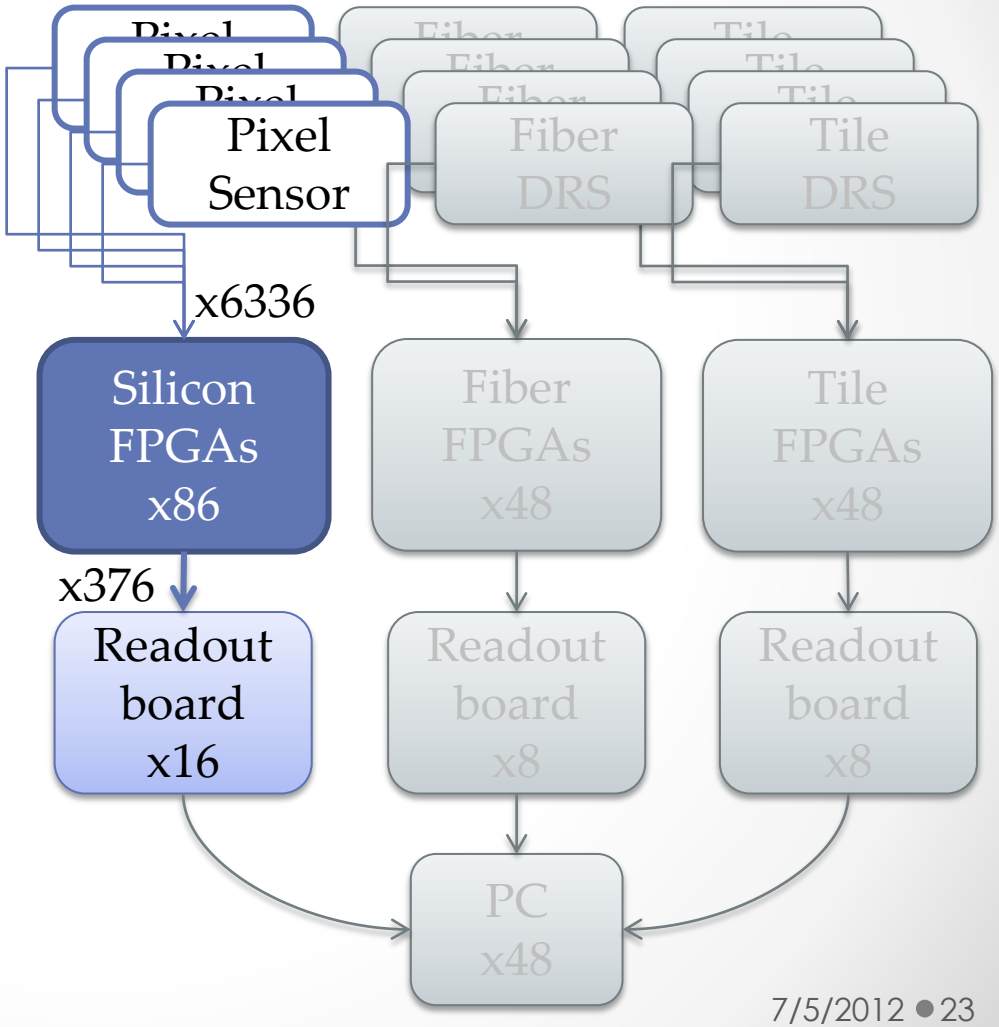

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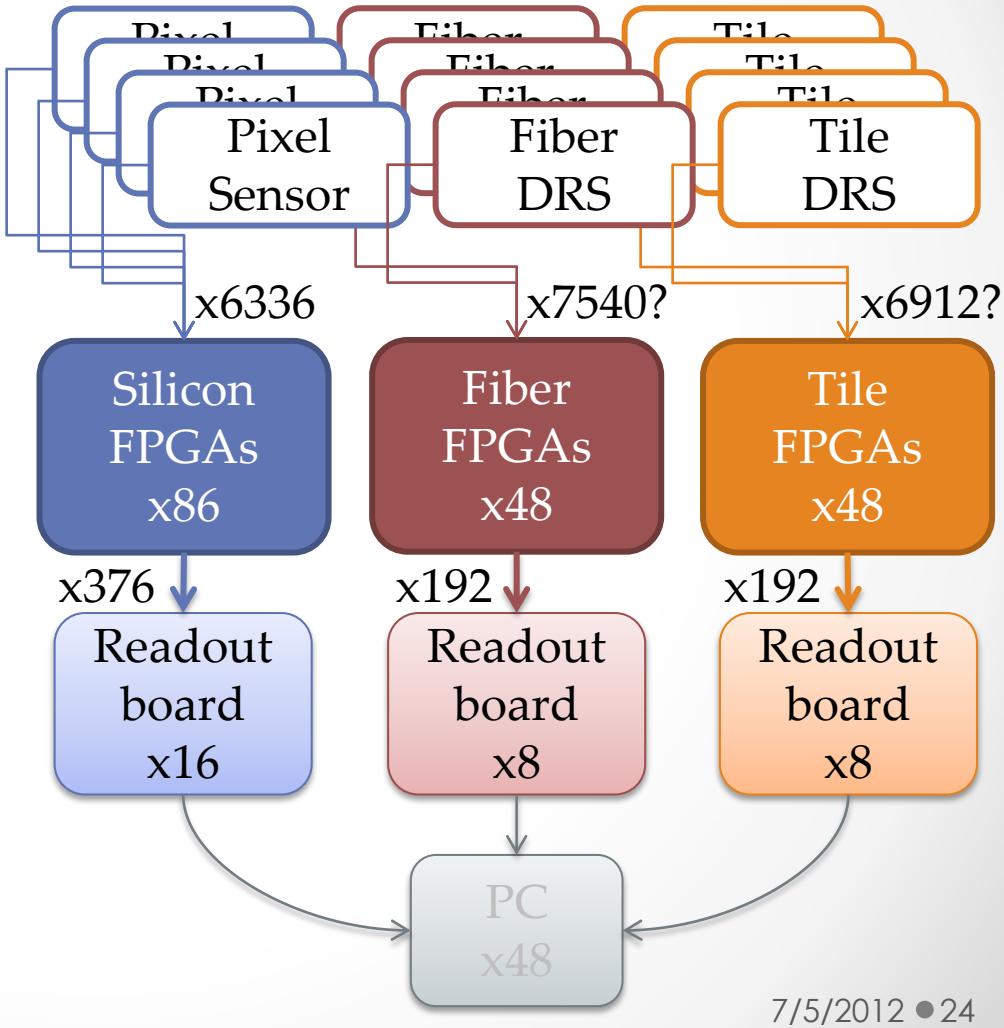

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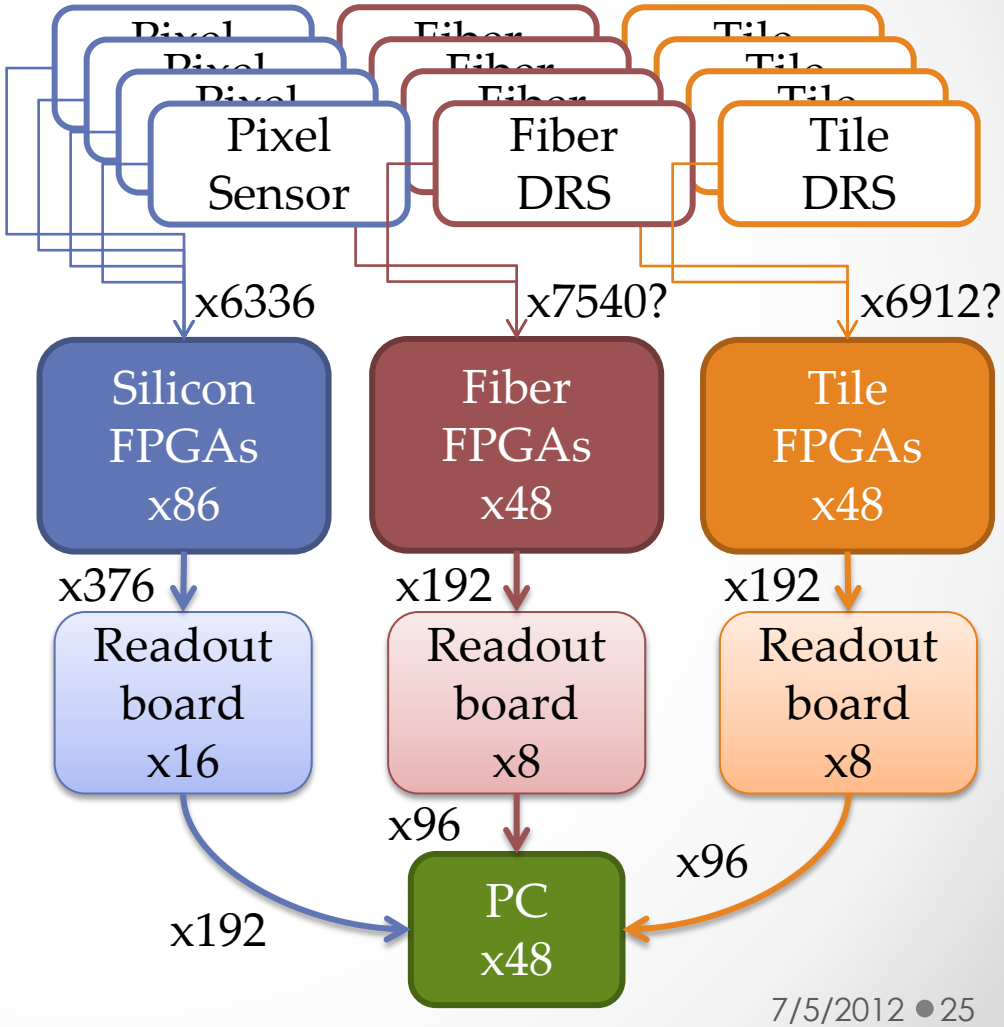
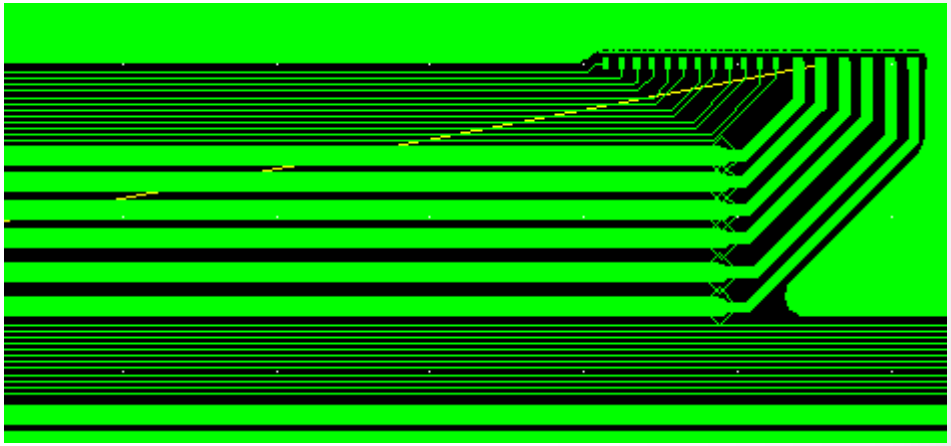


Pixel Sensor Links

- Vertex Sensor chips
  - 180 chips
  - 4 LVDS links
  - 800 Mbit/s per link
- Central Silicon Tracker
  - 936 chips
  - 2 LVDS links
  - 800 Mbit/s
- Recurl stations
  - 3744 chips
  - 1 LVDS link
  - 400 Mbit/s



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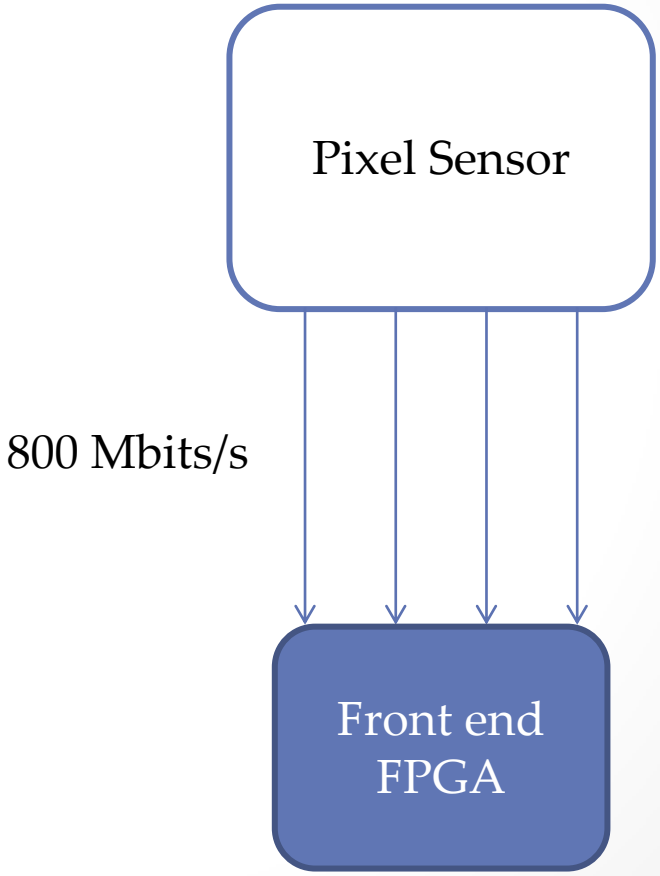

Front End FPGAs

- FPGAs on detector
  - 86 (+96) pieces
- Receive sensor data
  - 108 LVDS inputs
- 5 Gbit/s outputs
  - 8 optical links
  - … to counting house
- Switching between readout boards A-D

Optical transceiver FE board

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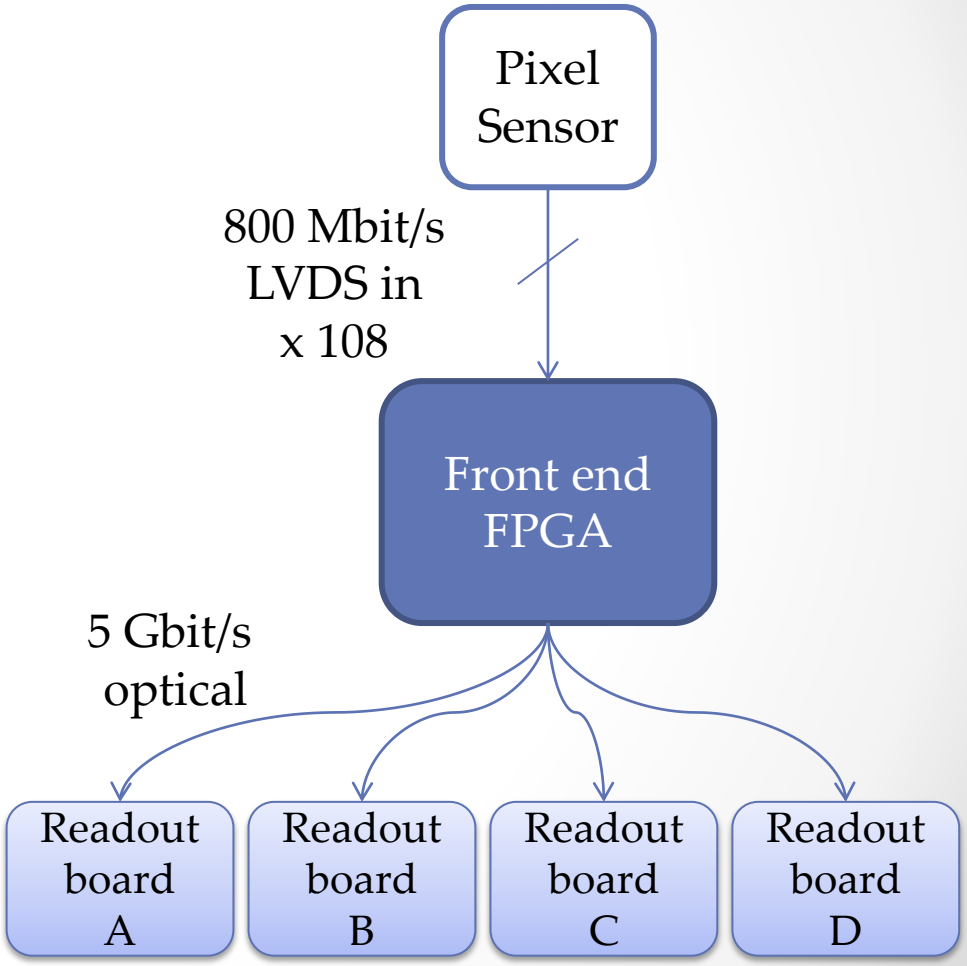
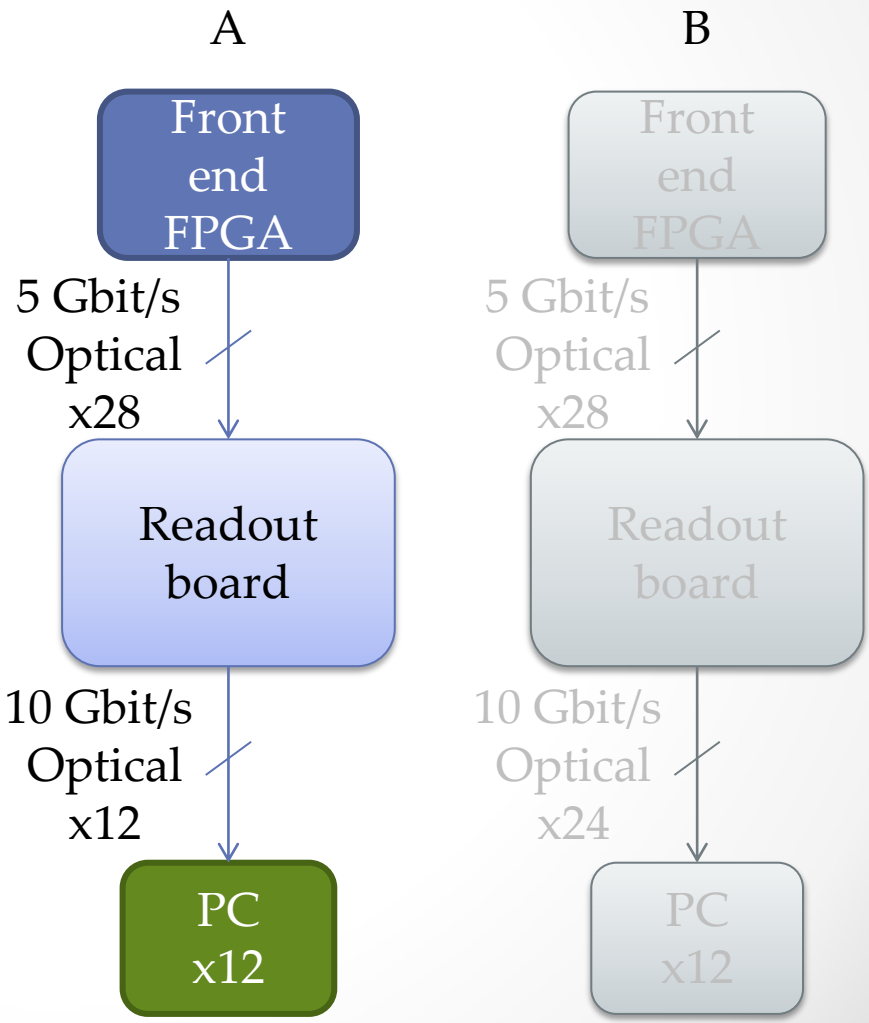


Readout Board

- FPGAs off detector
  - 32 pieces
- 5 Gbit/s optical input
  - 16-28 inputs
  - … from on detector FPGAs
- 10 Gbit/s optical output
  - 12 outputs
  - … to PCs
- Switching network
  - A-D sub-nets
  - One output per PC



GPU-PC

- PC with GPU
  - 48 pieces
- 10 Gbit/s Fiber input
  - 8 inputs
  - … from readout boards
- Switching network
  - One input per readout board
  - A-D subnets
- Data filtering
  - Timing trigger on FPGA
  - Data to tape < 100 MB/s

Optical mezzanine connectors

FPGA PCIe board

GPU computer

GPU-PC

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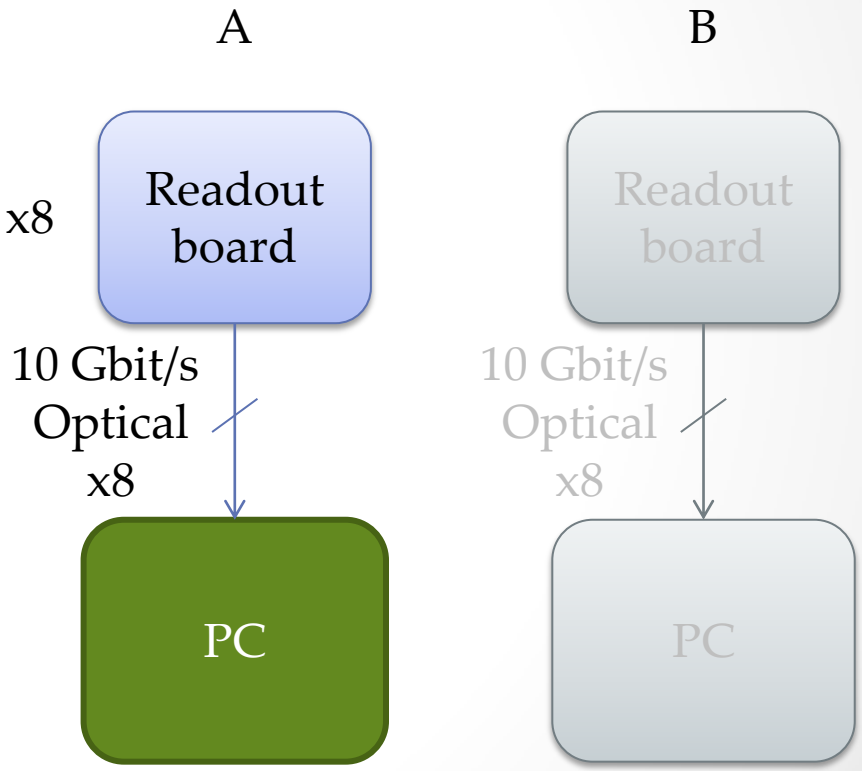
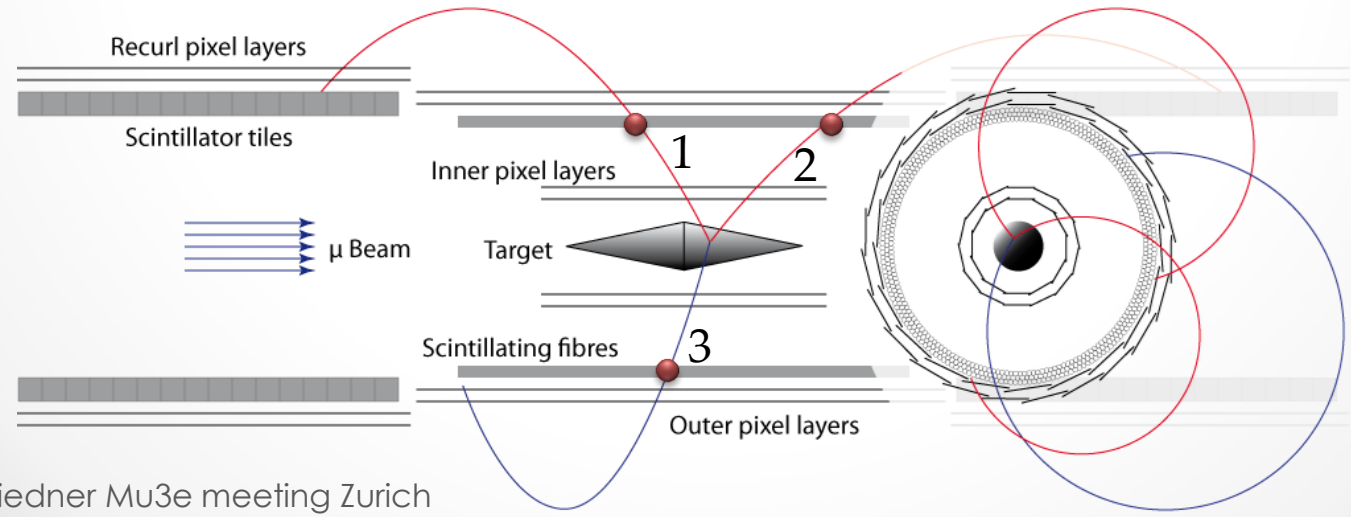
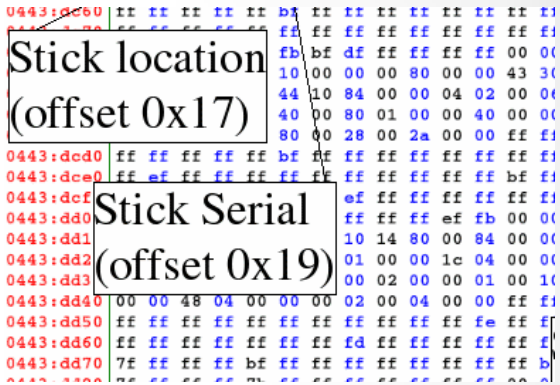


Timing Filter

- Entire event on PCIe FPGA
- Tile and Fiber data
  - Easy to match
  - Look for three hits
- Reject data without three hits
  - … inside time interval



Summary

- Occupancies simulated (Nik)
- Serial data from pixel sensors
- 800 Mbit/s LVDS links
- On detector FPGA boards
- Optical data transfer
- Read out board in counting room
- Switched optical network
- GPU PCs with optical inputs