Development of LAMBDA: Large Area Medipix-Based Detector Array

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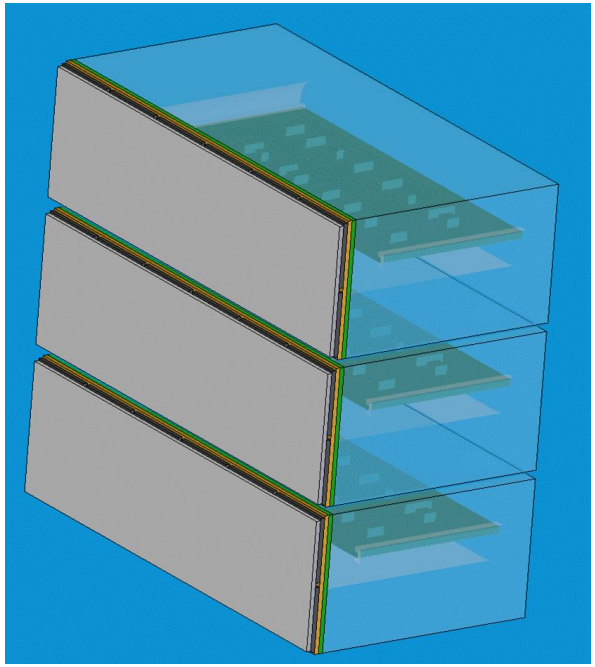
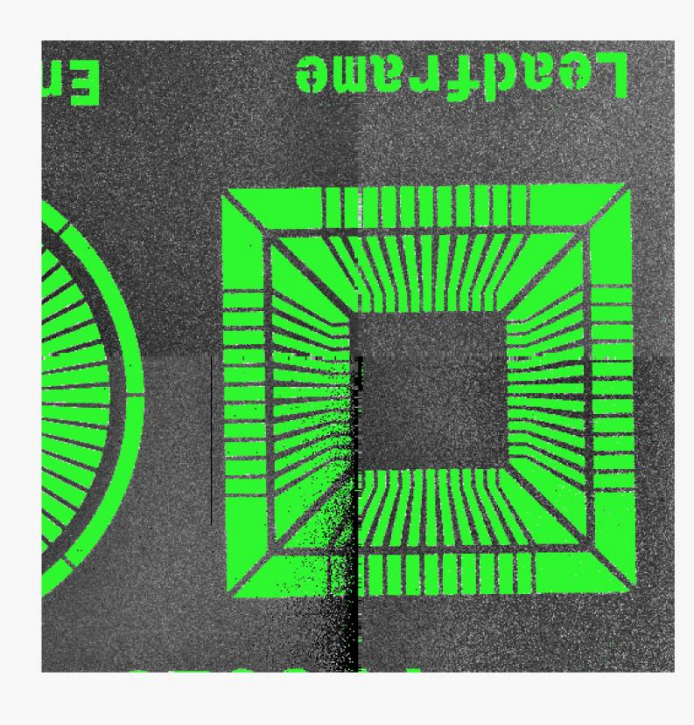


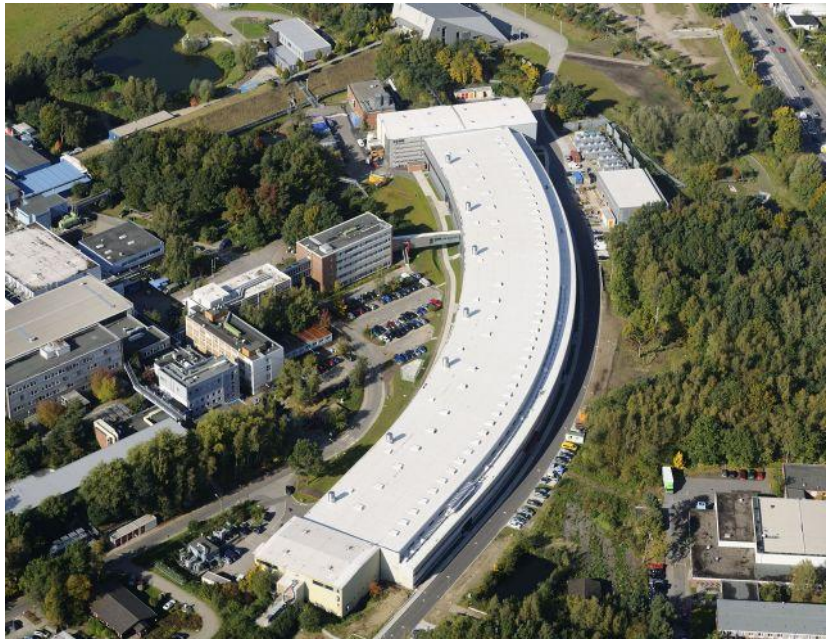


Large Area Medipix-Based Detector Array

- Motivation
- Detector design and current status of system
- Further developments
- Germanium pixel detector development

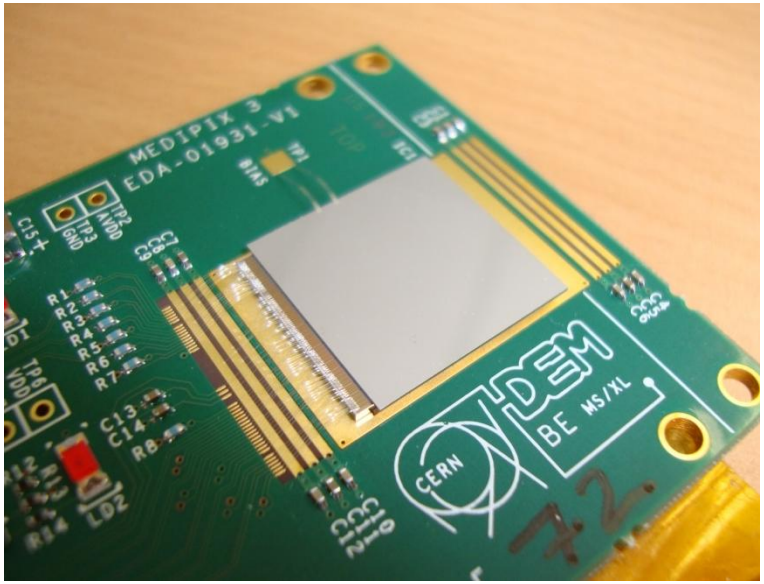
PETRA-III synchrotron

- New 3rd generation light source (2009)
- Aims of detector development
  - Improve on successes with silicon hybrid pixel detectors
  - Replace silicon with high-Z material for high energy beamlines



Medipix3 readout chip

- 21 groups in collaboration
  - Chip design at CERN
- Photon-counting chip
- 256 * 256 pixels, 55µm
- Continuous read-write (2000 fps with 12 bit counter depth)
- Charge summing using interpixel communication



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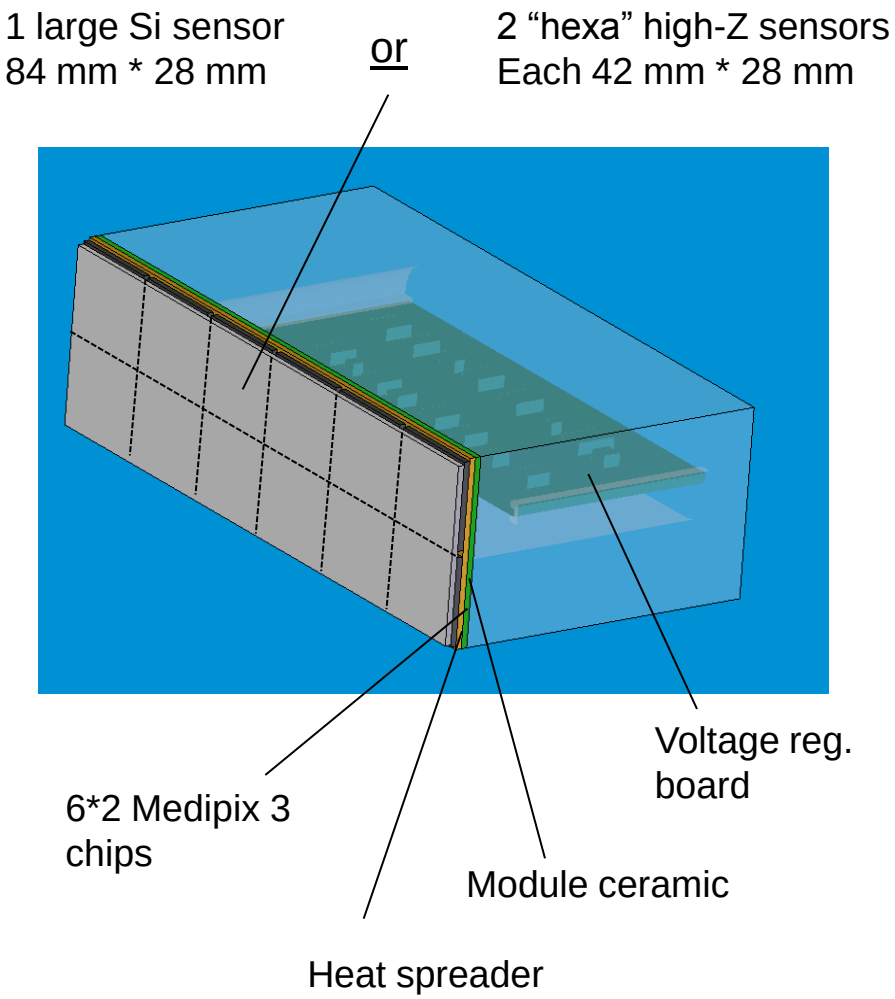
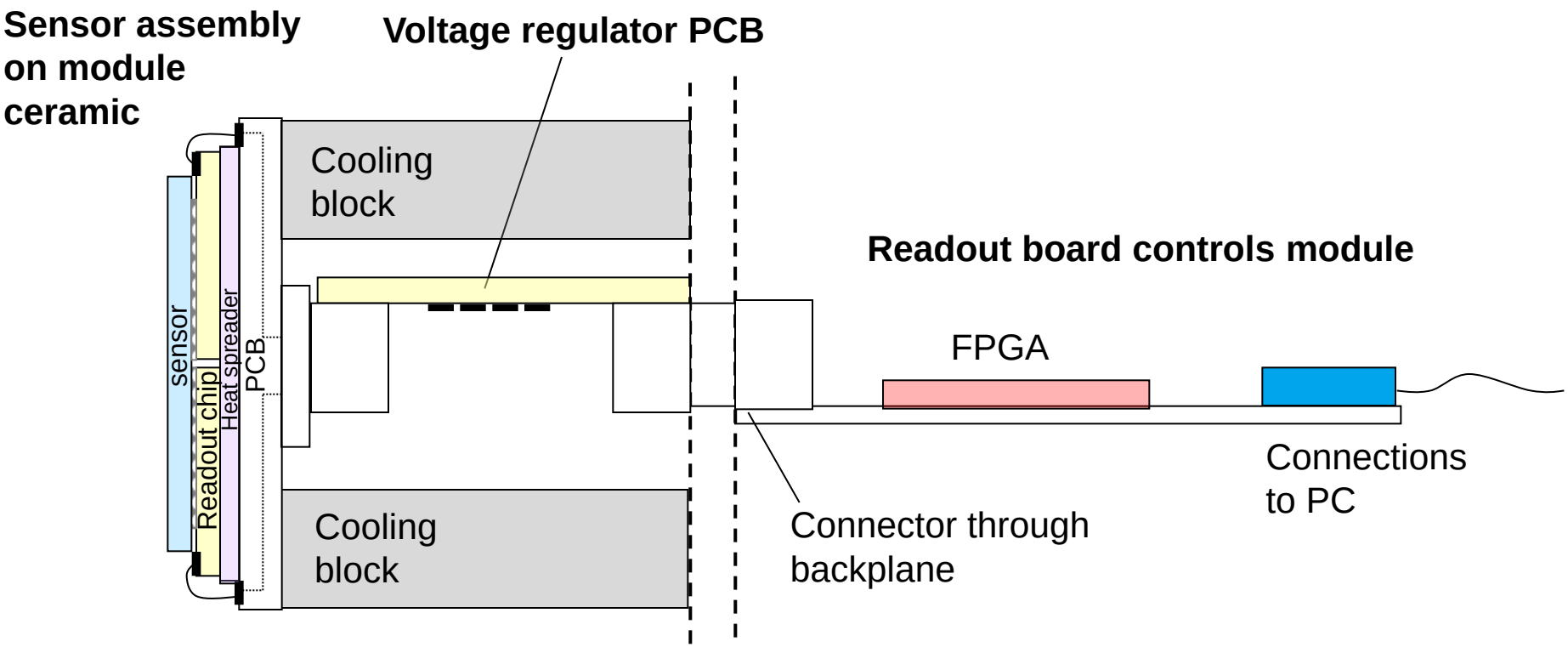
LAMBDA detector head

- 6-by-2-chip layout
  - Set by typical silicon and high-Z wafer sizes (6”, 3”)
- Tilable layout
  - Electronics behind sensor
- High-speed readout
  - All 8 readout pairs per chip used
- Cooling
  - Compatible with low-temperature operation (-60°C for germanium)



System design

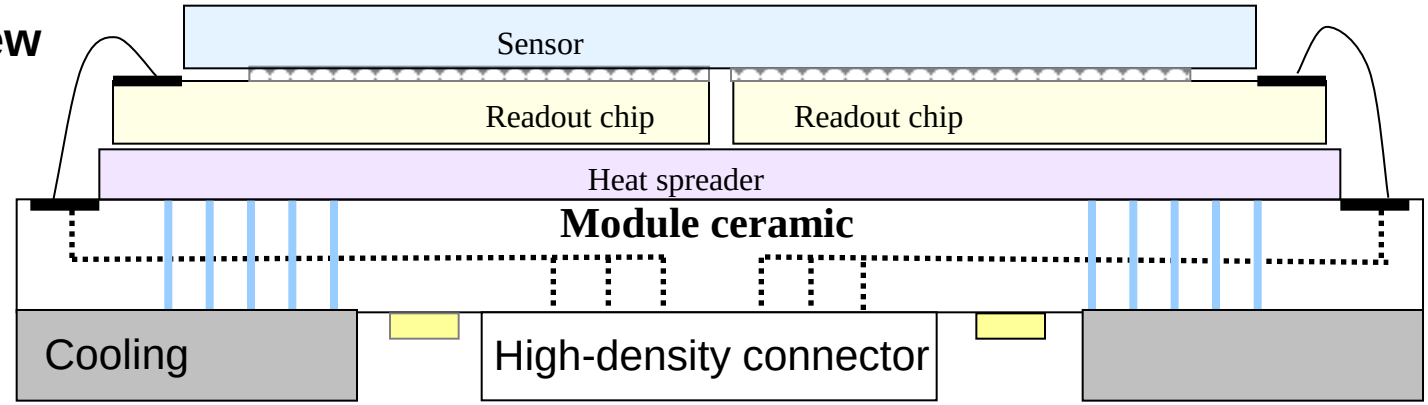


Initial readout board – USB2 readout, allows chip testing and firmware development

Final board – Board based on XFEL (AGIPD) developments with 10 GBE readout

Detector assembly and module ceramic PCB

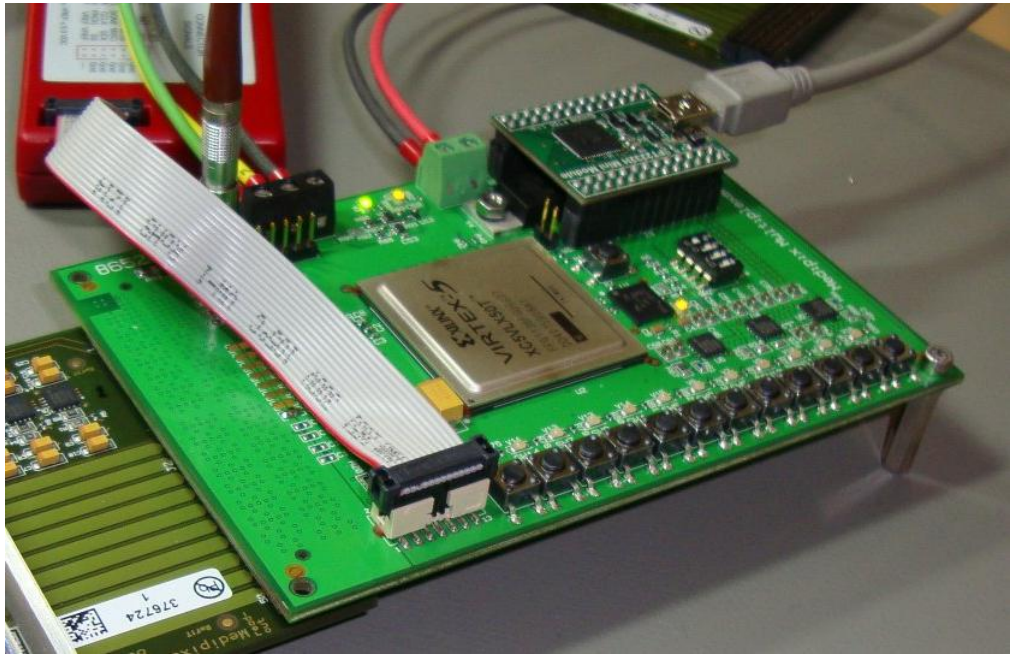
Side view

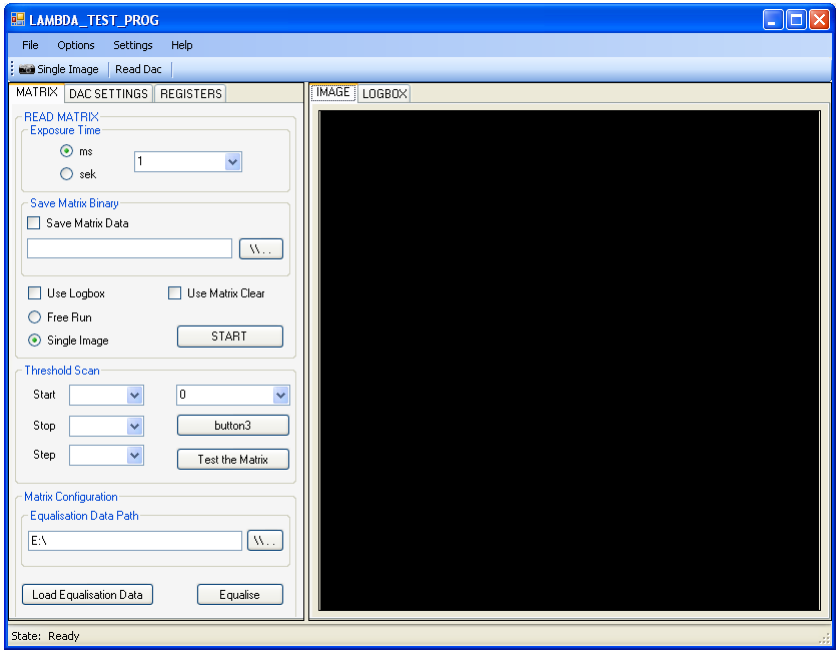


- Heat spreader to improve temperature uniformity
- Low-Temp Co-fired Ceramic (LTCC) board - KOA, Japan
  - Matching of CTE to sensor materials (6 ppm / K)
  - Heat coupling through board under each chip with thermal vias
- 500-pin Samtec high density right-angle connector

Current readout board

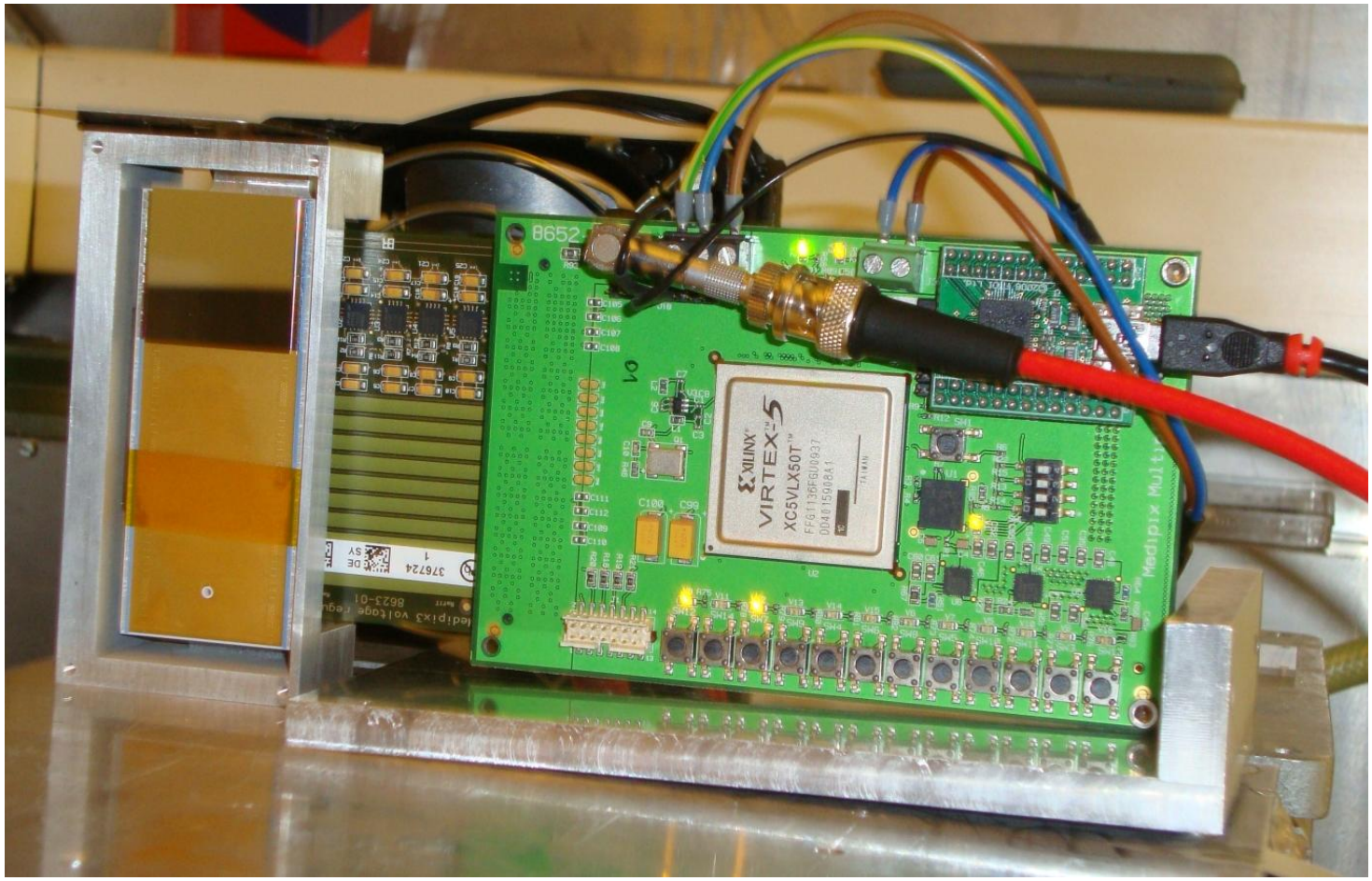
- Virtex-5 FPGA
  - Same series as FPGA for high-speed readout board
- USB2 readout
- PC control with C++ (functions called by simple GUI)





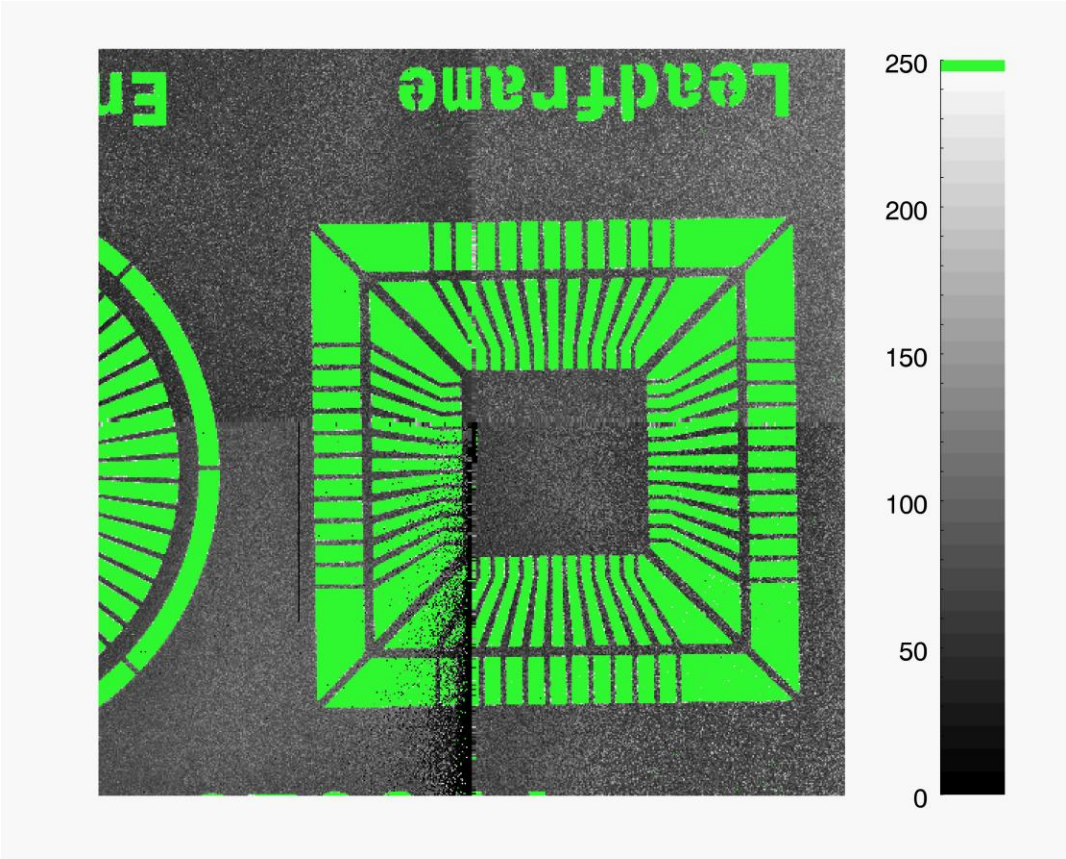
Current system

- Si Medipix3 2*2-chip assembly (300µm thick)
- Flat connector used, rather than right-angle



Detector test

- Detector is working
  - Standard functions implemented
  - Threshold equalisation running (but needs improvement)
- Test mask image taken with Mo X-ray tube



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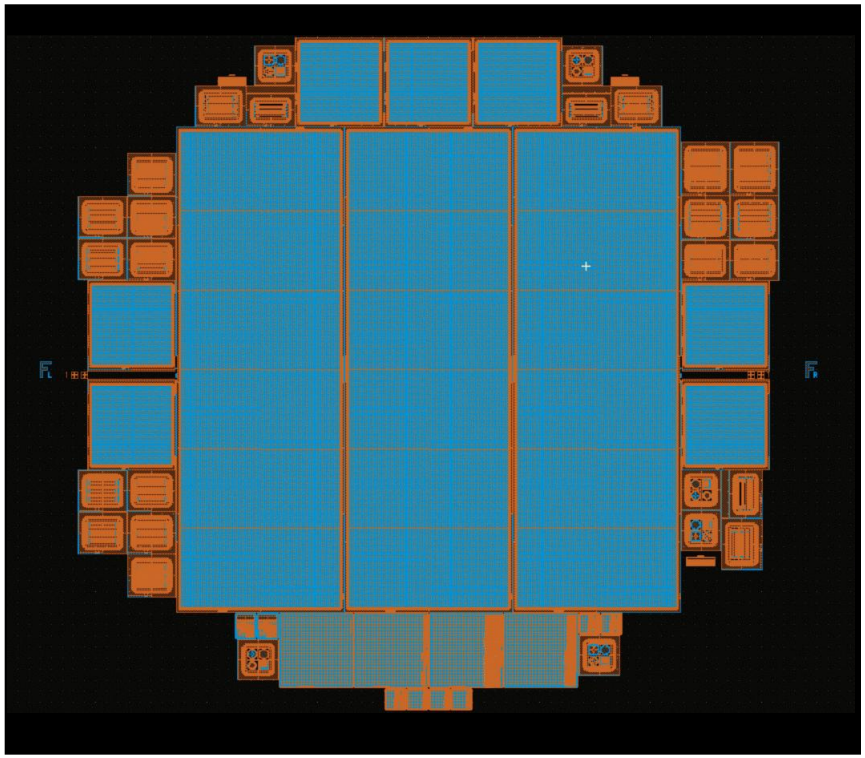
Large-area silicon modules

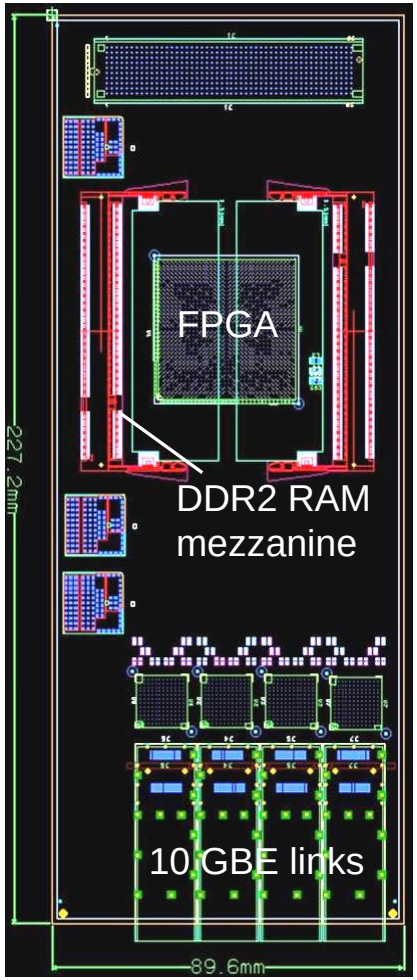
- 6” wafers with large Medipix3-layout sensors ordered from Canberra
  - Masks in production
- Working on assembly process and single module mechanics



High-speed readout system

- Will modify board and firmware from XFEL
  - Collaborating with TUM on firmware
  - See Franz M. Epple's poster
- Virtex-5 FPGA with PowerPC core
- RAM for data re-ordering and burst mode
- 4 * 10 Gbit Ethernet to allow maximum readout rate
  - Maximum data rate from module is ~ 25 Gbit/s!

High-density connector



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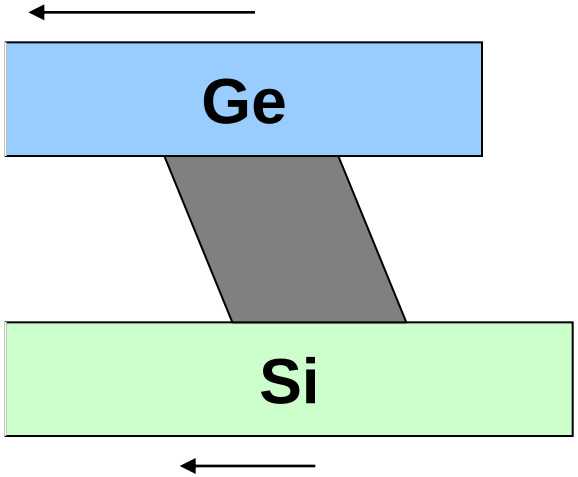
Germanium pixel development

Canberra (Lingolsheim): M Lampert, M Zuvic, J Beau

Fraunhofer IZM (Berlin): T Fritzsch, R Jordan, H Oppermann, O Ehrmann

- High-purity, high uniformity 90 mm Ge wafers available
- Cooled operation needed to reduce leakage current
  - *Per pixel* current must be within ROC limits (order of nA per pixel)
  - Est. **-60°C** operation with Medipix3 (55µm)
    - Measured transport and depletion fine at this temperature
  - Thermal stresses are biggest problem
- Fine pixellation and bump-bonding must be developed

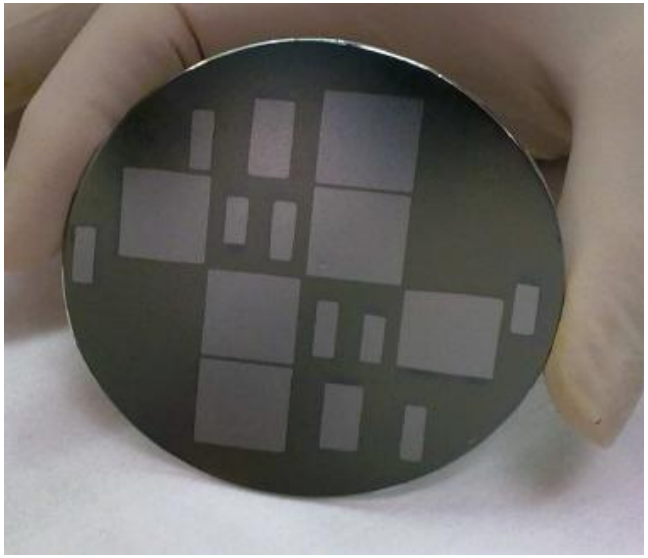
Bump bonding and sensor processing

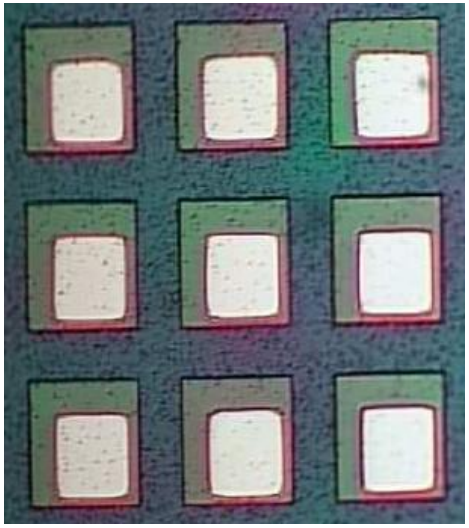


- ~3.5µm max displacement during cooling
- Indium bump bonding
  - Indium remains ductile at low temperatures
  - Already used for IR hybrids at −196 °C
- Ge diodes used for processing tests
  - Passivation and processing optimised to avoid sensor damage
  - Bumps will be electroplated on sensor and ROC
  - Bonding will use thermocompression at 80°C

Pixel detector production at Canberra

- Detector structure:
  - Thinned germanium wafer (700µm)
  - Boron implanted on back contact
  - New pixel architecture
- Test wafer produced (55µm pixels)
- Medipix3 90 mm mask produced
  - 16 singles per wafer
- Optical Ge dummies in production
  - Optimization of flip chip at IZM
- 2 high-purity wafers will be produced
  - Expect sensors later this year





Summary

- Goal is to provide improved hybrid pixel detectors for PETRA-III
- Prototype Medipix3 module is complete
- Continuing to produce full Si sensors and high-speed readout
- Developing pixellated Ge sensors for high-energy beamlines

> Thanks for listening