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# The Belle II pixel vertex detector

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Super-KEKB, an upgrade of KEKB is under construction, to increase the luminosity by two orders of magnitude during a three-year shutdown, with an ultimate goal of 8x10<sup>35</sup>cm<sup>-2</sup>s<sup>-1</sup> luminosity. To exploit the increased luminosity, an upgrade of the Belle detector has been proposed. The physical goals of the planned Belle II experiment require a vertex detector with unprecedented performance. The main issues are a high spatial resolution of a few micrometers, a high granularity, and a fast readout speed to cope with the expected high hit occupancy.

A new vertex detector (PXD) based on DEPFET technology is being developed, using sensors thinned down to 75um. In the DEPFET pixel concept, the first amplifying transistor is integrated into a high resistivity silicon substrate. By sidewards depletion and an additional n-implantation below the FET, a potential minimum for electrons is created right underneath the transistor channel, which can be considered as an internal gate of the FET.
The signal electrons created by an impinging particle are collected and stored in the internal gate, which results in a modulation of the transistor current.

The operation mode is the continuous row wise readout (rolling shutter), with four rows read in parallel on each side reaching a readout time of 20 us for a whole frame. The row control is provided by the steering chips (called Switchers) placed in the lateral balcony, while the analog front-end (DCD or Drain Current Digitizer) and the processors (DHP or Data Handling Processor) are on the ends of the stave, on both sides of the ladder. All ASICs will be directly bump-bonded on to the ladder with a dedicated machinery. PXD consists of two layers, at radius of 14mm and 22mm, respectively. The inner layer uses 8, the outer layer 12 individual detector modules.
The talk will cover the current status of the PXD system
and overview of recent results on system performance.

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