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A Multi-Mode Hybrid Pixel Detector ASIC for Dosimetry and General Radiation Detection

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Present-day dosimeters based on single diode implementations typically require strict presumptions regarding the radiation type and energy, have limited dynamic range, and tend to provide non-linear responses to energies within the ranges typical to occupational radiation environments. Moreover, the ability of the detector to resolve low energy photons is limited by the noise of the electronics. Hybrid pixel detectors provide a potential solution to these limitations. By segmenting the active area into many small channels, the probability of multiple radiation events simultaneously impinging on a single channel is greatly reduced, thereby allowing the front-end electronics to complete the processing of a single event before the arrival of the next event. Consequently, because the detector can process and provide energy information on discrete events, the linearity of the detector's response is very high. As the electronics noise is a function of the input capacitance from the detector, the segmentation also lowers the detector's noise-floor, thereby allowing a clean detection of low energy photons.

In this work, we present a hybrid pixel detector ASIC with three programmable modes of operation: dosimetry mode, single photon counting mode, and energy integration mode. The ASIC comprises a matrix of 16 by 16 (256 total) square pixels of 220 μm pitch, providing 12.4 mm2 of segmented active area. Each pixel can be configured to operate in one of the three measurement modes, with programmable-depth counters and shift registers to tailor the data word size and optimise the readout frame-rate in a given mode. The individual energies of impinging photons are determined through programmable analogue energy threshold discrimination, time-over-threshold measurement, or a combination thereof. Furthermore, the dosimetry mode contains 16 digital energy thresholds and automatically sorts data into 16 corresponding energy bin registers. The emphasis of this paper will be on the implementation of the shared electronics which enable the three modes within the same pixel area. A discussion on the initial electrical measurements of the prototype ASIC will also be presented.

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