Integrated USB based readout interface for silicon strip detectors of the ATLAS SCT module

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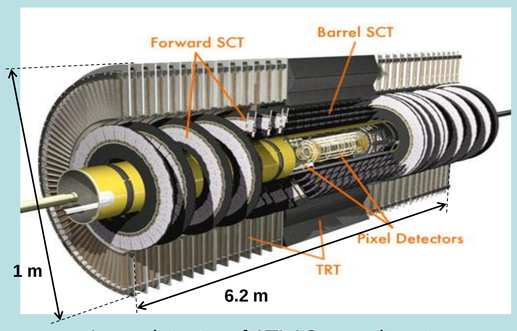
INTRODUCTION

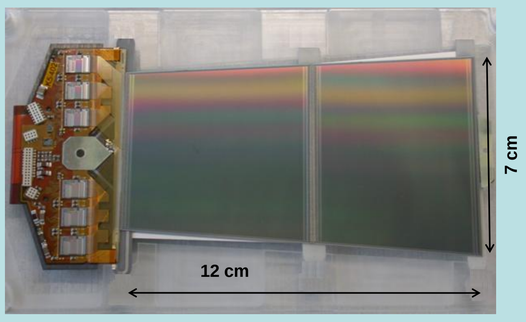
The ATLAS SCT modules are large area silicon strip detectors designed for tracking of high-energy charged particles resulting in collisions in the Large Hadron Collider (LHC) at CERN. These modules can be also used on small accelerators for medical or industry applications for which tasks an integrated and compact readout interface would be practical. Such new interface has been designed and constructed providing integrated power, control and DAQ with online and easily configurable communication between the detector module and the controlling PC.

SCT MODULE

- 2 silicon 300 µm plates divided into 768 strips
- Strips rotated about 2.3 degrees
- Spatial resolution 70 µm in one direction
- 6 ABCD3T chips per plate, binary readout
- Accumulation register for longer exposition
- Huffman-like compression readout circuitry
- DACs for remote adjusting parameters
- Readout buffer for data from 8 triggers
- Amplifier & shaper (25 ns) & comparator for each channel (the result can be logic 1-hit or 0-no hit)
- Comparator output sampled on each rising edge of 40 MHz clock
- Sampled logic value stored in FIFO or sifted through accumulator
- 132bit long FIFO allows 3.3 µm latency compensation @ 40 MHz



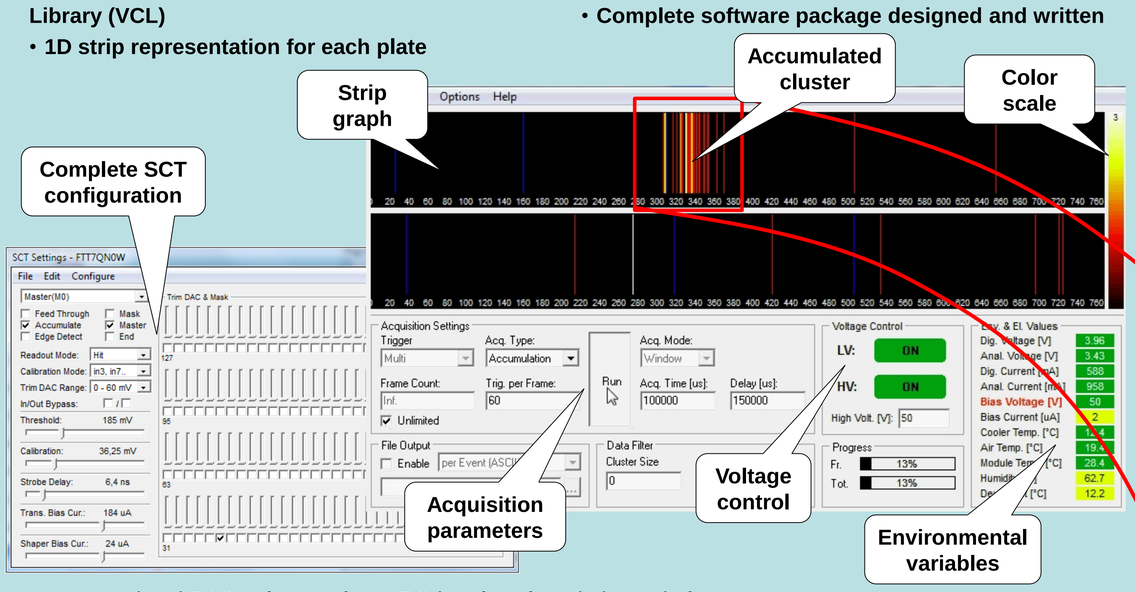
Inner detector of ATLAS experiment



ATLAS SCT type strip module

ONLINE VISUALIZATION AND CONFIGURATION

- C++ multithread application
- Windows compatible
- Low level communication through DLL driver library
- Strips decoded after event packet acceptation
- High level GUI based on Visual Component Library (VCL)
- 1D strip representation for each plate
- Well arranged, complete and easy to change SCT module configuration
- Setting several acquisition parameters
- Online control and status monitoring
- Generates output file with description header, compression available to reduce space
- Complete software package designed and written



Control and DAQ software of new RO interface for Windows platform

TEST WITH β SOURCE

- ^{90}Sr source placed above silicon plate
- Plastic scintillator situated under the silicon detector, external conversion needed, CMOS 3.3 V standard supported only
- Tracking mode selected, external trigger chosen

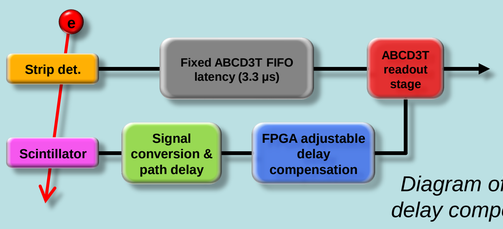
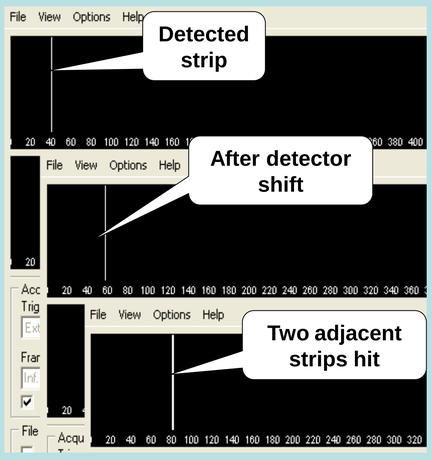


Diagram of trigger delay compensation



Response of three events at different times

READOUT INTERFACE: POWER, CONTROL, DAQ

FPGA

- Spartan 3E family assembled
- Massive parallel structure, huge logic capacity, PCB simplified
- Working frequency 40 MHz
- Hierarchical design described in VHDL, FSM based
- Low-level communication with ABCD3T implemented
- Command protocol stored in internal ROM
- Data protocol parsed and parallelized real-time
- Internal RAM used as fast data buffer
- Acquisition control with time resolution of 25 ns
- External trigger processing, latency compensation

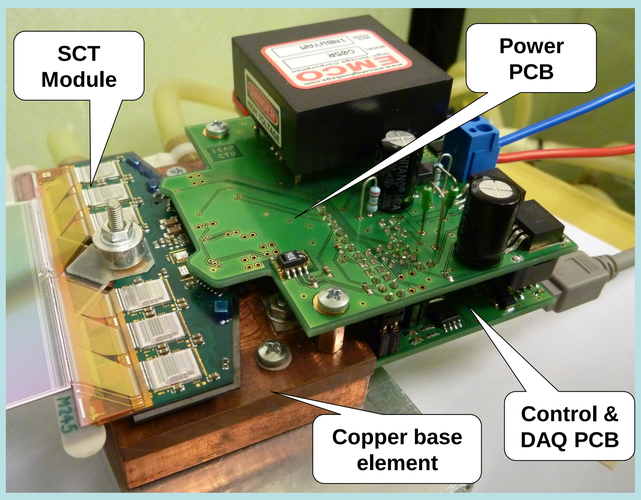
FPGA xc3s250e-4tq144 utilization			
Logic	Available	Used	Utilization
Number of Slice Flip Flops	4,896	762	15%
Number of 4 input LUTs	4,896	1,916	39%
Number of occupied Slices	2,448	1,153	47%
Total Number of 4 input LUTs	4,896	2,022	41%
Number of bonded IOBs	108	87	80%
Number of RAMB16s	12	2	16%
Number of BUFGMUXs	24	2	8%

USB INTERFACE

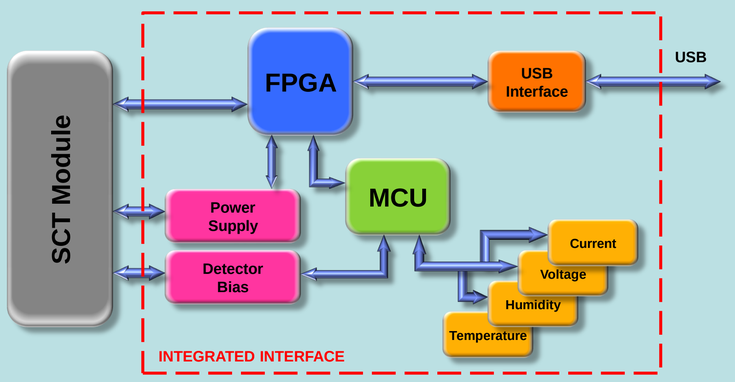
- Controller FT2232H used
- Royalty free drivers supported by producer
- Power supply for interface electronics
- Theoretical throughput 12.5 MB/s (fifo mode)

MICROCONTROLER

- 8bit RISC architecture, 10 MIPS @ 40 MHz
- Communication with environment sensors & values ADC conversion
- Bias voltage adjusted & controlled by feedback measurement (range 50 – 500 V)
- User sub-firmware decoder implemented – complex routine can be run independently of operator



Assembled prototype of integrated readout interface



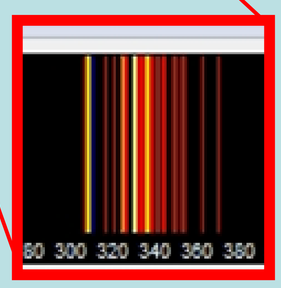
Block scheme of interface architecture

ASSEMBLY & COOLING

- Two tightly connected boards create compact unit
- Switching power supply separated from signal circuits
- Everything mounted on copper base element for better manipulation
- Conventional liquid coolant apparatus or Peltier element can be attached
- External 12 V power source needed

TEST WITH α SOURCE

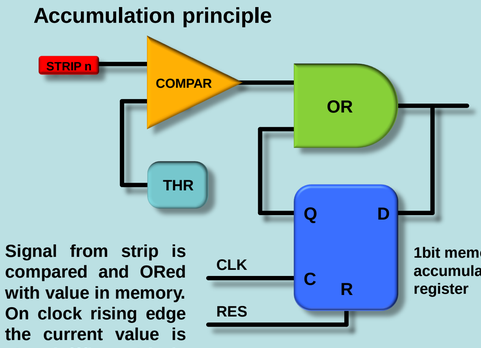
- Collimated ^{241}Am (106 Bq) source 1 cm above silicon plate used
- Accumulation mode in ABCD3T chips enabled
- Sequence of 60 L1 trigger commands generated
- Detected strips after each L1 trigger summed in user software
- Exposition time 100 ms, 6 expositions per second



Detailed visualization of about 100 strips

- Detected strips are represented in color scale
- When allowed, data are stored in file

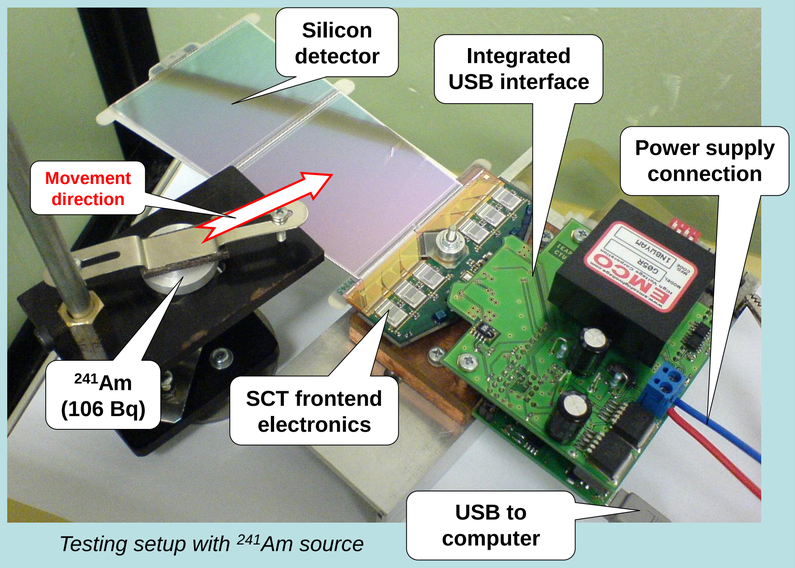
Accumulation principle



Signal from strip is compared and ORed with value in memory. On clock rising edge the current value is stored. When strip is hit logic 1 remain stored until reset.

1bit memory in accumulation register

Schematic diagram of accumulation principle



Testing setup with ^{241}Am source

ACKNOWLEDGEMENTS

This work has been supported by the Ministry of Education, Youth and Sports of the Czech Republic under the Research Projects MSM 6840770029 "Fundamental Experiments in the Physics of the Microworld" and LA 08032 "International Experiment ATLAS-CERN".

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C. Lacasta (2003), *Design optimization of silicon microstrip detector modules for operation in high radiation levels at the LHC*. NIM A. 157-166.
P. Masek (2010), *Hardware Interface and Software Readout for Detection of Heavy Charged Particles in Silicon Strip Detectors*. Master thesis. CTU in Prague, Czech Republic.

CONCLUSIONS

- New integrated USB interface was designed including power, control and DAQ
- The first prototype constructed
- Complete software package written and provided
- Logic function for programmable devices successfully tested
- System provides detector configuration and measurement settings adjustment
- Prototype demonstrated and successfully tested with real sources

FUTURE WORK

- Complete system commissioning
- Module settings optimization
- Calibration with defined sources
- Response characterization of neutrons
- Calculation of 2D imaging
- Physics experiments with MIPs energetic particles

International Workshop on Radiation Imaging Detectors
3-7 July 2011, ETH Zurich (Switzerland)