Monolithic Radiation Image Detectors with SOI technology

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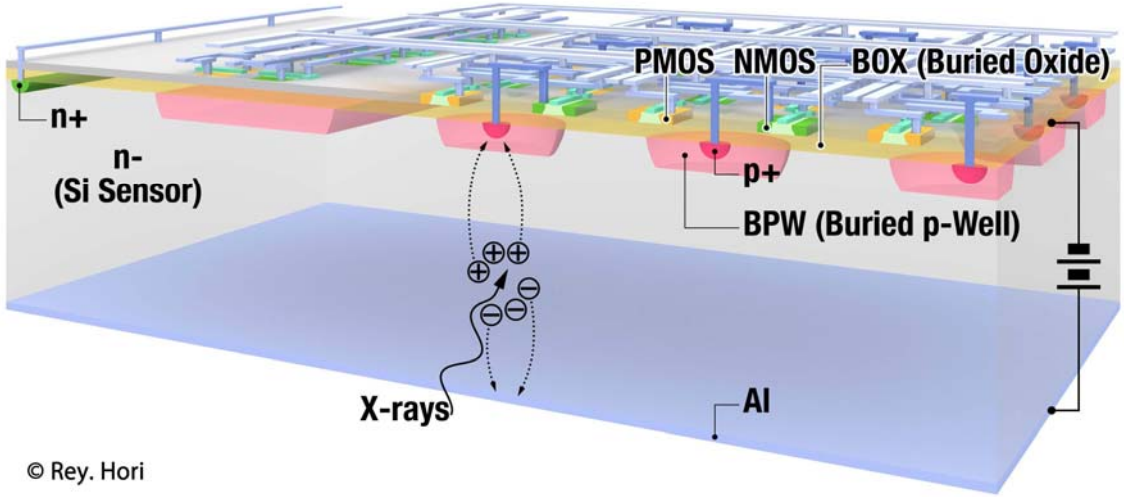
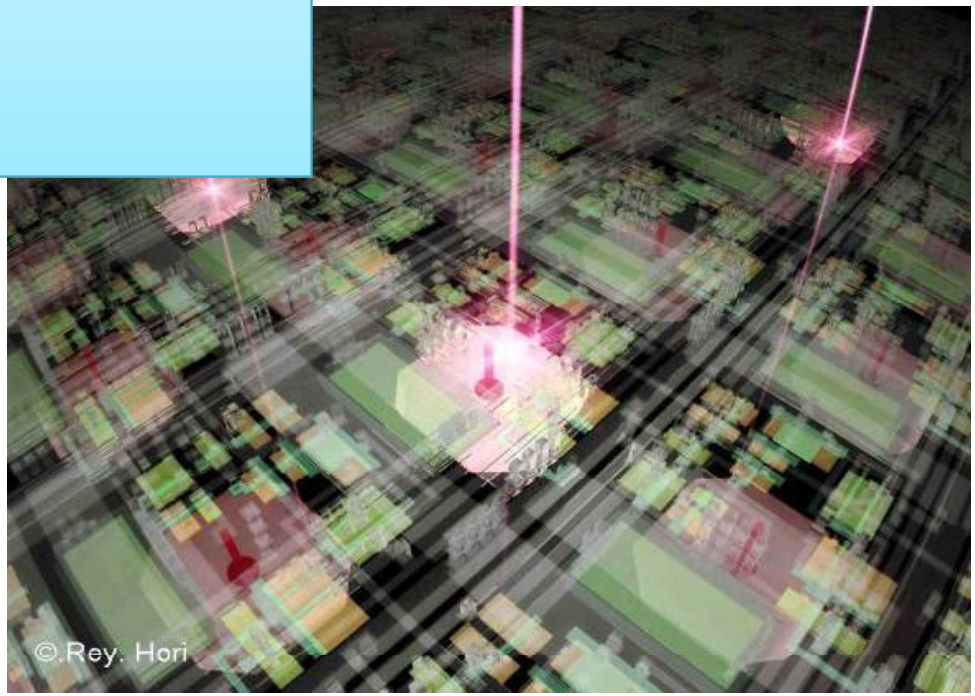
http://rd.kek.jp/project/soi/

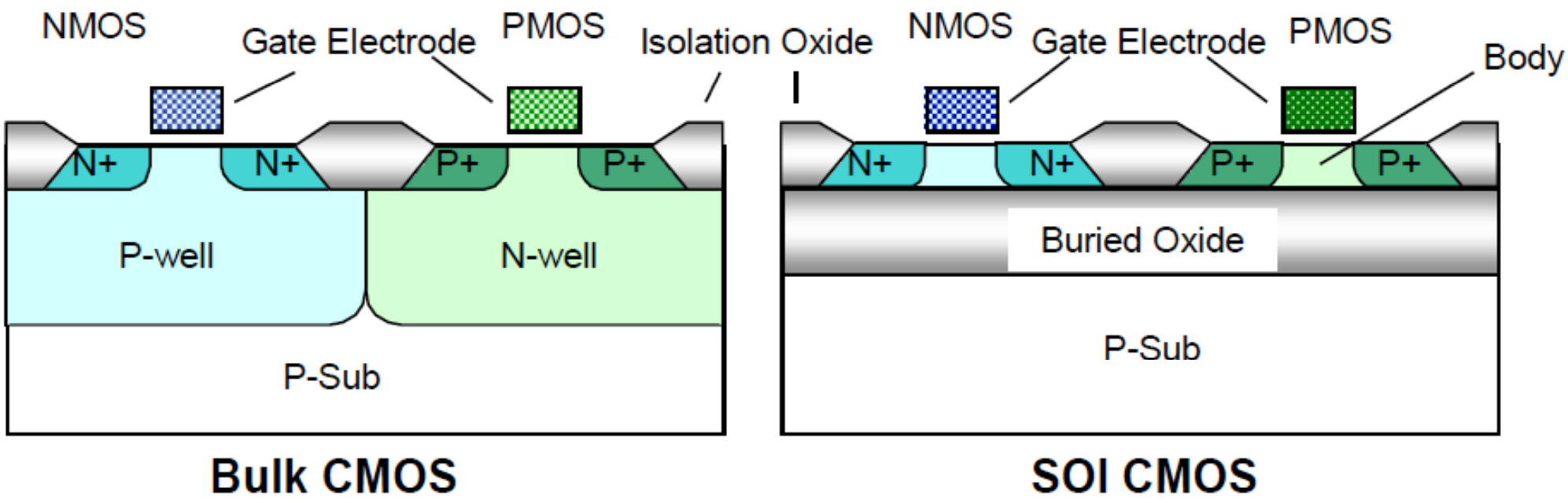


OUTLINE

- Introduction
- Developed Techniques
- Test Results of SOI Detectors
- Summary



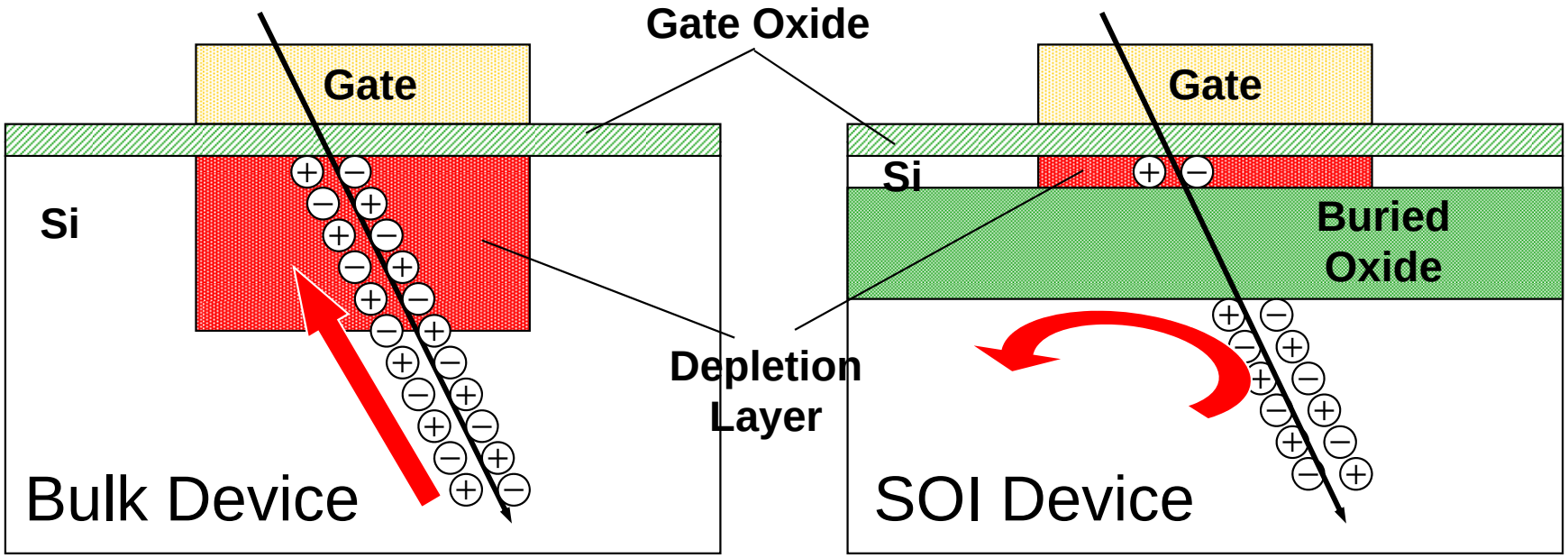
Bulk CMOS vs. SOI CMOS



In SOI, Each Device is completely isolated by Oxide.

- Low Parasitic Capacitance. Low Power & High Speed.
- No Latch Up. Good Isolation between circuit.
- Operate in wide temperature range (4K-570K(300˚C)).

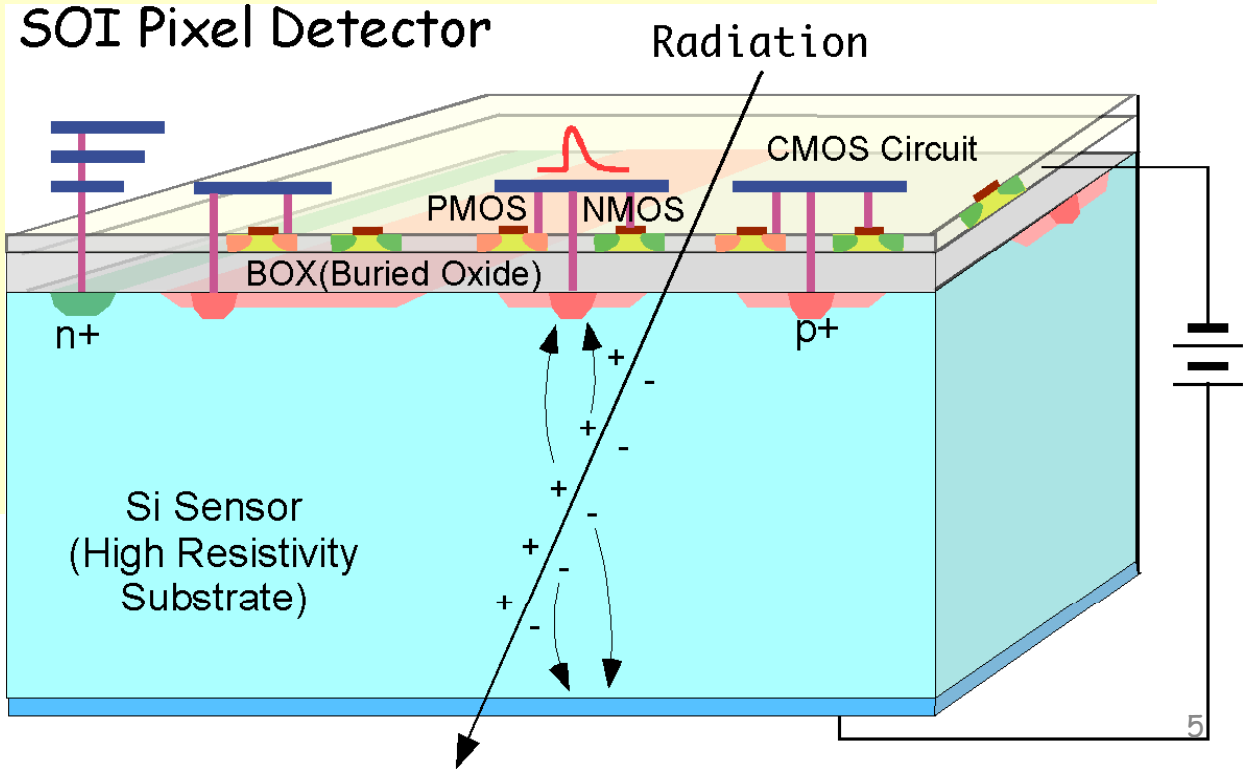
SOI is Immune to Single Event Effect



Thus, the SOI devices are often used for satellite.

Features of the SOI Pixel Detector

- Bonded wafer : High Resistivity (Sensor) + Low R (CMOS) .
- Truly Monolithic Detector (-> High Density, Low material).
- Standard CMOS circuit can be implemented.
- No mechanical bump bonding (-> High yield, Low cost).
- Small capacitance of the sense node (~10fF)
- Based on Industrial standard technology (-> Cost benefit and Scalability)
- ...

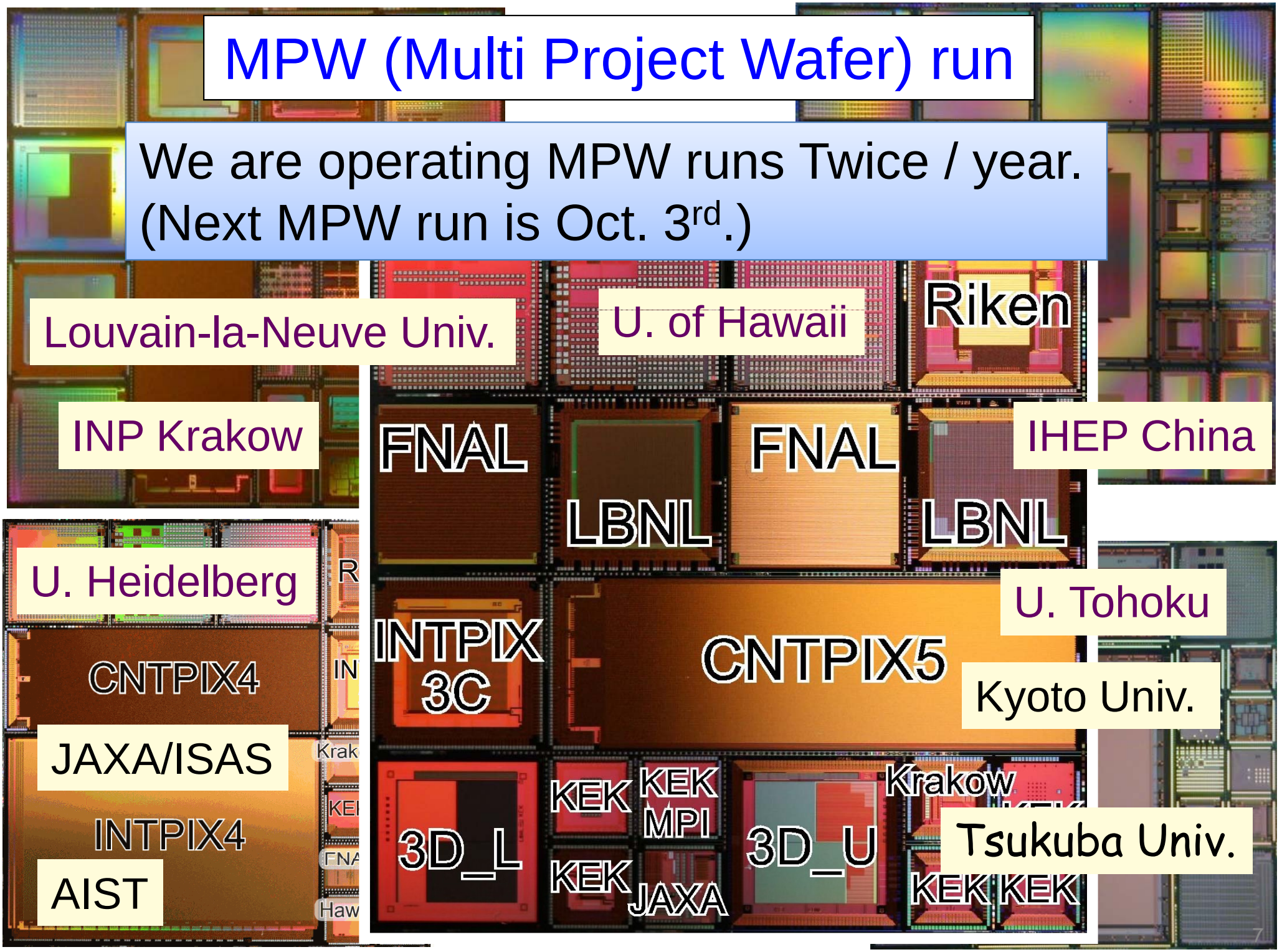


OKI semi 0.2 μm FD-SOI Pixel Process

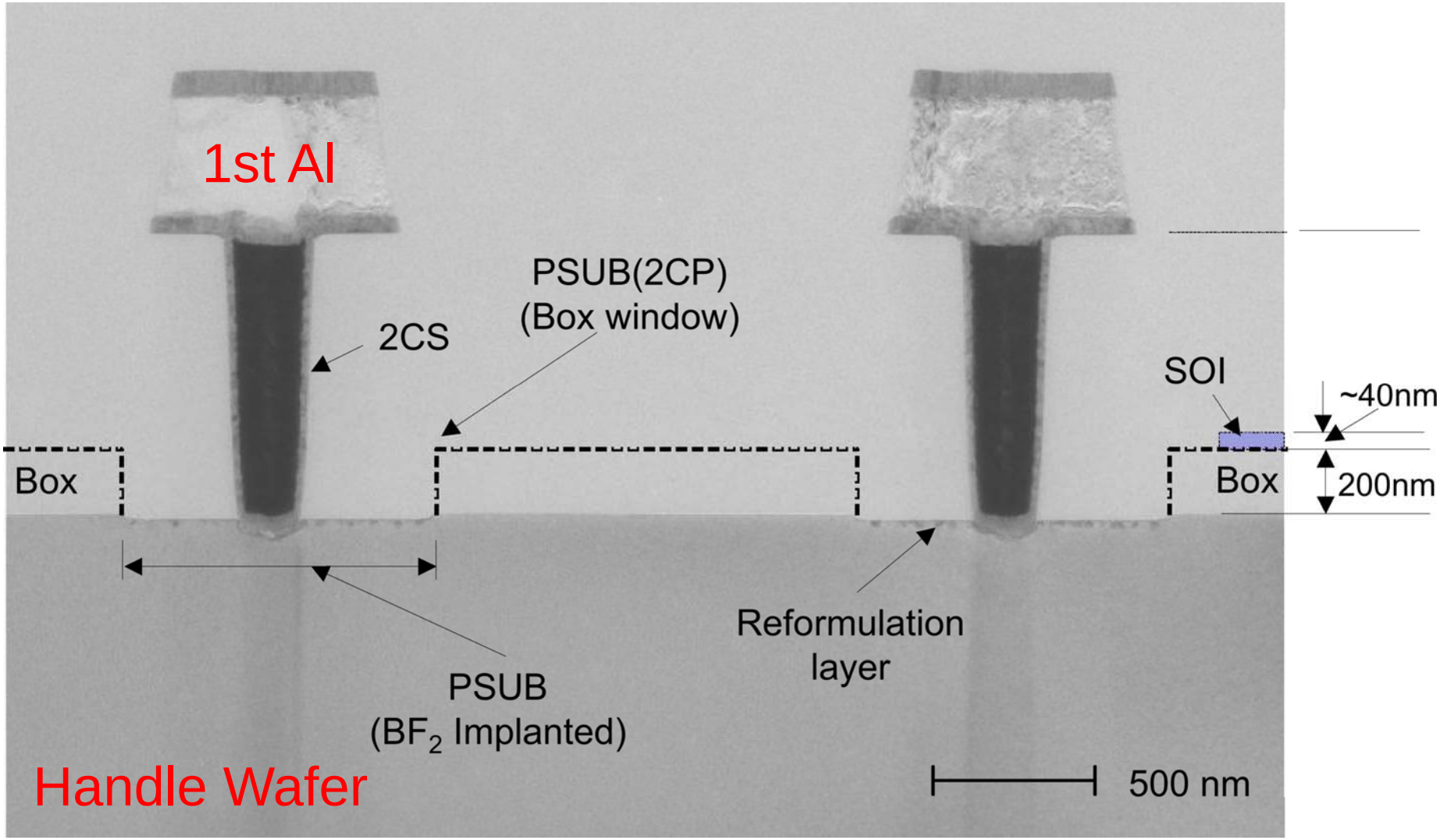
Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) ~7k Ω-cm, FZ(p) ~40 k Ω-cm
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

MPW (Multi Project Wafer) run

We are operating MPW runs Twice / year.
(Next MPW run is Oct. 3rd.)

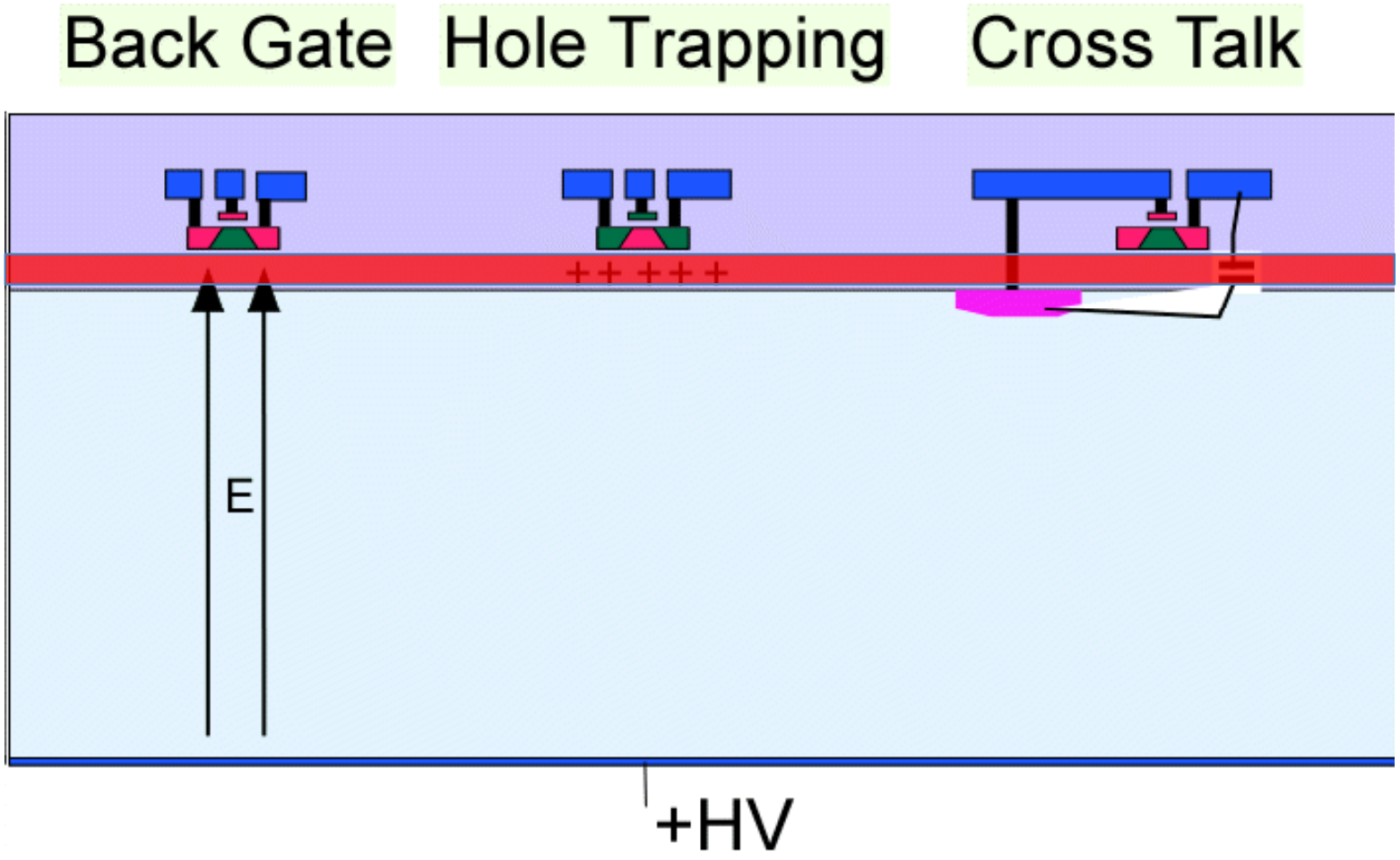


Developed Techniques



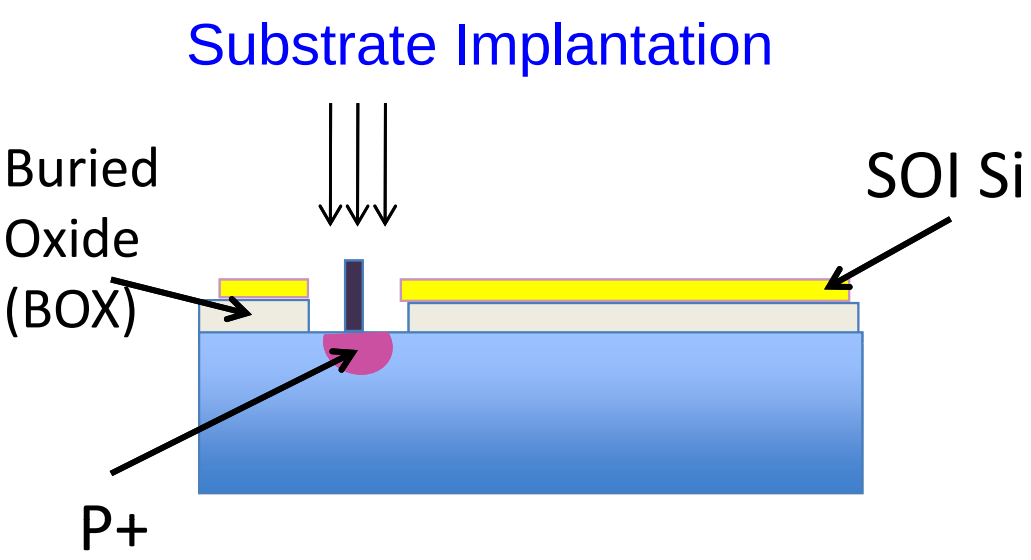
Isuues in SOI Pixel

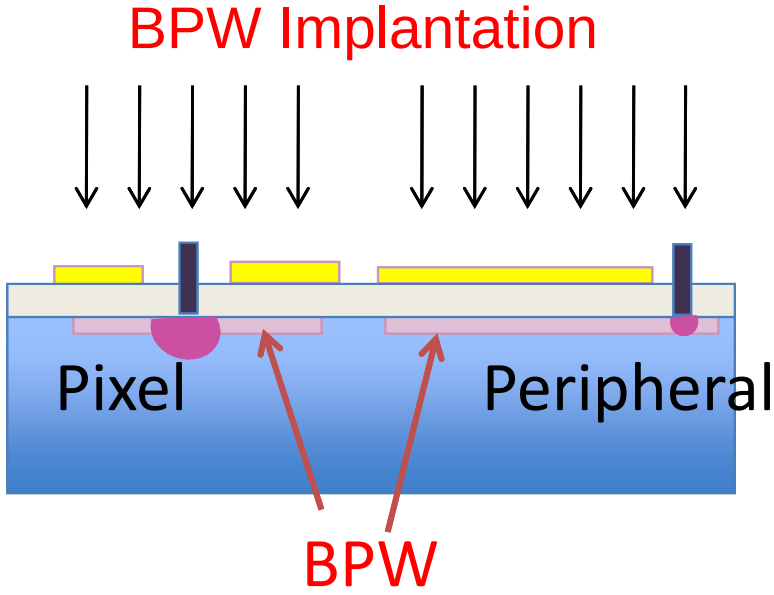
Sensor and Electronics are located very near. This cause ..



We need another electrode under the transistors.

Buried p-Well (BPW)





- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

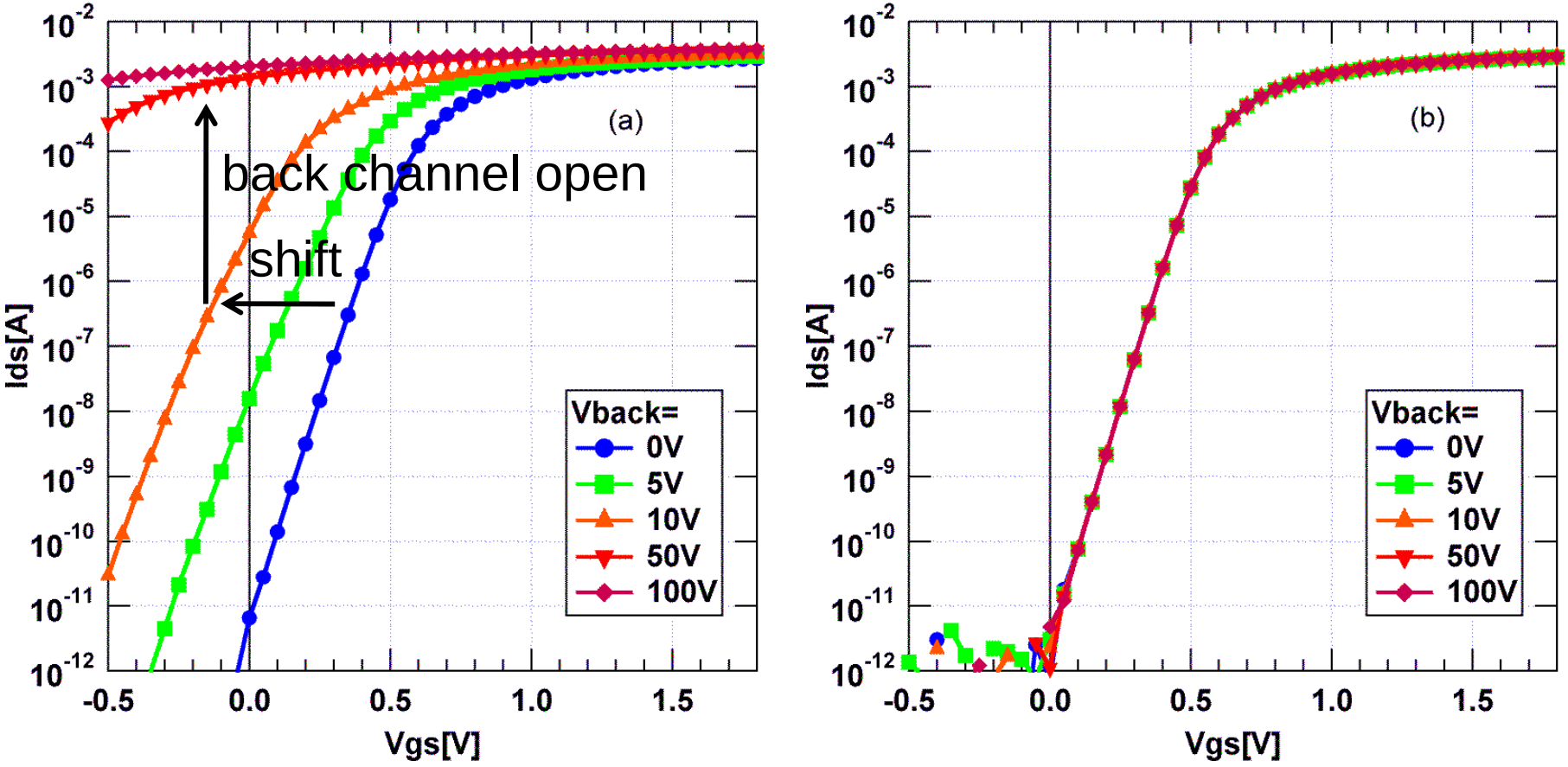
- Suppress the Back Gate Effect.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Less electric field in the BOX which improve radiation hardness.

I_d-V_g and BPW

w/o BPW

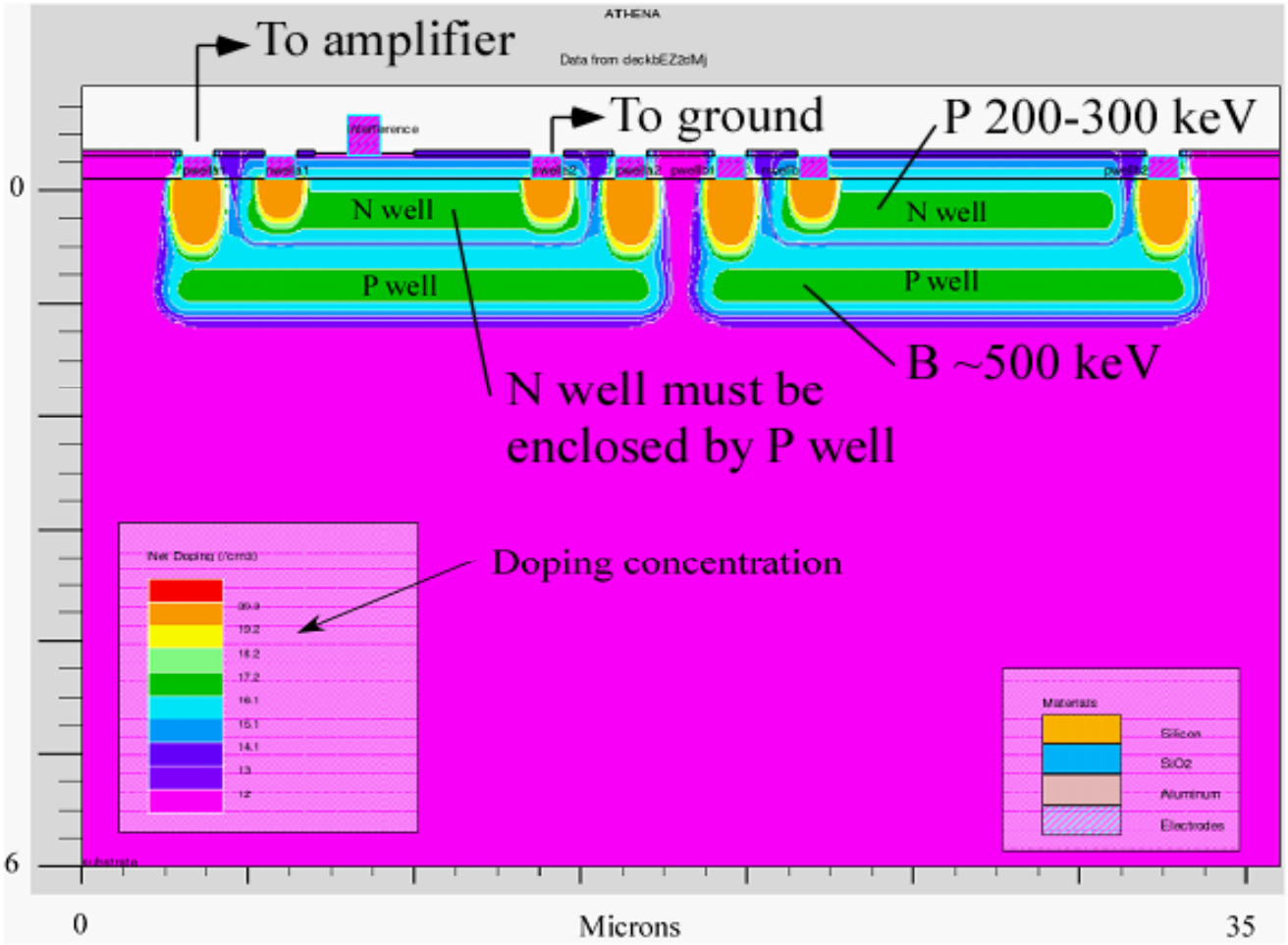
with BPW=0V

NMOS



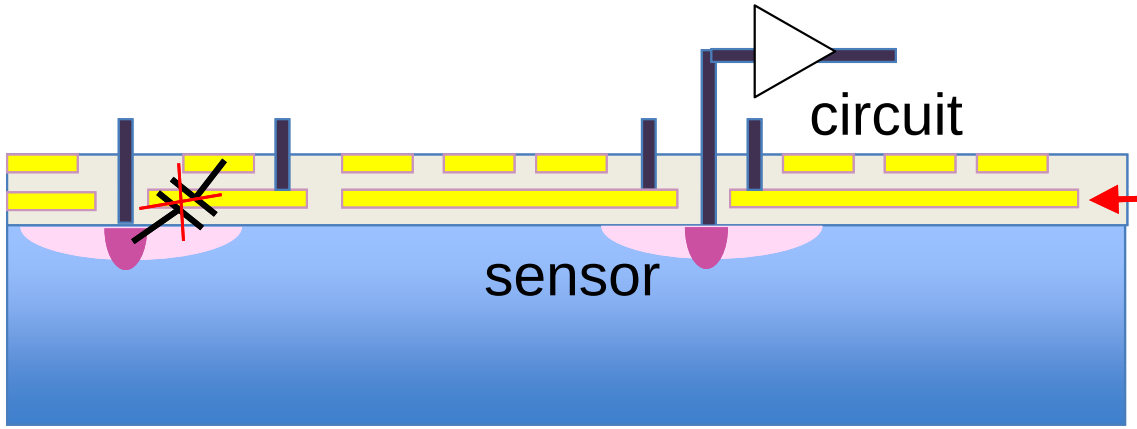
Back gate effect is suppressed by the BPW.

Nested BNW/BPW Structure



- Signal is collected with the deep Buried P-well.
- Back gate and Cross Talk are shielded with the Buried N-well.

Double SOI Layer wafer



additional conduction layer

Shield sensors from circuit

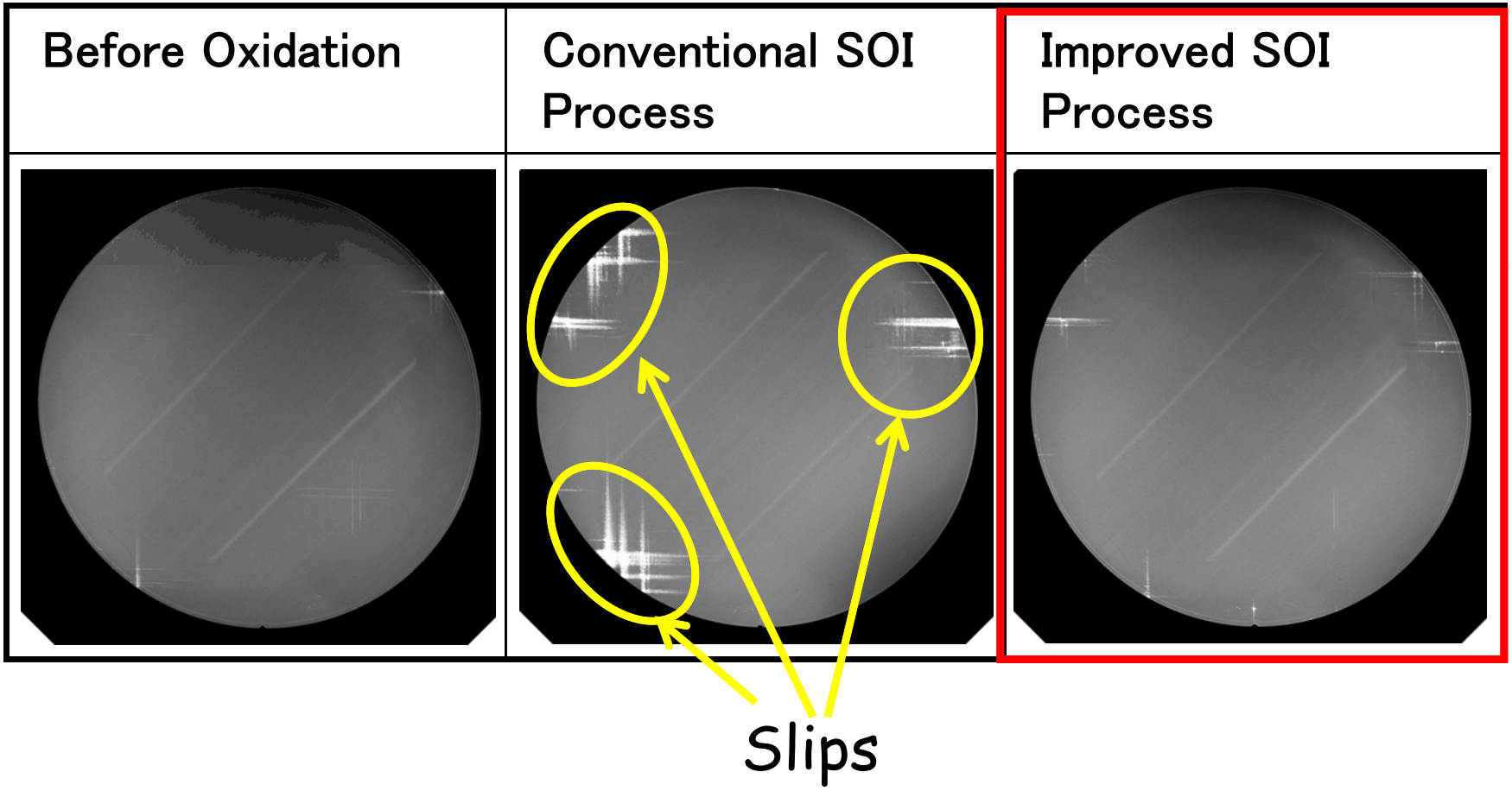
In addition to the shielding between sensor and electronics,

* oxide trapped hole can be compensated
* able to control Tr threshold voltage block by block
* additional components such as diode, resistors can be implemented.

Wafer is ready.
Process study is in progress.

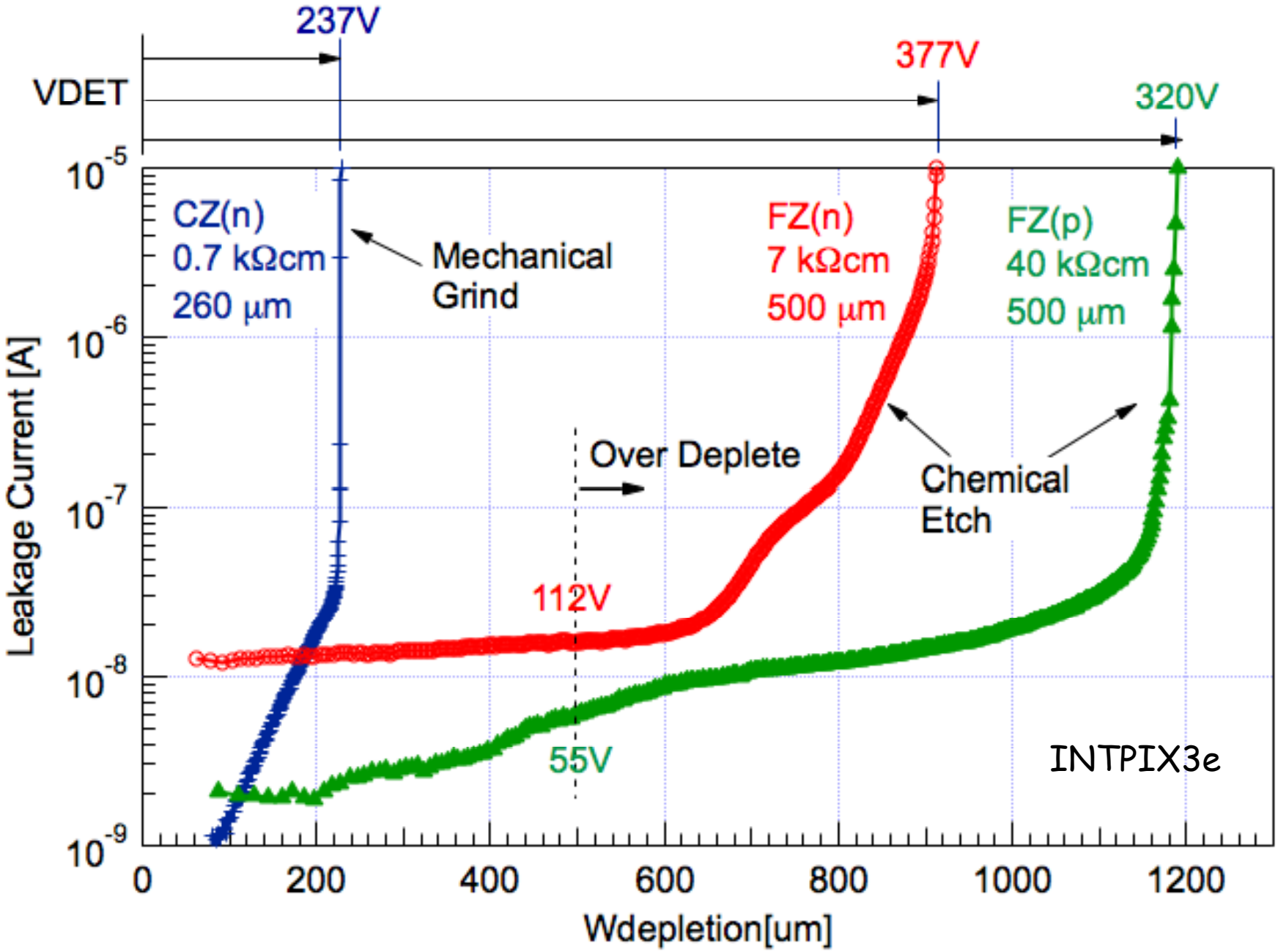
FZ(p and n) SOI Wafer

It was difficult to process 8” FZ-SOI wafer in CMOS process.



We optimized the process parameters, and succeeded to perform the process without creating many slips.

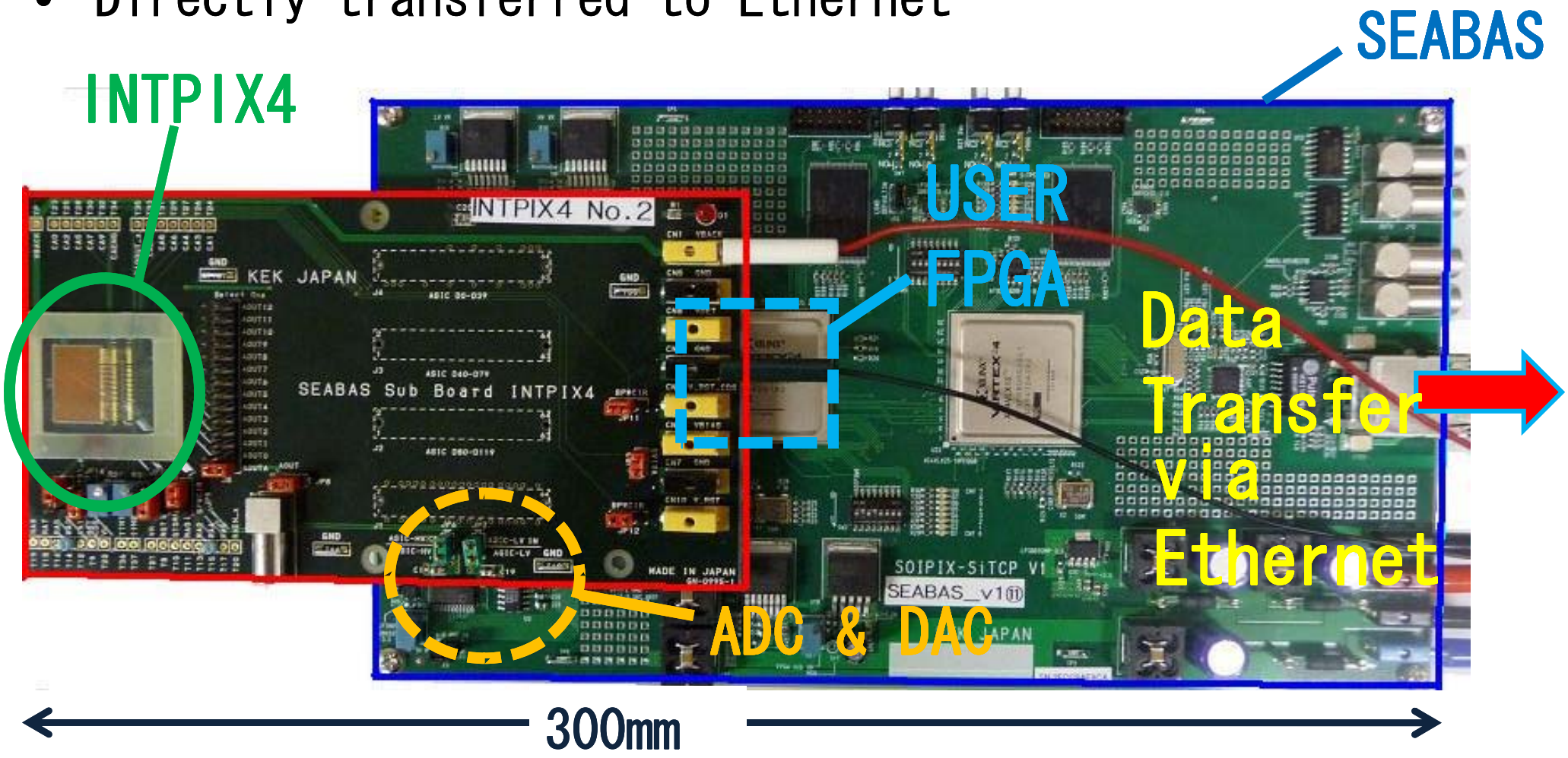
Wafer type and Leakage Current



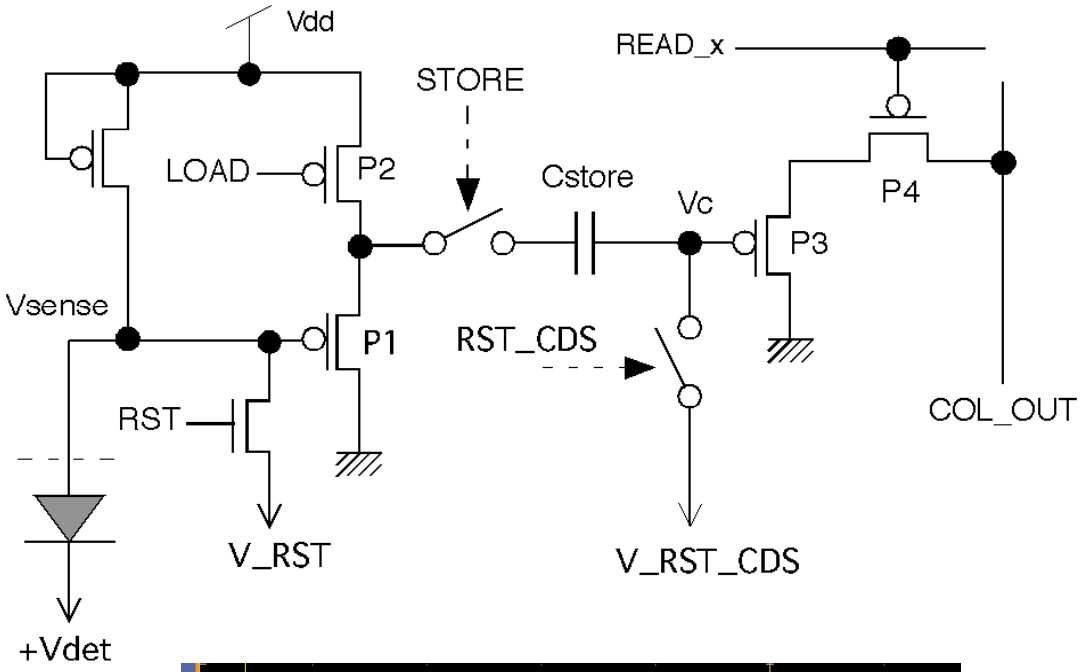
SOI Detectors

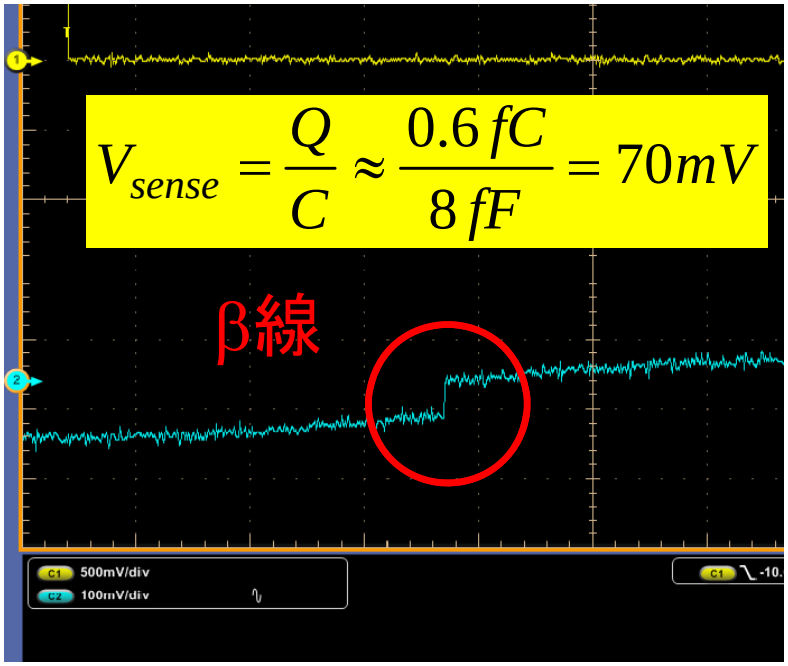
Data Acquisition Board

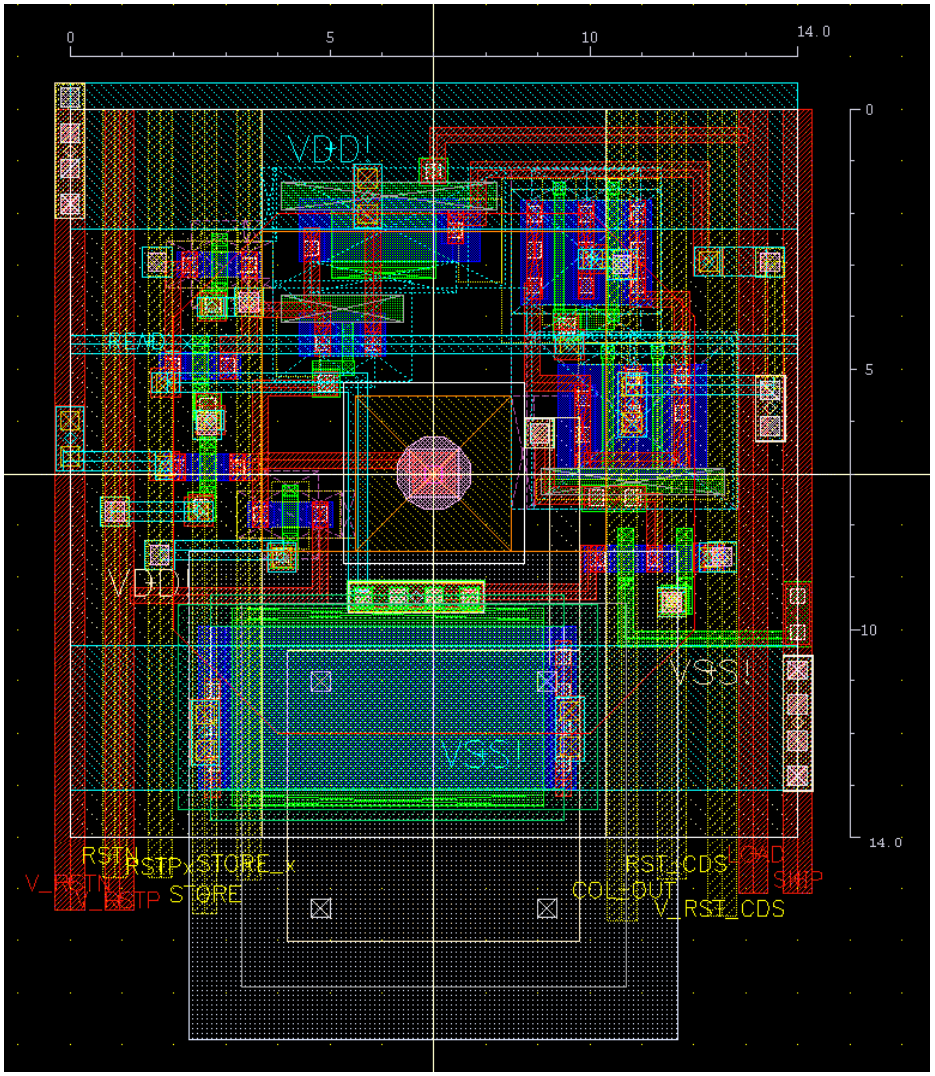
- Soi EvAluation BoArd with Sitcp(SEABAS)
- A FPGA controls the SOI Pixel chip
- Directly transferred to Ethernet



Integration Type Pixel (INTPIX)



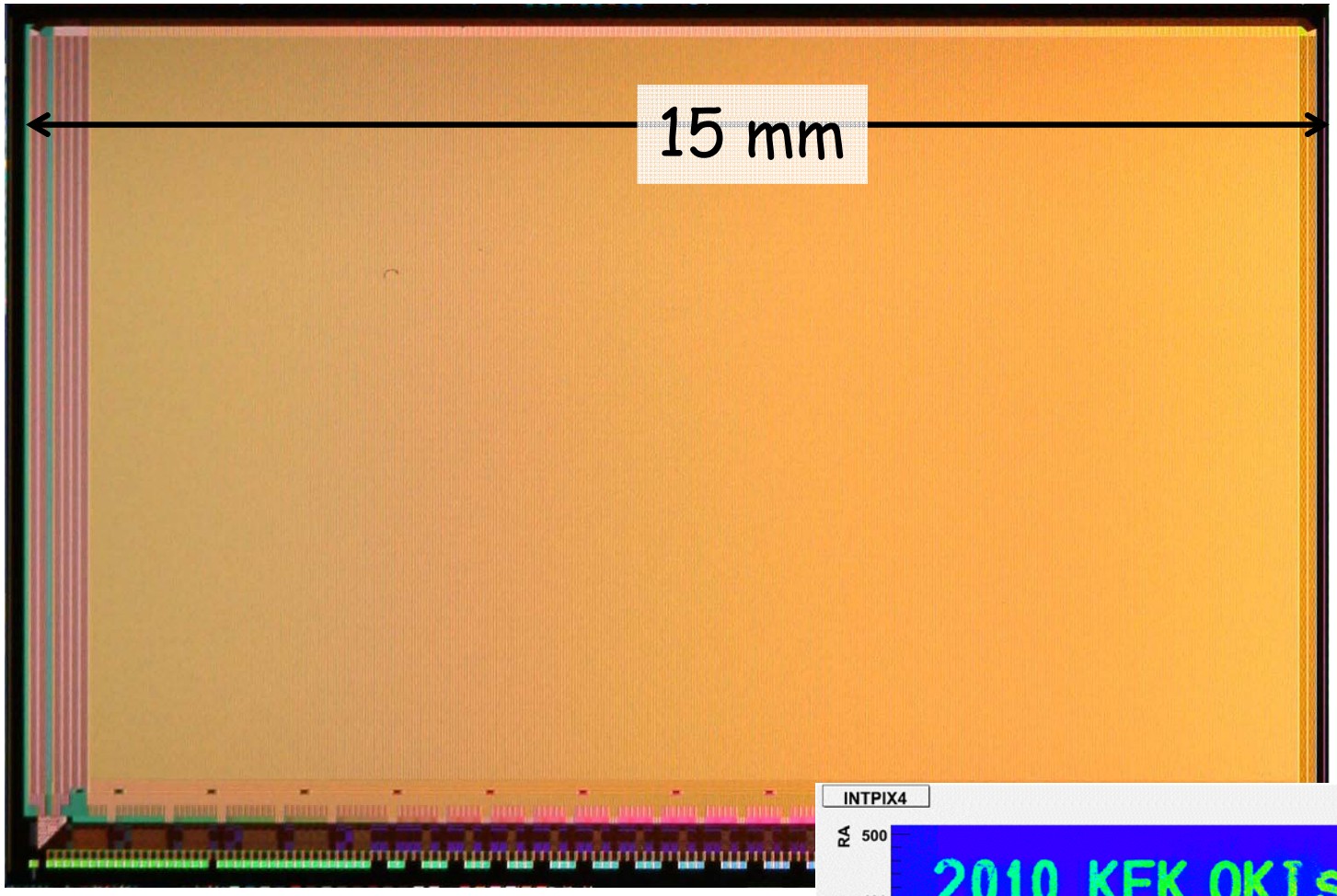


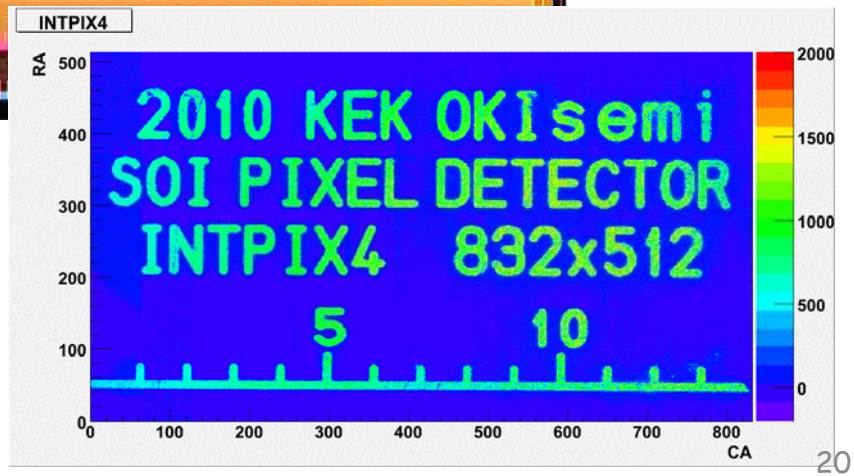


Size : 14 μm x 14 μm with CDS circuit

Integration Type Pixel (INTPIX4)

Largest Chip so far.

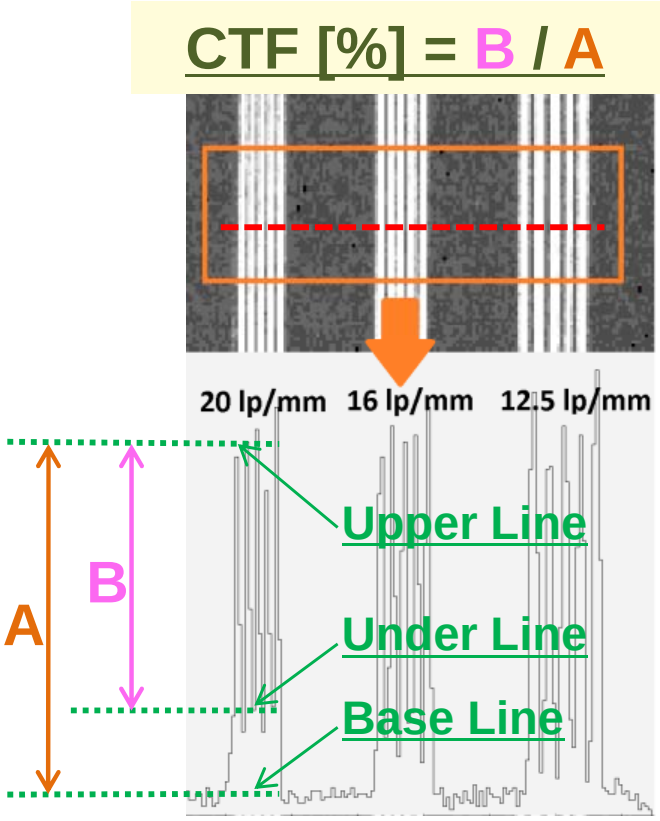


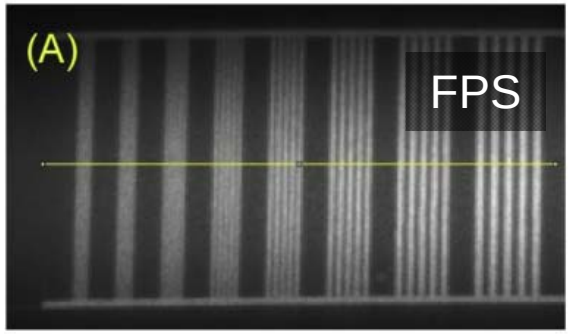


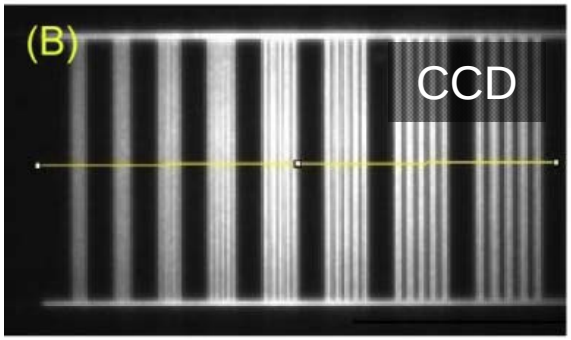
17x17 μm, 512x832 (~430k) pixels、13 Analog Out、CDS circuit in each pixel.

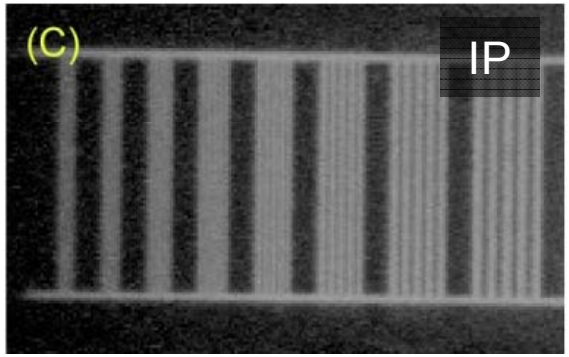
Spatial Resolution (Contrast Transfer Function)

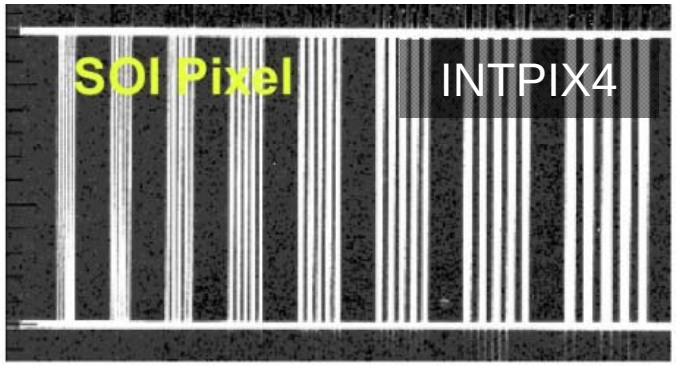
- Comparison of contrasts with commercial X-ray devices.
  - SOI Pixel : INTPIX4, **F**lat **P**anel **S**ensor (FPS), CCD, and **I**maging **P**late (IP)

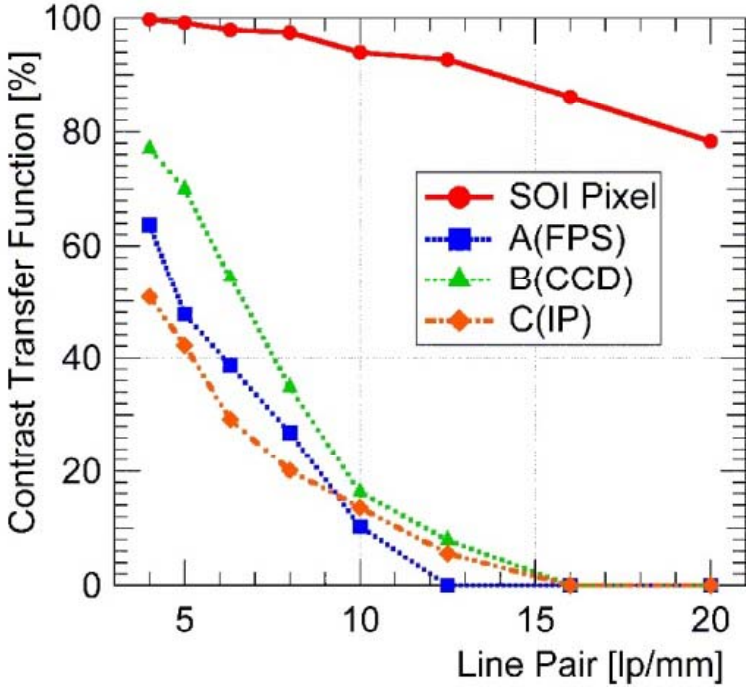


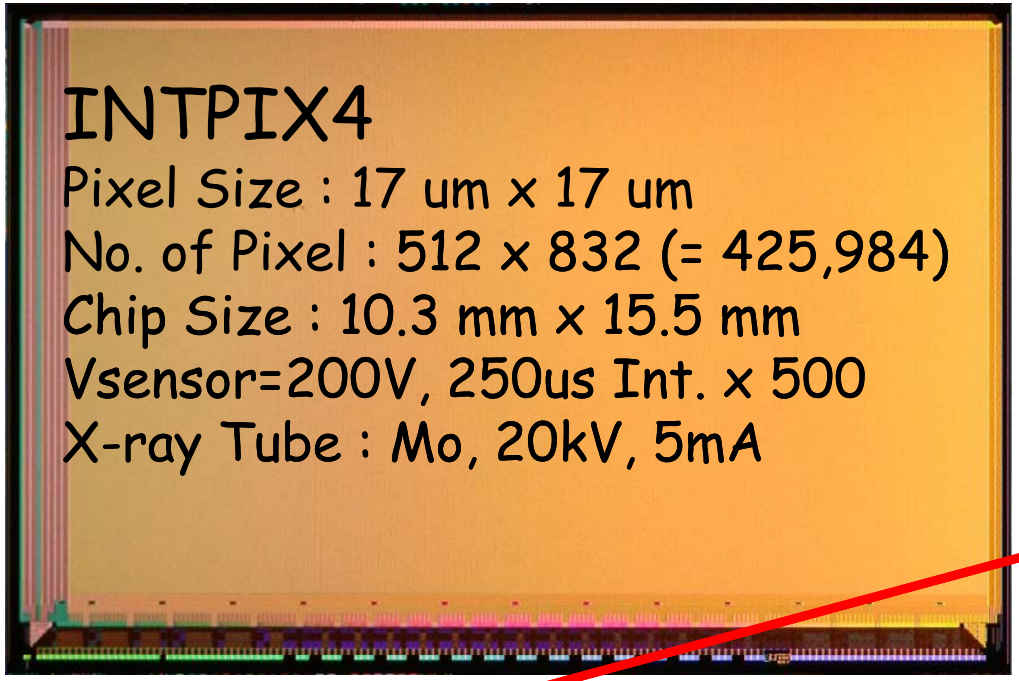




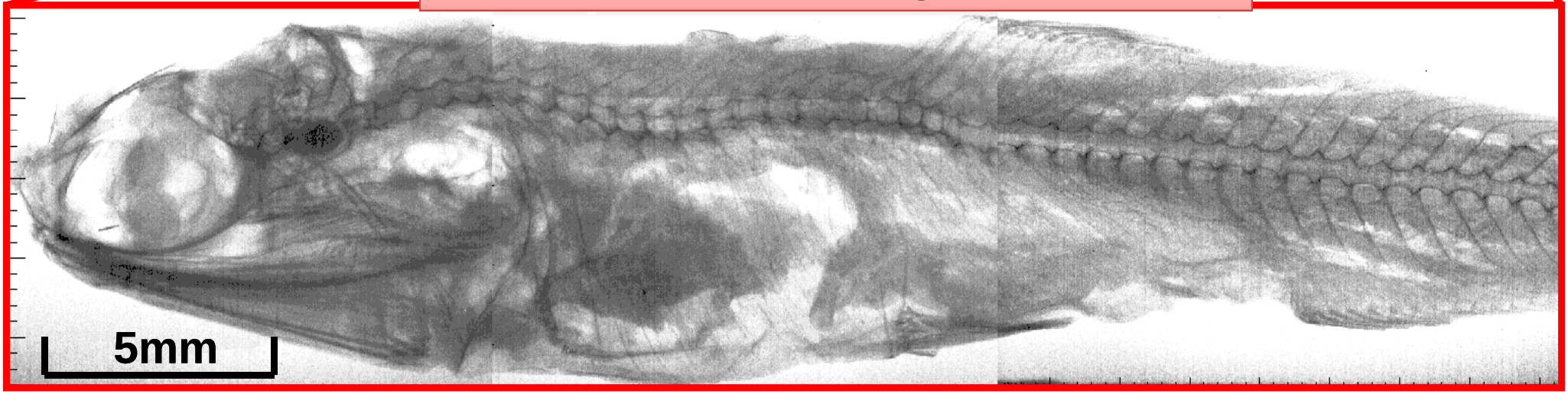








Fine resolution & High Contrast



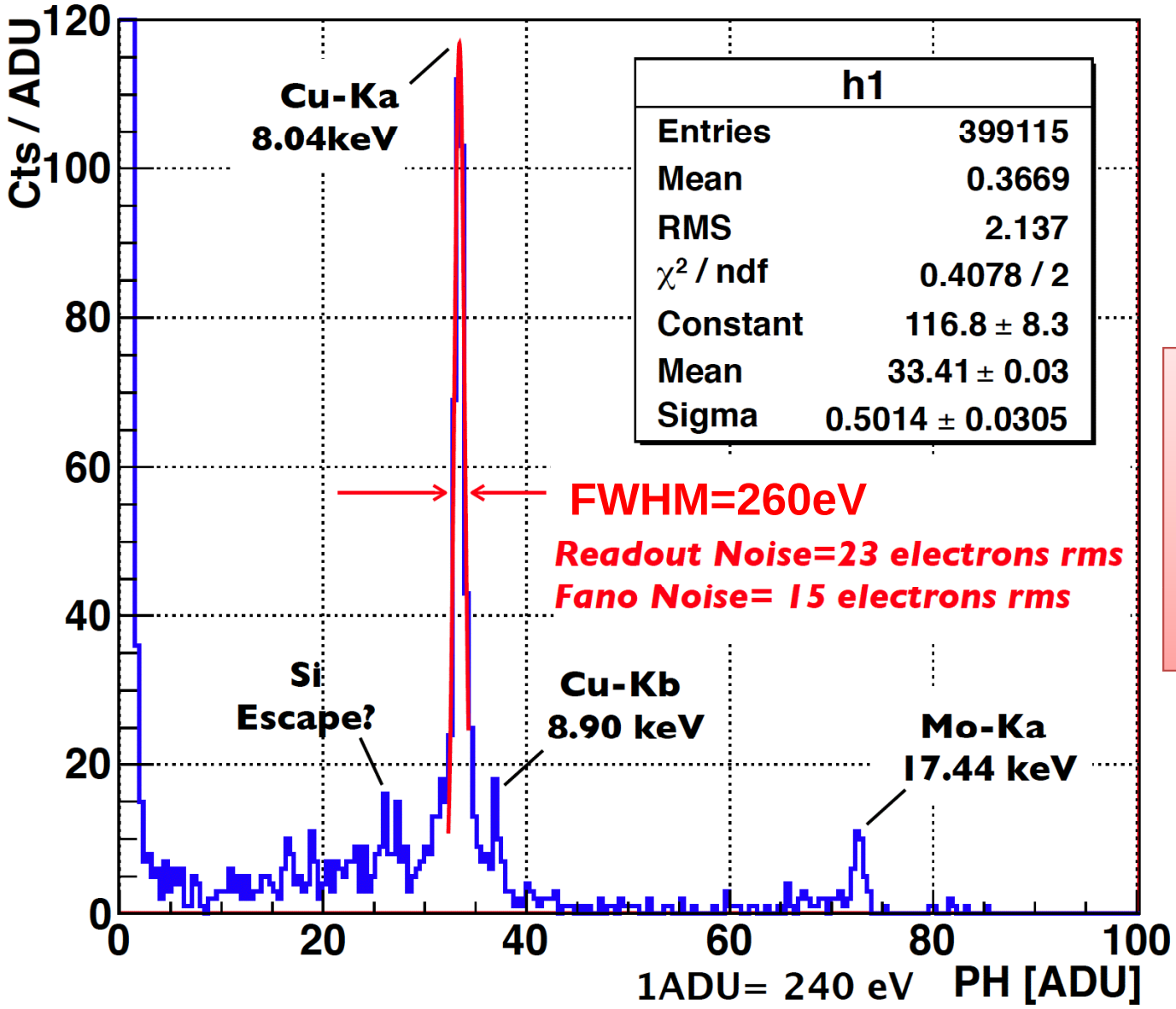
X-ray Image of a small dried sardine taken by a INTPIX4 sensor (3 images are combined).

(A. Takeda)

XRPIX1

◎ XRPIX1-CZ Correlated Multi Sampling 試験 2011/02/10@-50℃,100Vb

◎ 39D (ST&BT Type) Single Pixel (25,25) Spectrum (Target: Cu + Mo)



Cu Kα and Kβ is separated

Noise ~ 23e⁻ @-50°C

(Kyoto Univ.)

4. Summary

- SOI technology has many good features; low power, large range of operating temperature, low single event effect, vertical integration, ...
- SOI Pixel process becomes more stable and practical to use. Most of the technical problems are solved.
- We have ~twice/year regular MPW runs with increasing no. of users (Next MPW run is Oct. 3rd).
- Many pixel sensors are working and showing good performance.
- We welcome new users to the SOI pixel process.