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## Monolithic Radiation Image Detectors with SOI technology

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We have been developing monolithic radiation detectors based on OKI Semiconductor Co. Ltd. 0.2  $\mu\text{m}$  Fully-Depleted Silicon-on-Insulator (FD-SOI) CMOS technology. The SOI wafer is composed of a thick high-resistivity substrate (for sensor part) and a thin low-resistivity Si layer (for CMOS circuitry) sandwiching a buried oxide (BOX) layer. After removing the top Si and the BOX layer in the region of the sensing nodes, p or n dopant is implanted to the substrate. In the SOI detector, there is no mechanical bump bonds, so the capacitance of the sensing node is very small and has very high sensitivity.

Many kinds of detectors are being developed for applications such as X-ray imaging, astrophysics and high-energy physics experiments. In addition to simple integration type detector, we have also developing counting type pixel to utilize the SOI advantage. Largest chip we developed so far is 10.2 mm by 15.4 mm in size having 512 x 832 pixels, each 17  $\mu\text{m}$  square and including correlated double sampling (CDS) function.

A new implantation process which creates buried p-well (BPW) layer under the BOX layer is introduced to circumvent the back gate voltage problem inherent in the SOI radiation sensor. There are other benefits in the BPW process such as increase of break down voltage and radiation hardness.

Recently we have succeeded to process Floating-Zone (FZ) SOI wafer instead of normal CZ-SOI wafer by adjusting thermal load. The FZ-SOI wafer has higher resistivity ( $>10 \text{ kohm-cm}$ ) compared with CZ-SOI wafer, so we could easily achieve full depletion of thick sensor ( $> 260\mu\text{m}$ ) without breakdown.

We have been operating regular MPW runs of the SOI process two times per year. Many institutes including foreign institutes are participating the MPW run each time. Recent progress of the SOI detectors will be reported.

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