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Wafer Level 3D Integration Technologies

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Wafer level packaging processes has been used over several years in hybrid pixel module manufacturing. Deposition processes like electroplating, sputtering as well as evaporation are well established technologies for the formation of interconnection structures on readout chip wafers as well as on sensor wafers. Following the packaging roadmaps to higher integration, increased functionality and a reduction in size 3D wafer level packaging technologies come into the focus of technology development. The formation of Through Silicon Vias (TSVs) is a key technology for the fabrication of 3D architectures on wafer level. Therefore new concepts of wafer thinning, thin wafer handling and via filling processes have to be developed. An overview of 3D integration technologies will be given focusing on the special requirements for pixel module fabrication. Chip size packages for different applications using 3D wafer level integration technologies were fabricated at Fraunhofer IZM. Examples of 3D chip size packages using TSV technology will be described in detail in this presentation.

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