CMS Pixel Phase I Upgrade:

System Test at UZH

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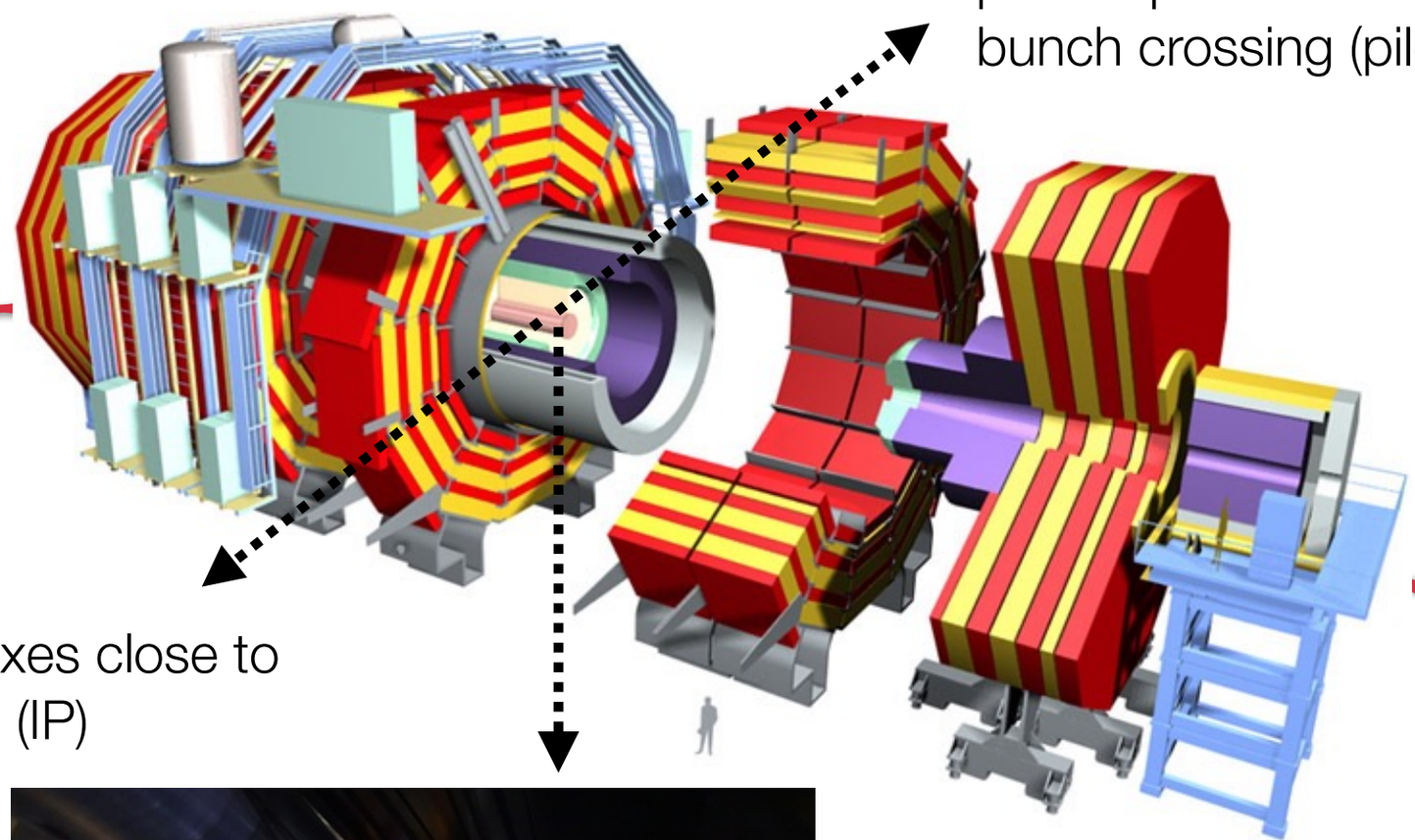
Joint PhD Seminar
26-27 August, 2015
PSI

The CMS Detector at LHC

LHC now delivering proton-proton collisions @ 13 TeV!

expected average of ~ 25 proton-proton collisions per bunch crossing (pileup)



proton beam

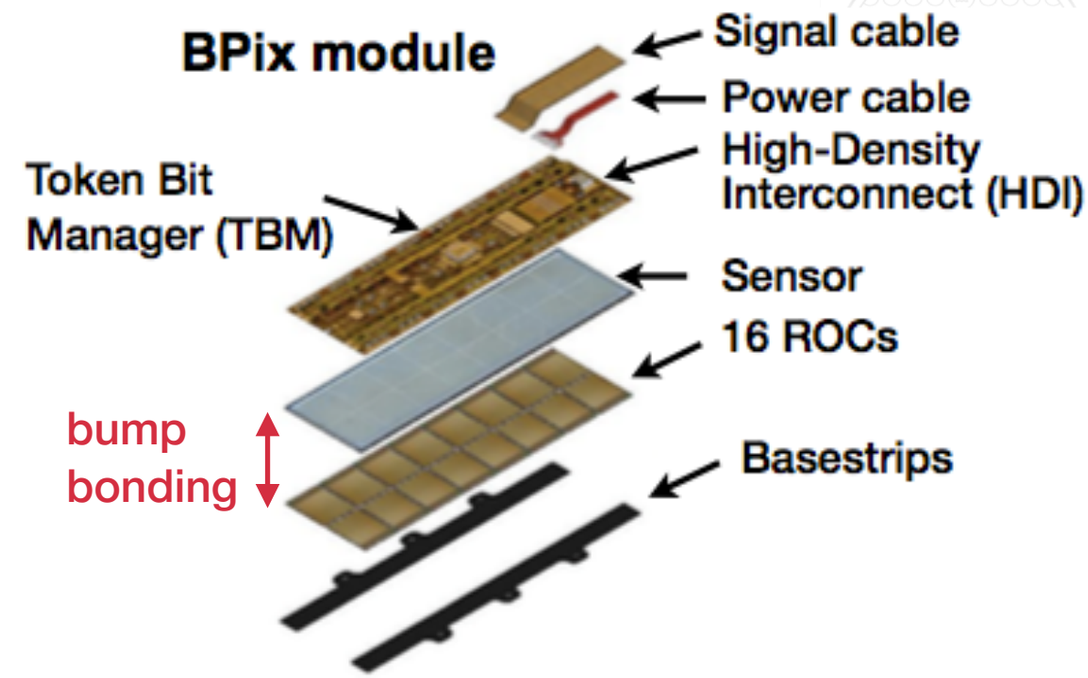
proton beam

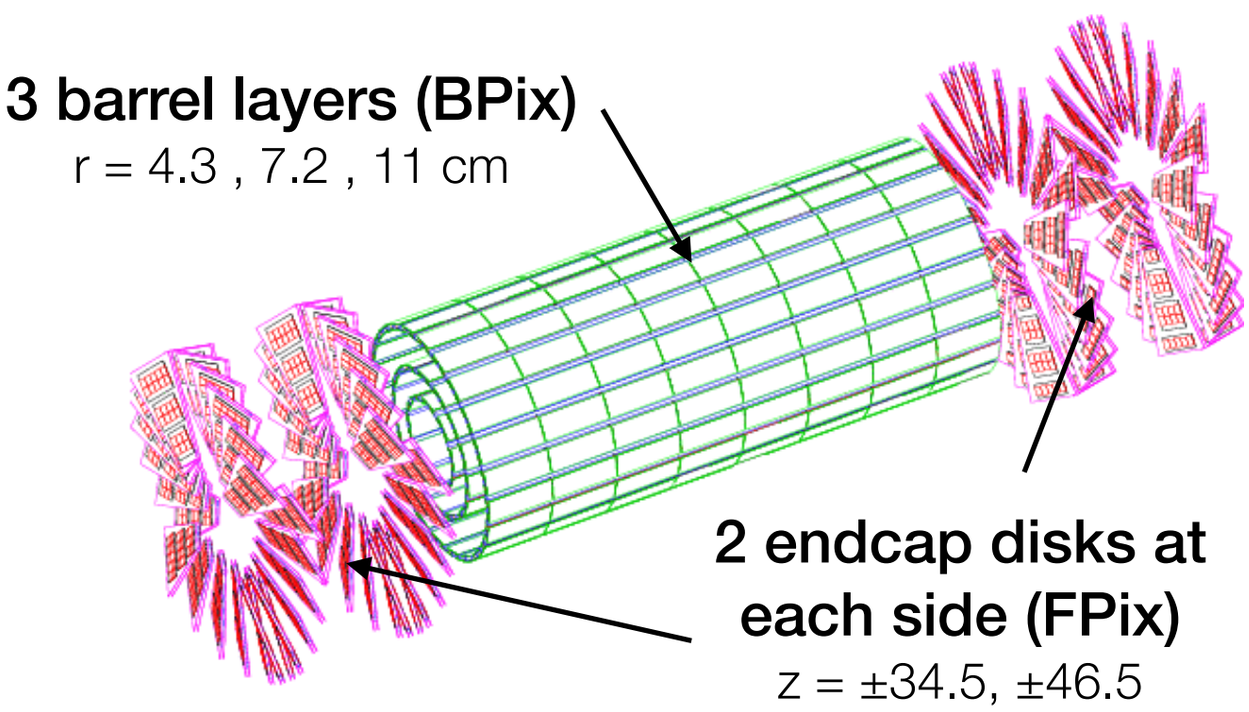
very high particle fluxes close to the interaction point (IP)

The inner **Pixel Detector** provides spatial information with high resolution close to the IP

The CMS Pixel Detector

- Sensors technology:
  - n+ implants on n doped silicon bulk
  - pixel size : 100x150 μm^2
- A **Readout Chip (ROC)** serves an array of 52x80 pixels
  - each pixel is soldered to the ROC through "bump" bonding

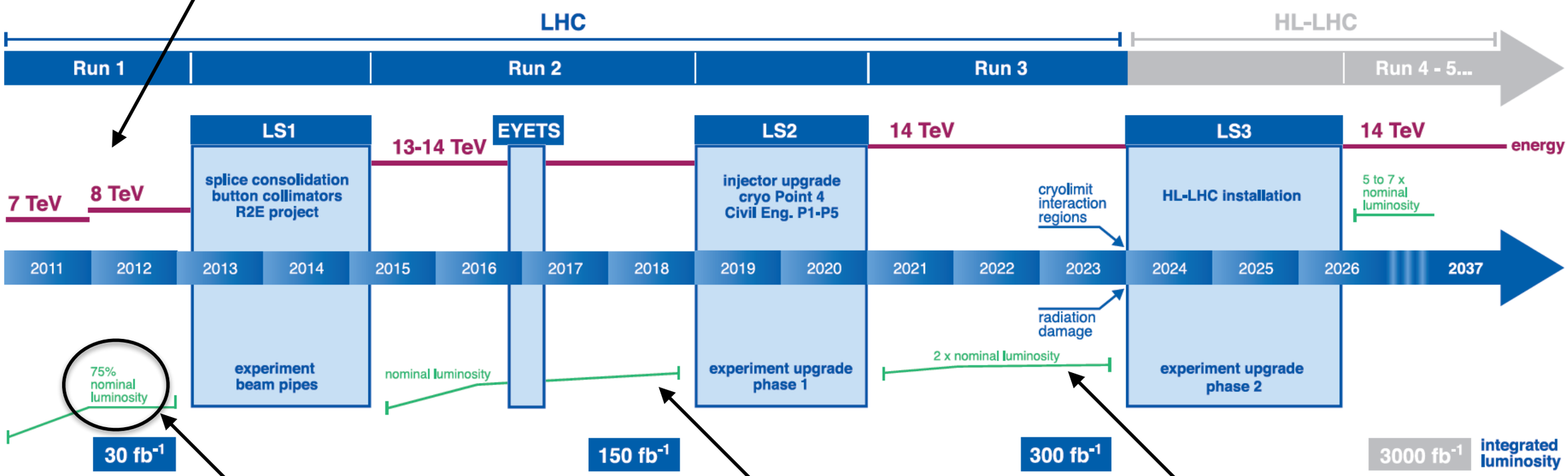




- High hit resolution ~ 10 μm
- High tracking efficiency
- High track impact parameter resolution and precise vertex reconstruction
  - separation of primary vertex from pileup vertices
  - efficient tagging of long-lived particles through secondary vertices
- Provides seeds for track finding

CMS pixels & LHC schedule

Excellent performance of the Pixel Detector during first LHC run



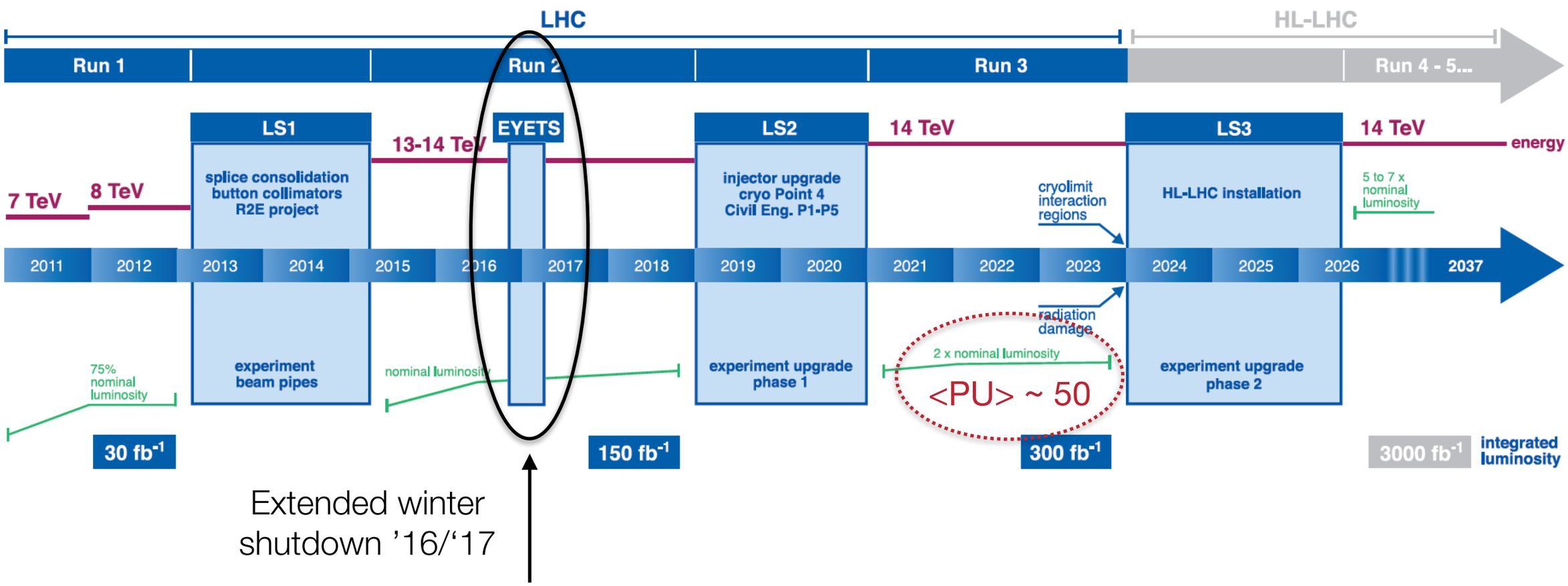
Current Pixel Detector designed for the nominal luminosity of $1x10^{34}cm^{-2}s^{-1}$ → almost reached during RunI

Plan to exceed the nominal luminosity in the second part of RunII…

…and to double it in RunIII → $2x10^{34}cm^{-2}s^{-1}$

CMS pixels & LHC schedule

High luminosity → high track density , trigger rates and pileup



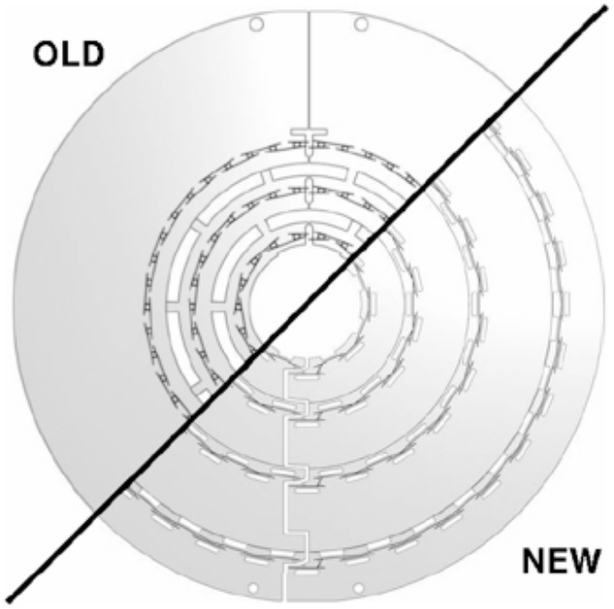
Extended winter shutdown '16/'17

Need for a replacement to maintain the current level of performance under high luminosity conditions!

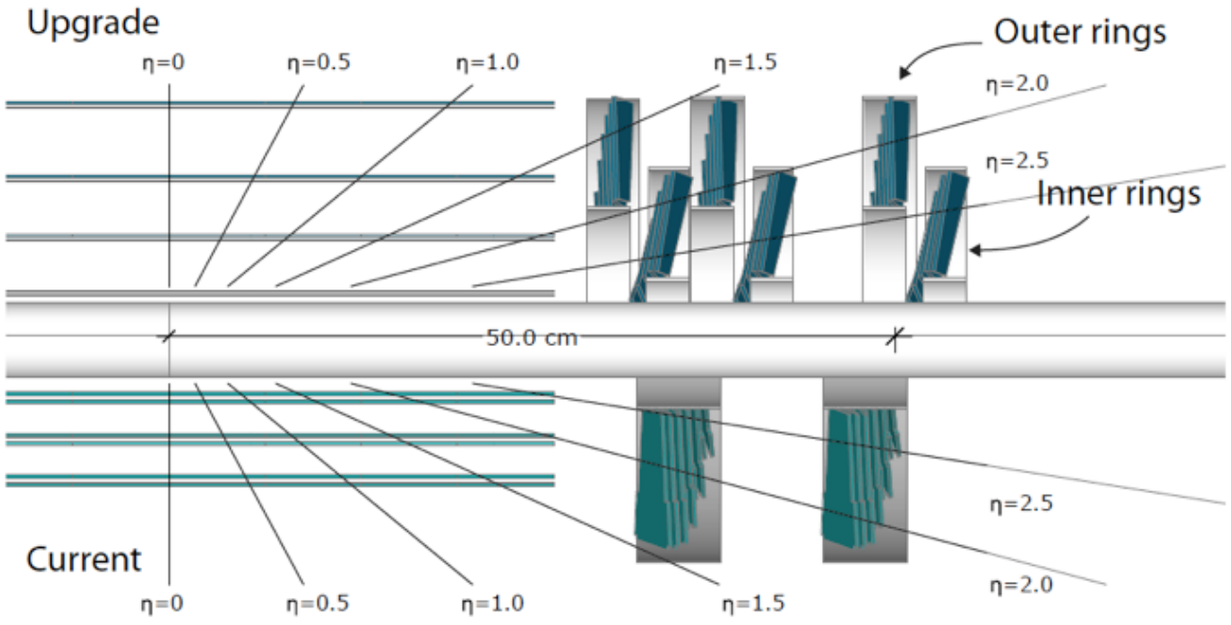
→ CMS Pixel Phase I Upgrade

CMS Pixel Phase I Upgrade

- New digital Readout Chip
  - faster digital readout (40MHz → 400Mbit/s) for high rates
  - increased buffer size
  - reduced dead time → reduced data loss
- One additional layer
  - 3 → 4 barrel layers , 2x2 → 2x3 endcap disks
  - robust vertexing at large pileup and improved track seeding



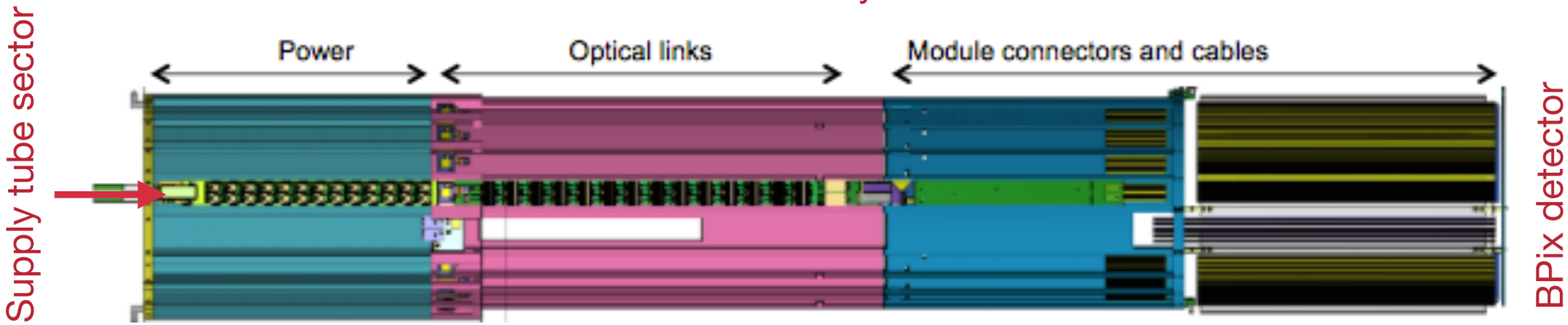
- Shift electronic boards to high |η| + lightweight mechanics and CO2 cooling
  - less multiple scattering and photon conversion due to material in the fiducial tracking volume
  - improved impact parameter resolution

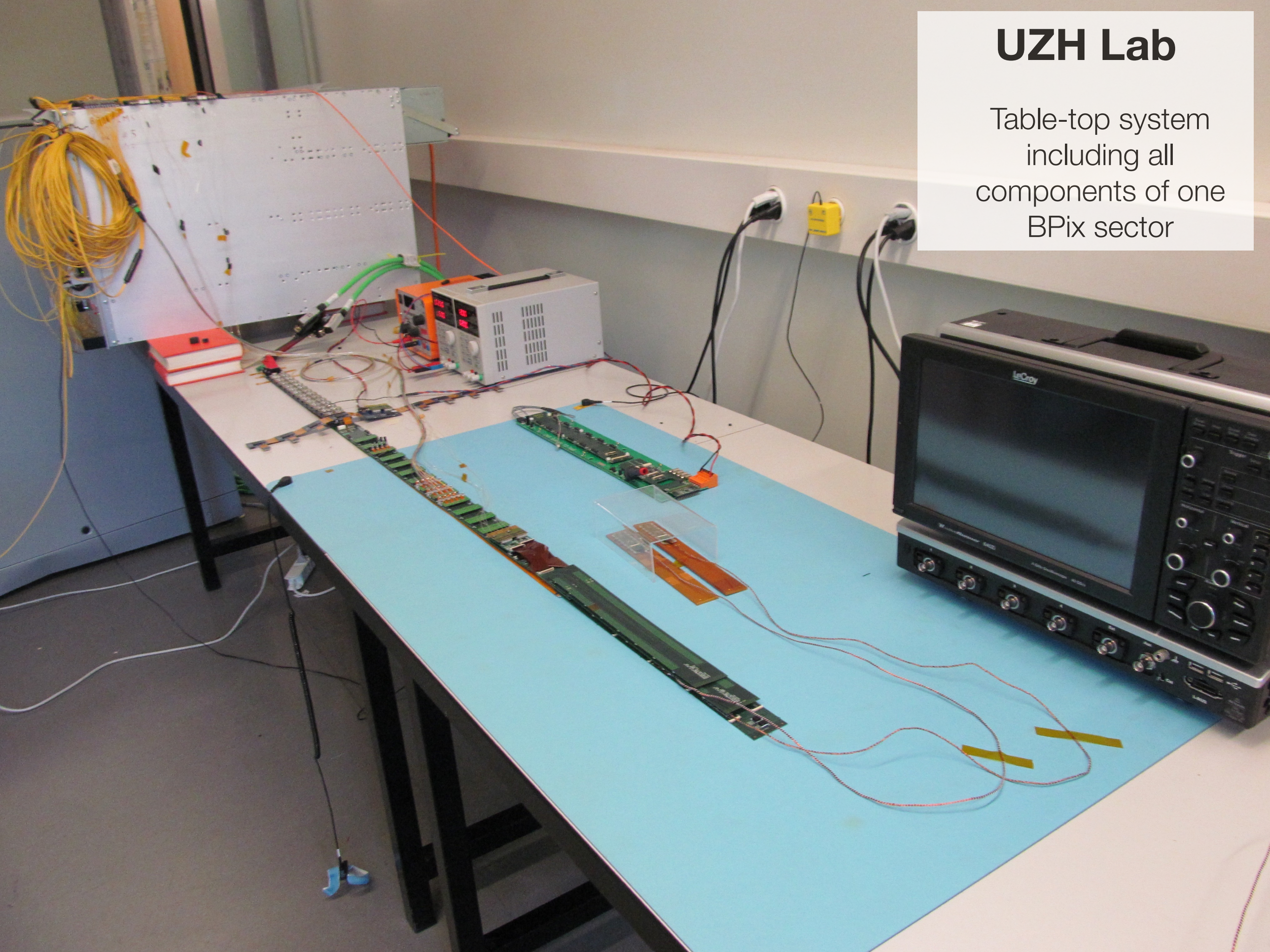


Upgrade system: service cylinders

- Service cylinders house power, readout electronics with optical converters and cooling lines
- <u>UZH responsibilities for BPix service cylinder:</u>
  - design and build mechanical structure and cooling lines
  - test and integrate final components and integration of the complete system (4 supply tubes)
- Currently we have integrated all the components of one sector on a table-top system
  - test each components in view of final production
  - develop test and procedures to be used during assembly of the final system

BPix service cylinder



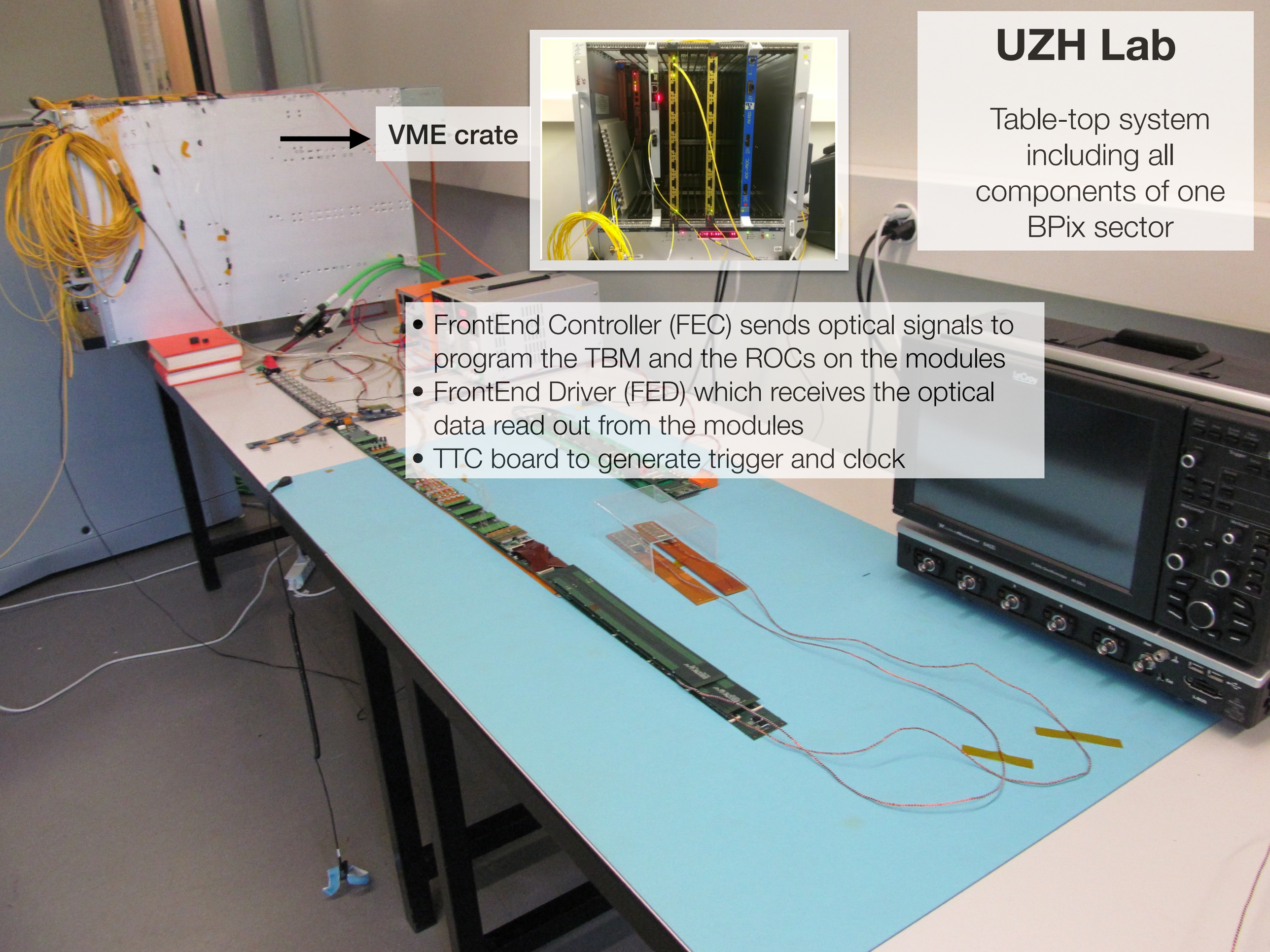


UZH Lab

Table-top system including all components of one BPix sector

UZH Lab

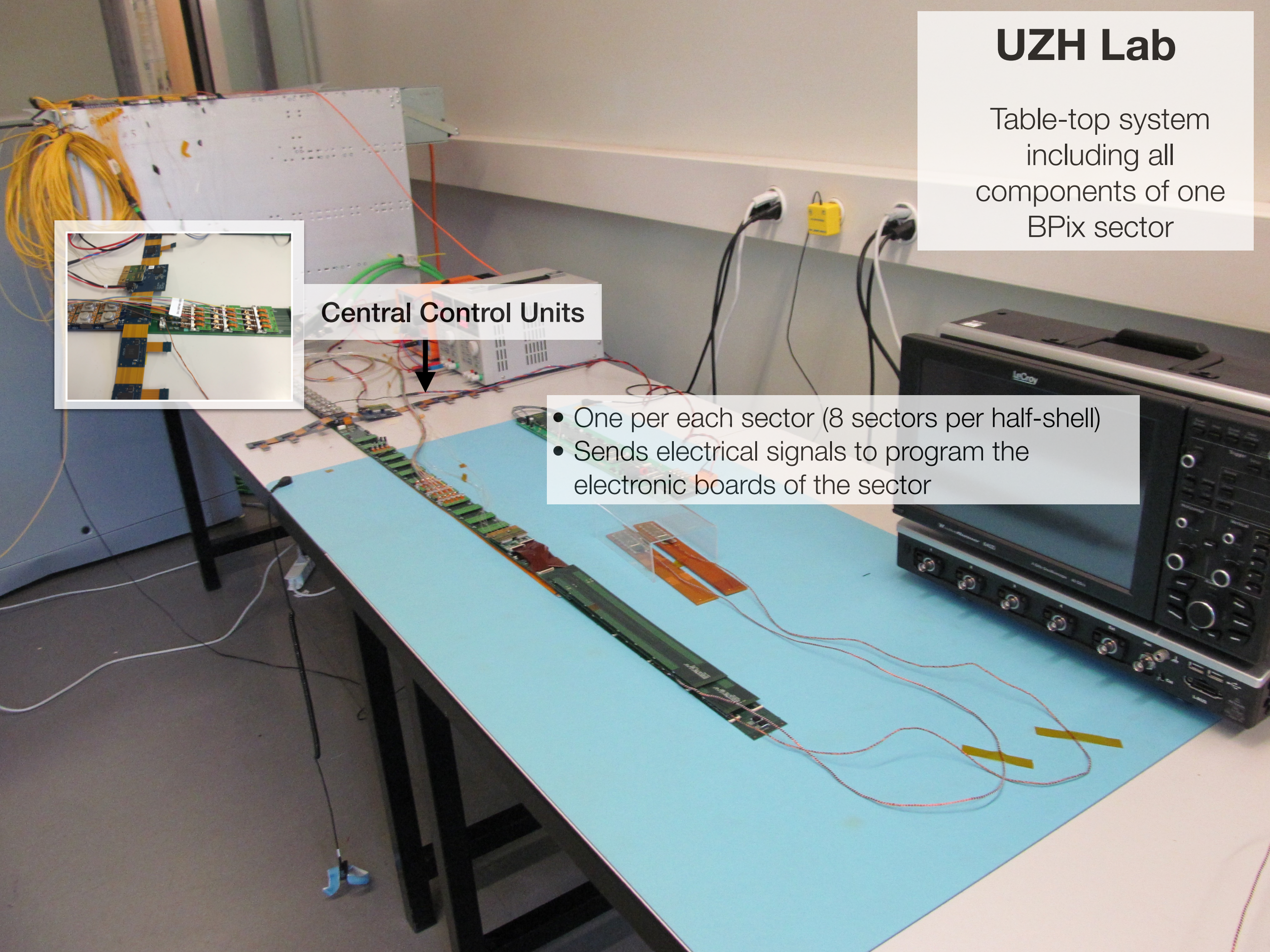
Table-top system including all components of one BPix sector



- FrontEnd Controller (FEC) sends optical signals to program the TBM and the ROCs on the modules
- FrontEnd Driver (FED) which receives the optical data read out from the modules
- TTC board to generate trigger and clock

UZH Lab

Table-top system including all components of one BPix sector



Central Control Units

- One per each sector (8 sectors per half-shell)
- Sends electrical signals to program the electronic boards of the sector

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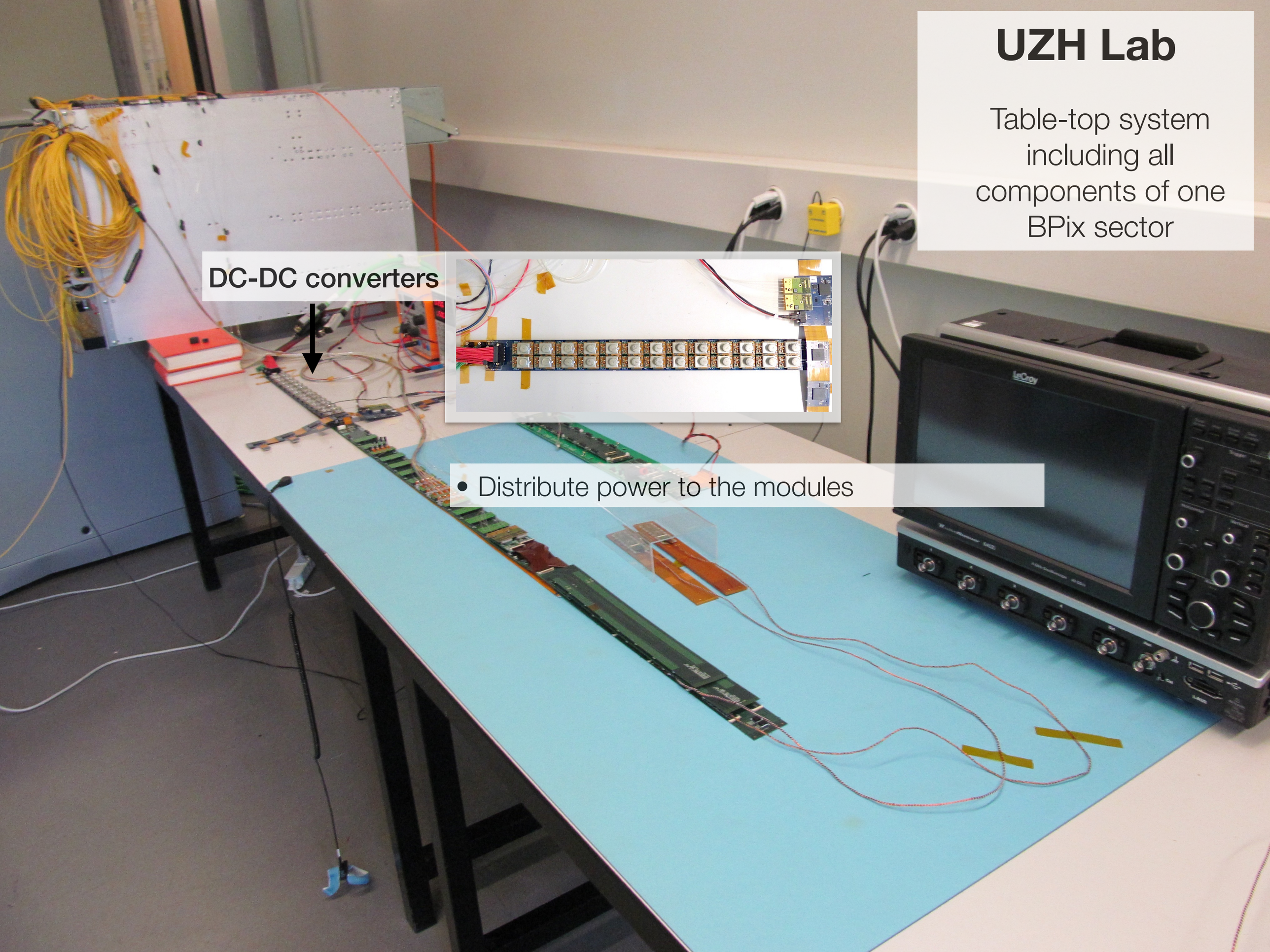
Table-top system including all components of one BPix sector



- Distribute power to the modules

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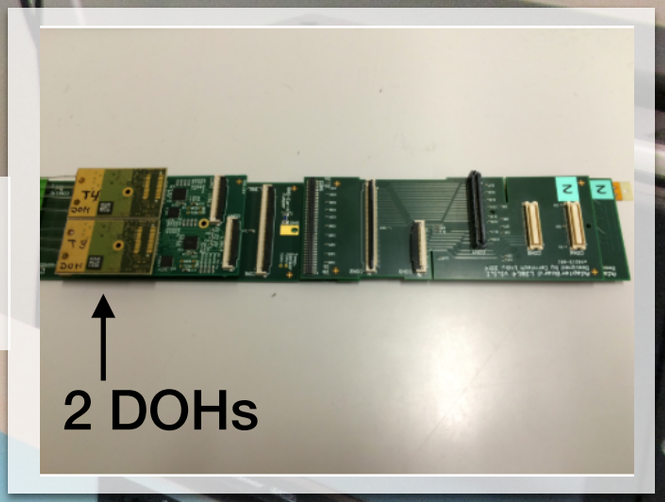
Table-top system including all components of one BPix sector

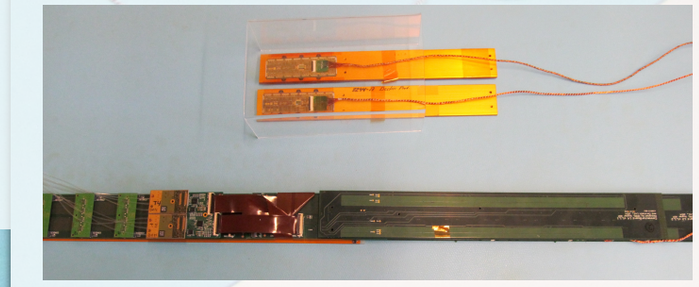
- Mother board equipped with Digital Optohybrids (DOHs)
- Digital-to-optical links from the FEC to the modules for module programming

Digital-optical control link



- Transfer digital programming and readout signals to and from the modules

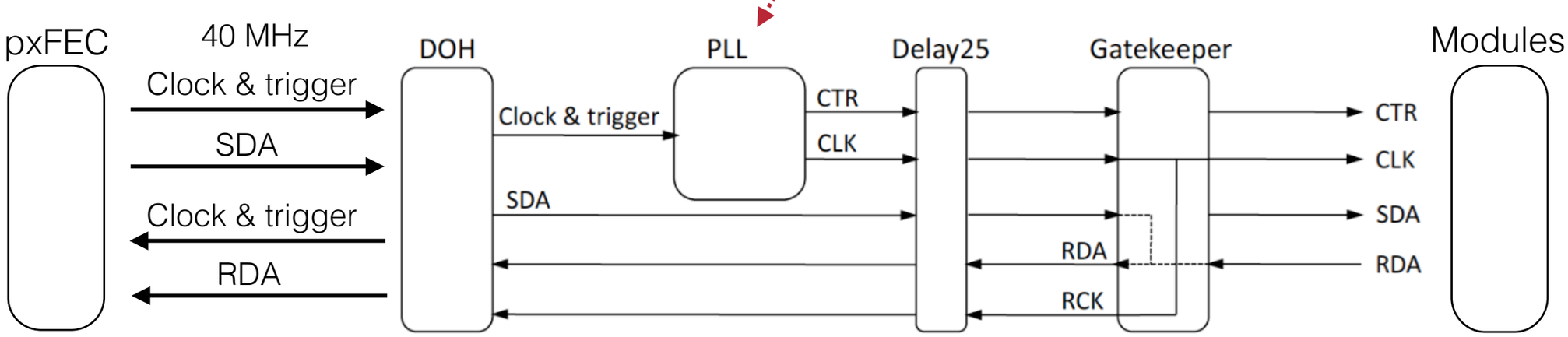
Adapter and connector boards with two modules



Module programming (I)

The FEC sends the clock and trigger information together with programming signals through the DOHs to the detector

A phase locked loop (PLL) chip is used to split the clock from the trigger information before sending it to the detector modules



The LHC clock and trigger information is encoded in one signal which is sent over a single fiber to the DOH

The Delay25 chip adjusts the relative phases of all programming signals

A Gatekeeper chip converts the low voltage differential signal used by the PLL and the Delay25 to a low current differential signal (LCDS) used by the ROCs

Module programming (II)

clock, trigger and programming signals transmission:

- 2 DOHs connected to DOH mother board (MB): L12 & L34
- 2 adapter boards connected to DOH MB: L12 & L34
- 3 connector boards (L12, L3 & L4) equipped with LCDS and module connectors and connected to adapter boards

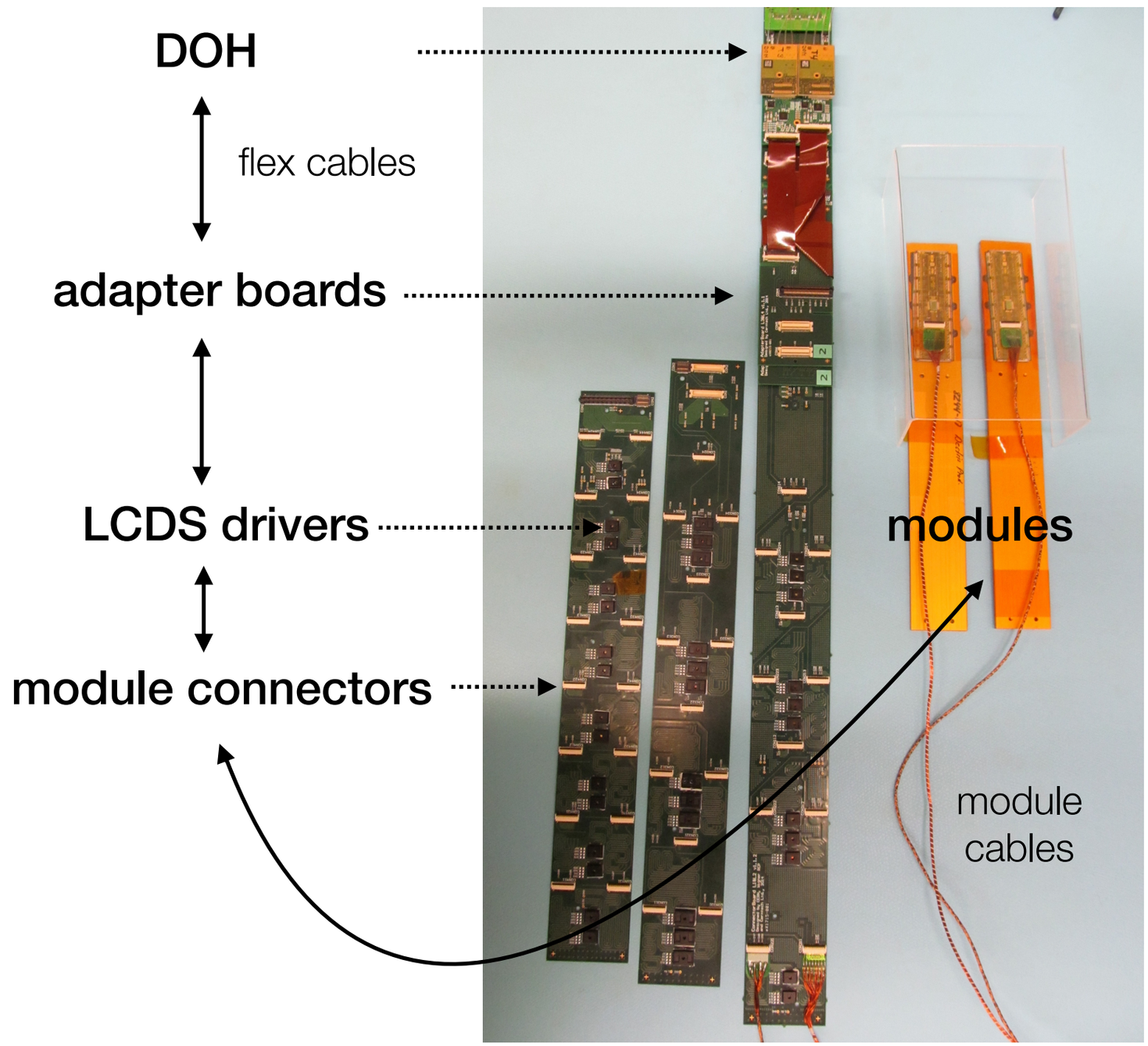


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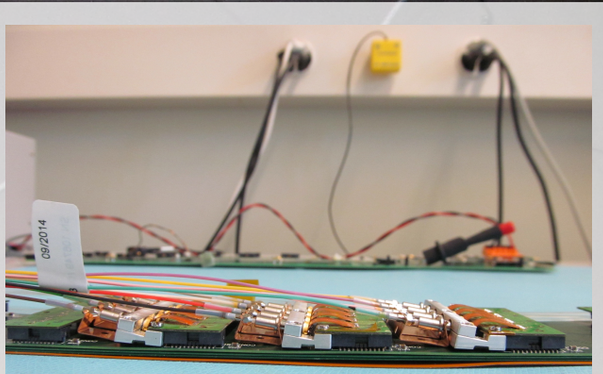
Table-top system including all components of one BPix sector

Readout optical links

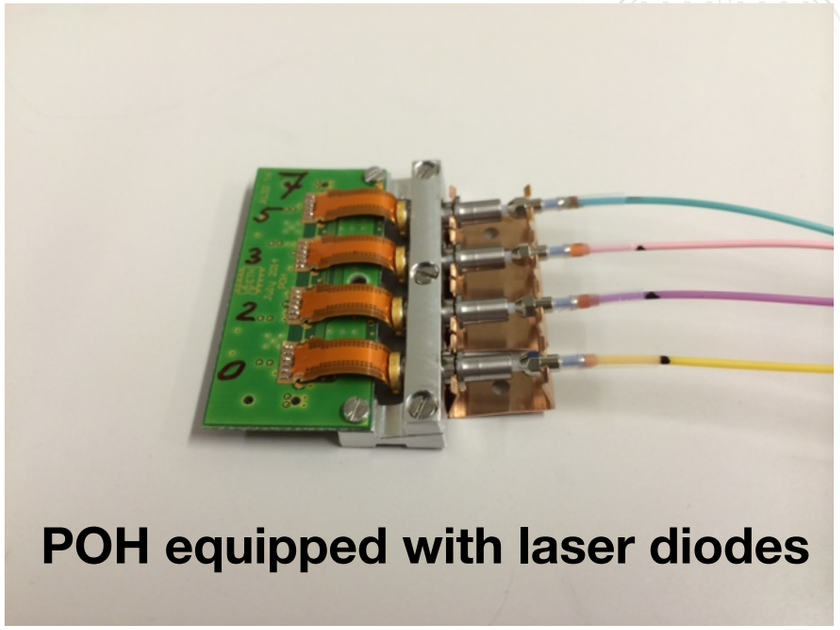


POHs

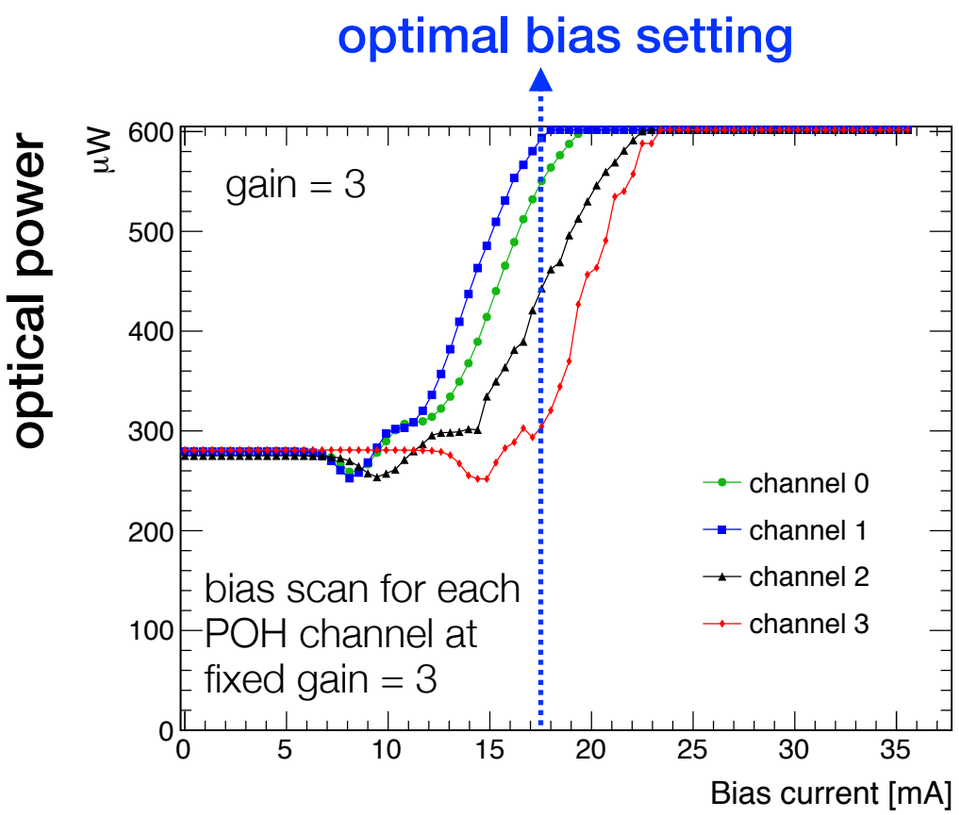
- Mother board equipped with Pixel Optohybrids (POHs)
- Each POH receives readout signals from the modules and convert them to optical signals to be sent to the FED

Optical readout

- Pixel Optohybrid (POH) converts the module digital output signal to optical signals through laser diodes
- Each POH equipped with 4 lasers (channels) each connected to an optical fiber
- The laser gain and bias settings have to be initialized to proper values to optimize the quality of the module readout signal

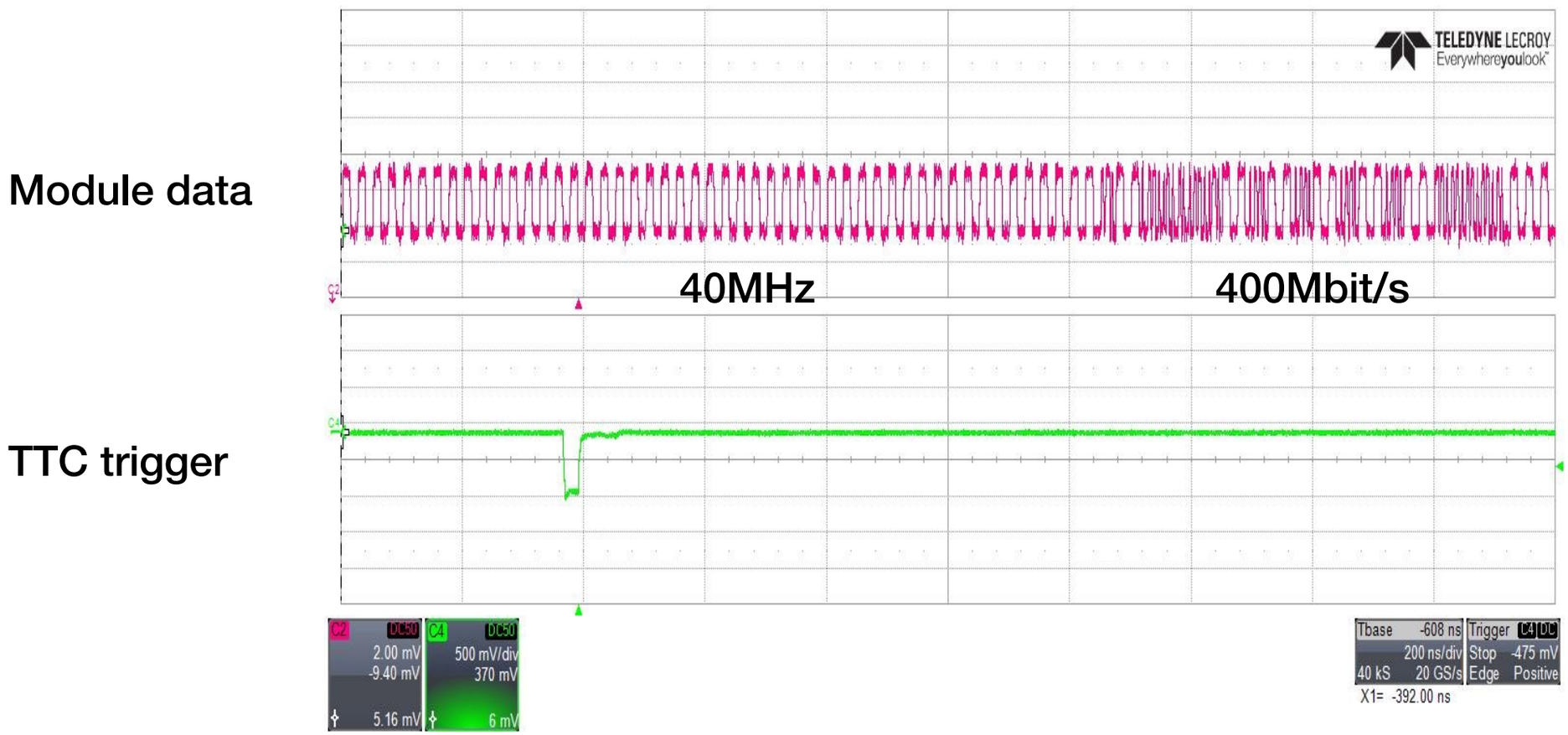


POH equipped with laser diodes



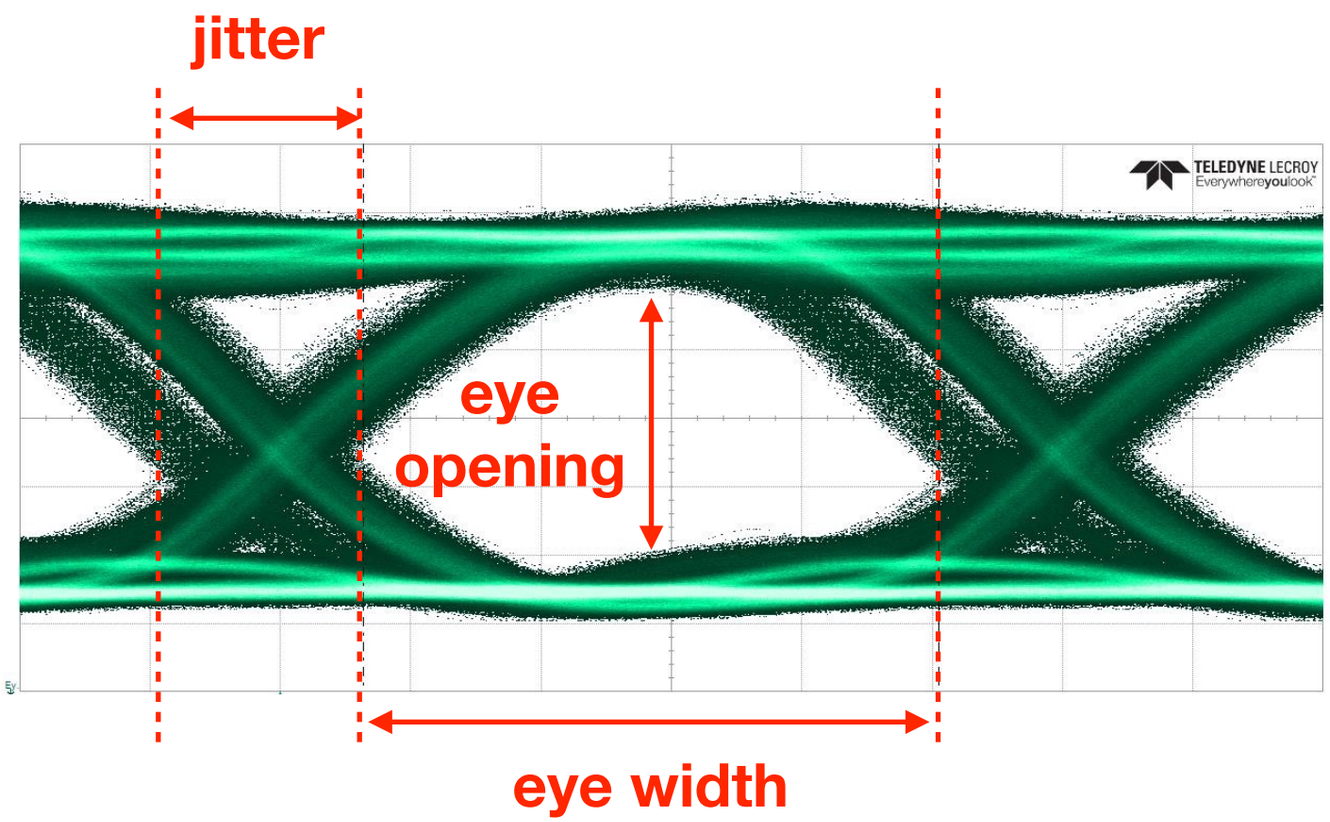
Module readout signal

- If trigger is not sent to the module → 40 MHz idle pattern
- If trigger arrives to the module → 400Mbit/s digital output signal
  - TBM header + 16 ROC headers + TBM trailer



Optical signal quality (I)

- The optical signal quality is analyzed sampling the 400Mbit/s digital signal for each trigger at a defined trigger rate
- The negative (zeros) and positive (ones) states are overlaid producing an **“eye diagram”**
  - ideally the diagram would look like rectangular boxes
  - in reality the signals are not perfectly squared and the transitions do not lay perfectly on top of each other
- The **eye width** gives information about the jitter
- The **jitter** represents the deviation from true periodicity due to misalignment of rise and fall edges
- The **eye opening** gives information about additional source of noise in the signal amplitude

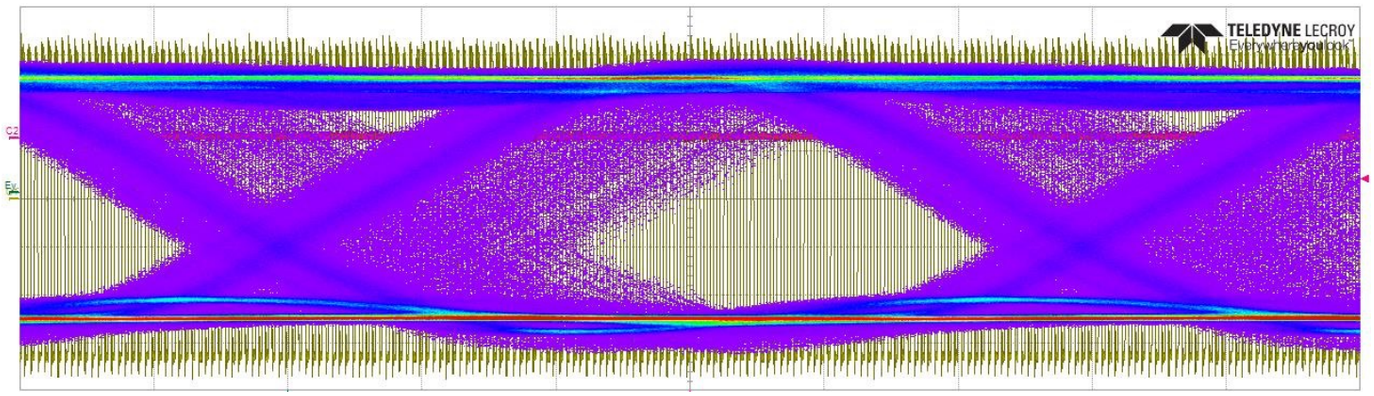


Optical signal quality (II)

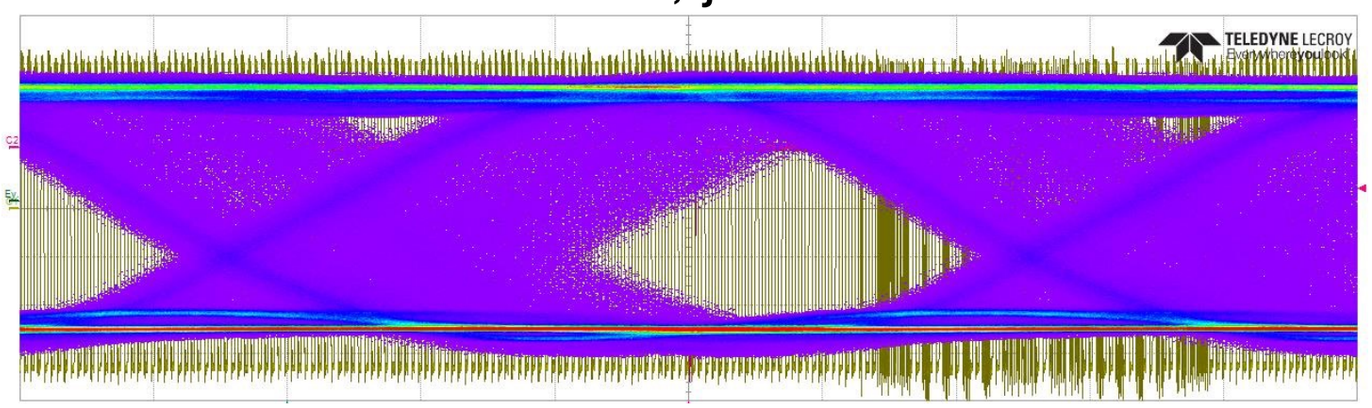
- Measured large jitter on readout module signal for high trigger rates due to jitter on the clock line caused by the PLL

- DOH motherboard design has been optimized to improve clock signal by introducing new QPLL (PLL based on quartz crystal oscillator)

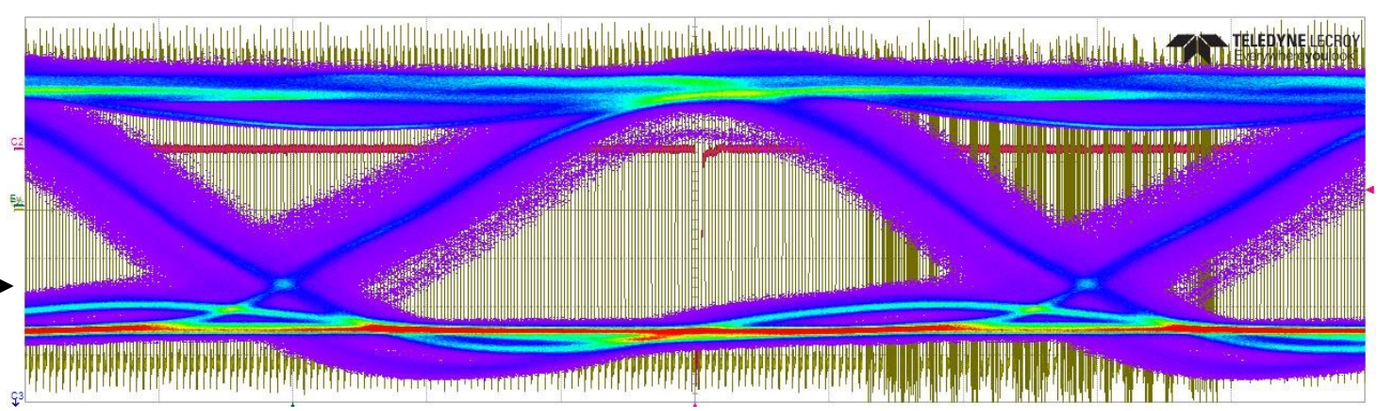
PLL @ 10Hz, jitter ~ 2.8 ns



PLL @ 10kHz, jitter ~ 3.4 ns



QPLL @ 10kHz, jitter ~ 1.9 ns



Conclusions

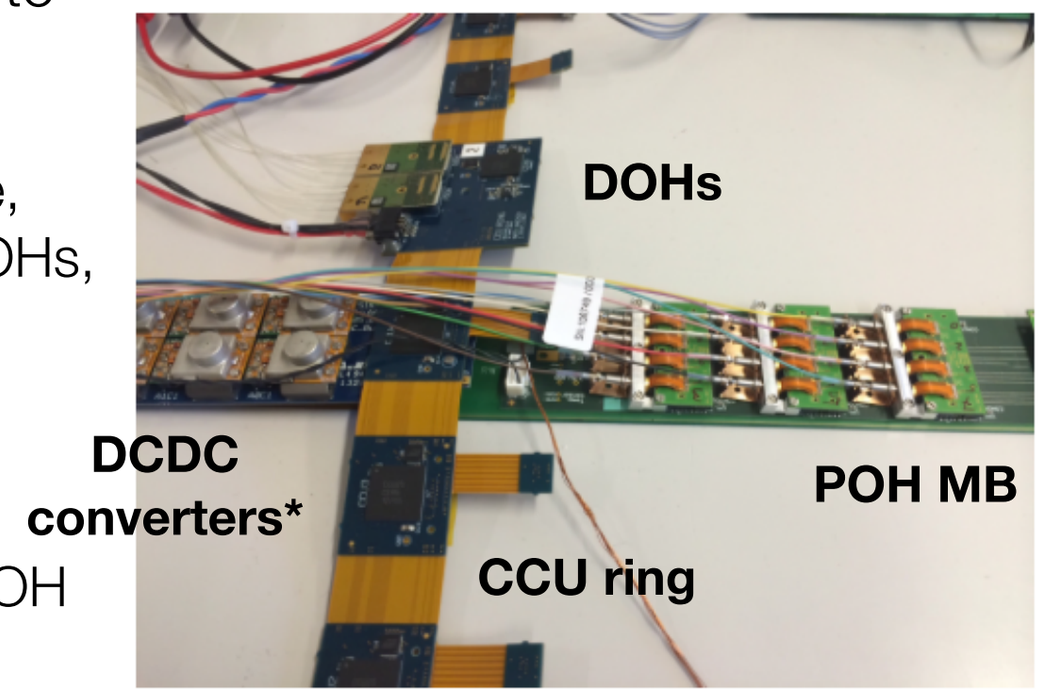
- Current CMS Pixel Detector will be replaced by Phase I pixel system during extended LHC winter shutdown 2016/2017
- Prototypes of all final components of the BPix service cylinders are available and are currently tested at the University of Zurich
- Described the system test setup at UZH and presented some of the results
- Many other tests have been performed with the goal of giving a final word before the full production
  - tested also mechanical aspects of the system
  - found problems in the logic of electronic boards which will need modifications or adjustments
- Now focusing on the development of automatic procedures in view of the assembly of the final system

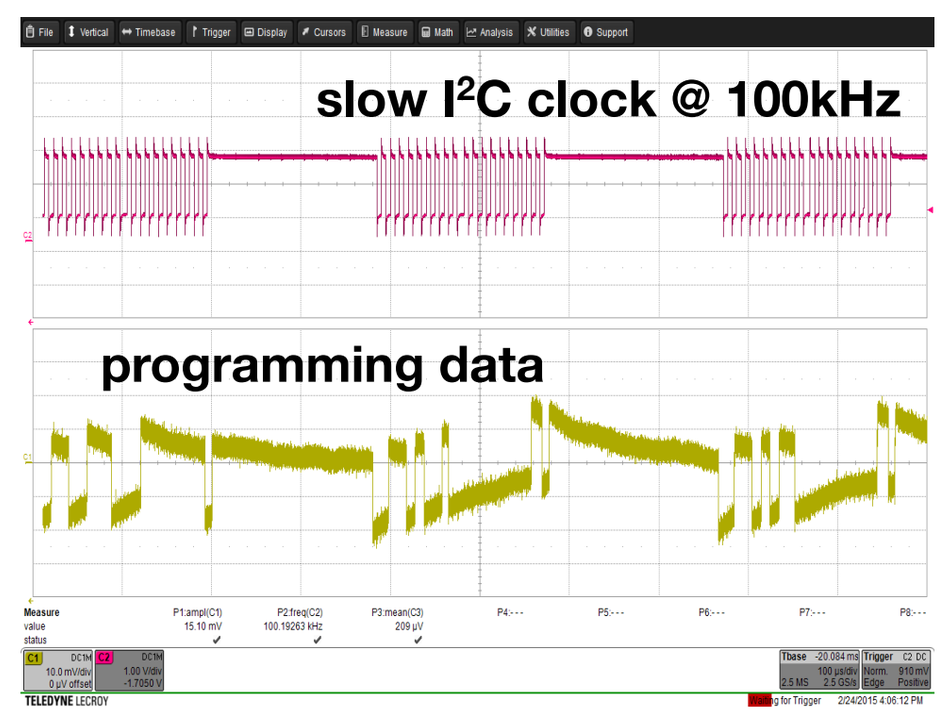
Backup Slides

Slow control

- CCU ring with 8+1 CCUs (Aachen) connected to TrackerFEC through 2 DOHs
  - successfully tested: FEC-CCU ring architecture, redundancy scheme, I²C communication to DOHs, functionality and control of DCDC converters
- One CCU connected to POH MB
  - measured slow I²C signal quality on different POH connectors
  - successfully tested slow I²C speed and POHs programming
- DOH MB mounted on POH MB and equipped with two DOHs (L12 and L34) connected to pxFEC
- Successfully tested DOHs, Delay25 and PLL chips programming through slow I²C

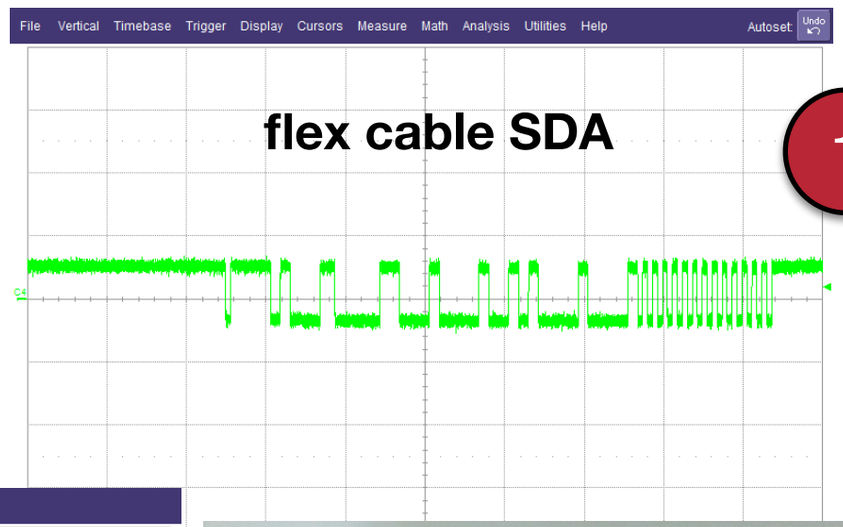
* DCDC converters → Deborah's talk

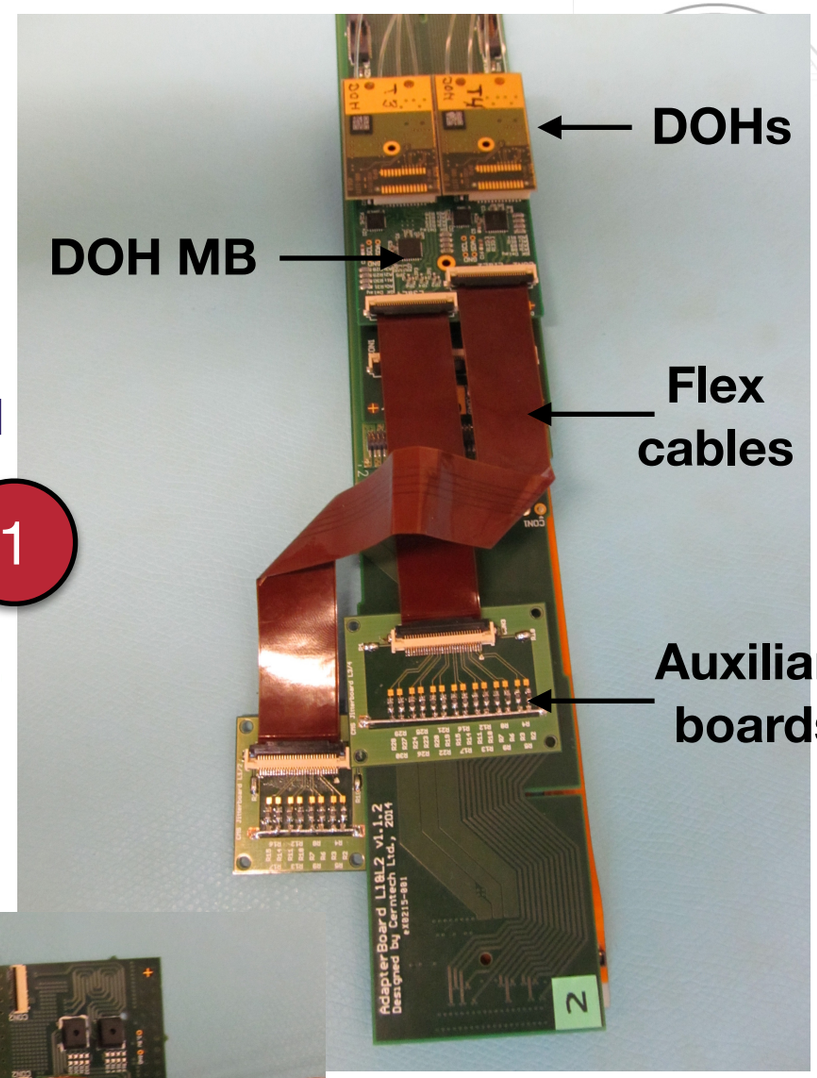


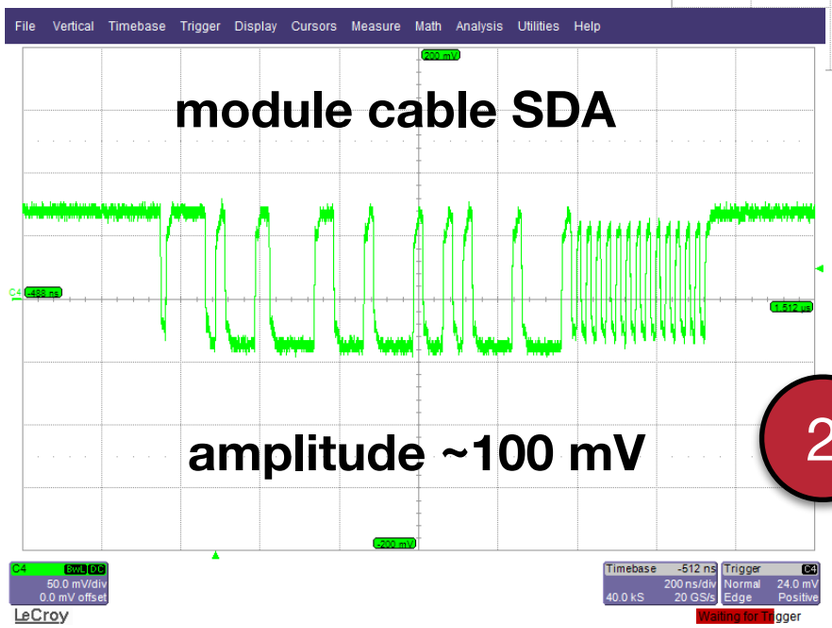


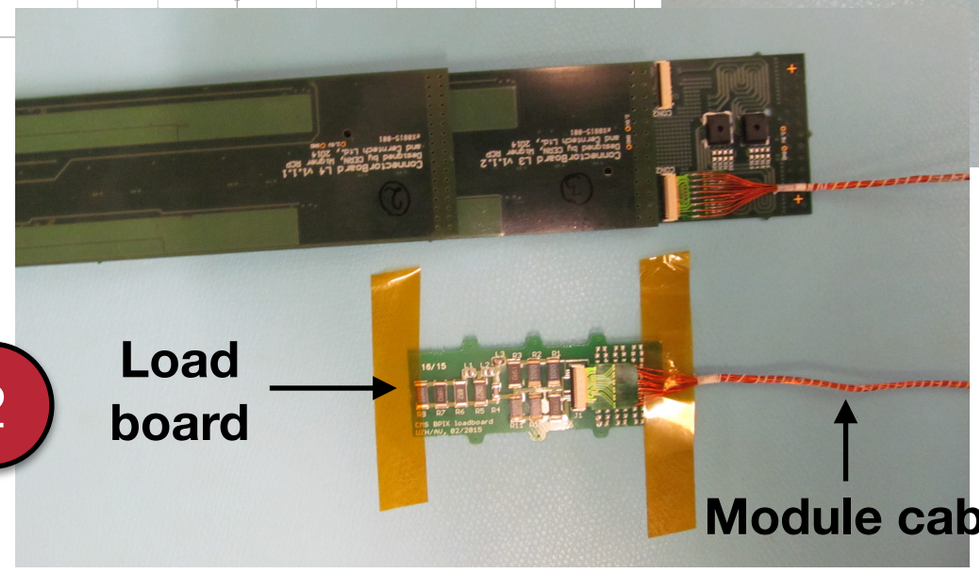
Module programming (II)

- Measured clock, trigger and fast I²C signals
  1. at the end of flex cables using “auxiliary” boards
  2. at the end of module cable using load boards



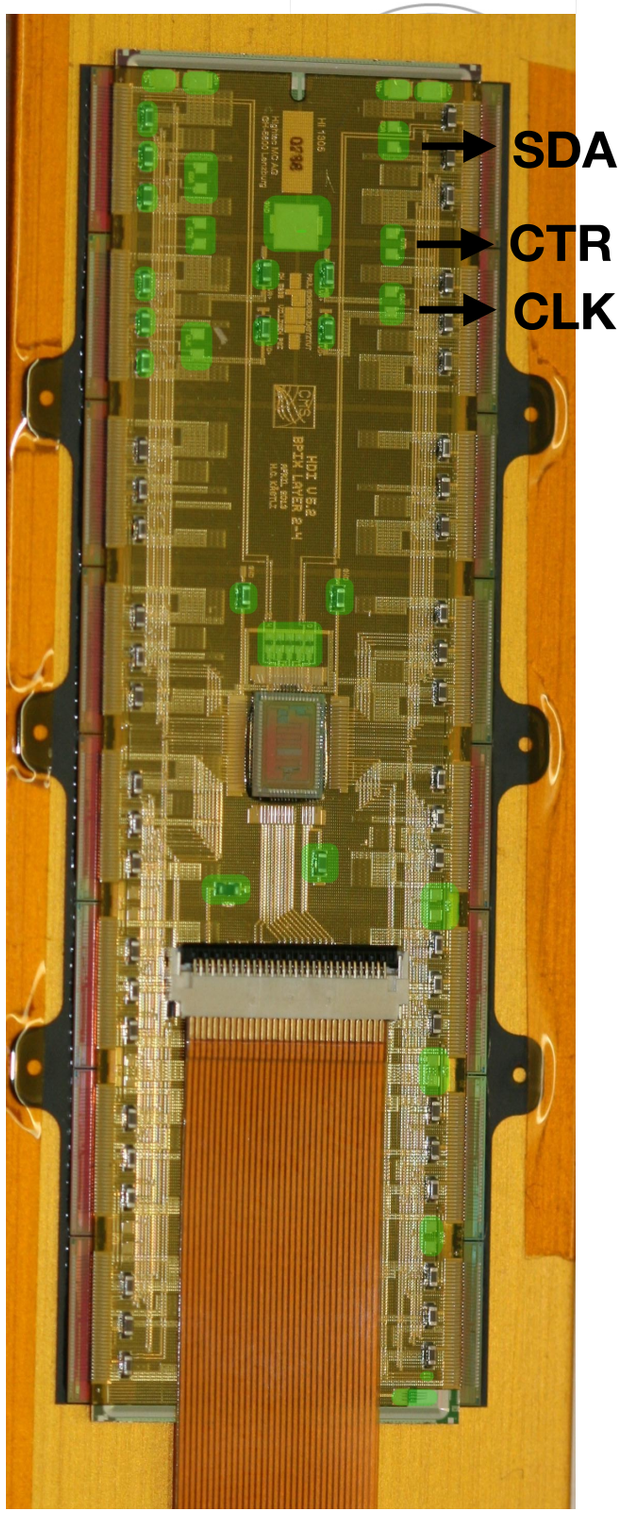




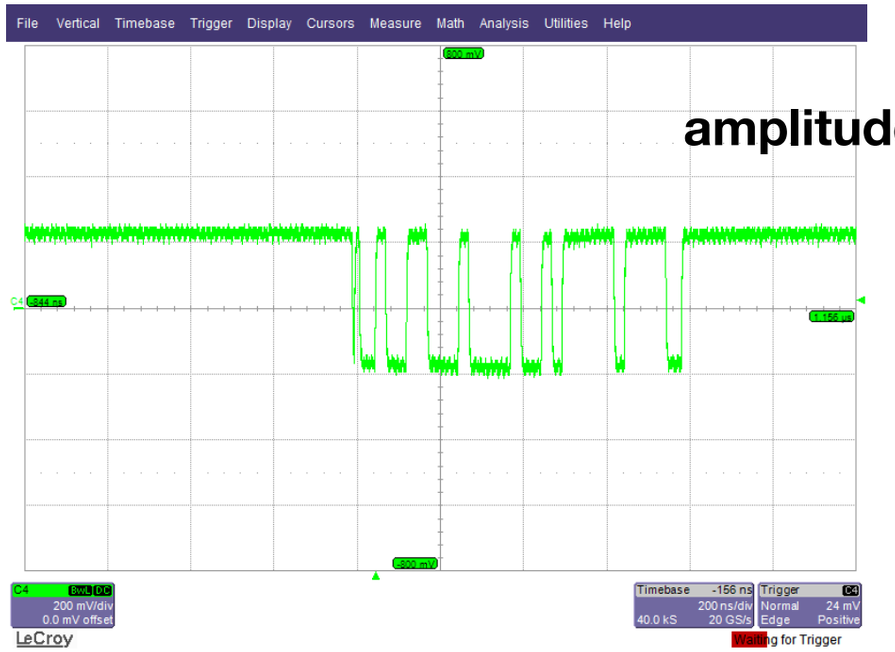


Module programming (III)

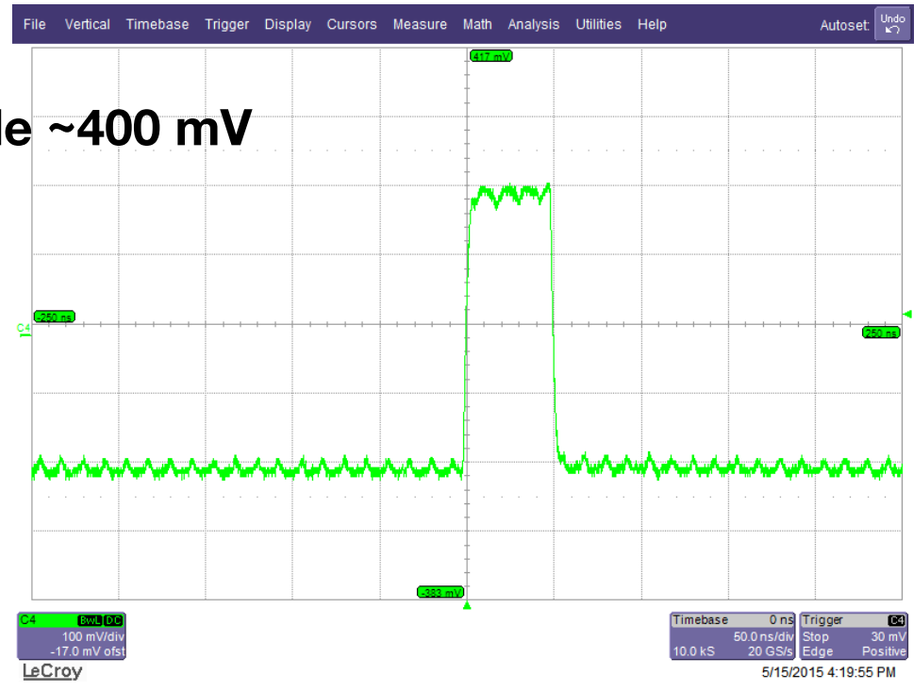
- Measured clock, trigger and SDA on the module HDI test pad
- Verified module programming (changes in analog current with Vana)
- Only tested few connectors for L12 and L3 connector boards



HDI SDA



HDI CTR



amplitude ~400 mV

Module readout (I)

- Verified readout chain injecting random data with Digital Test Board directly into POH MB and into connector boards
- verified complete connector to POH channel mapping for all 4 layers
  - module assignment in the readout does not match the I²C addressing
- transmitted signal not visible for some of the connectors on L4 connector board → still need to investigate
- Plans to use this setup to measure the quality of the transmission line (eye diagrams)

POH	module readout	i2c addressing
1	L1	0x11
2	L2	
3	L4	
4	L1	
5	L4	
6	L2	
7	L2	

POH	module readout	i2c addressing
8	L4	0x13
9	L1	
10	L3	
11	L4	
12	L2	
13	L3	
14	L3