PAUL SCHERRER INSTITUT

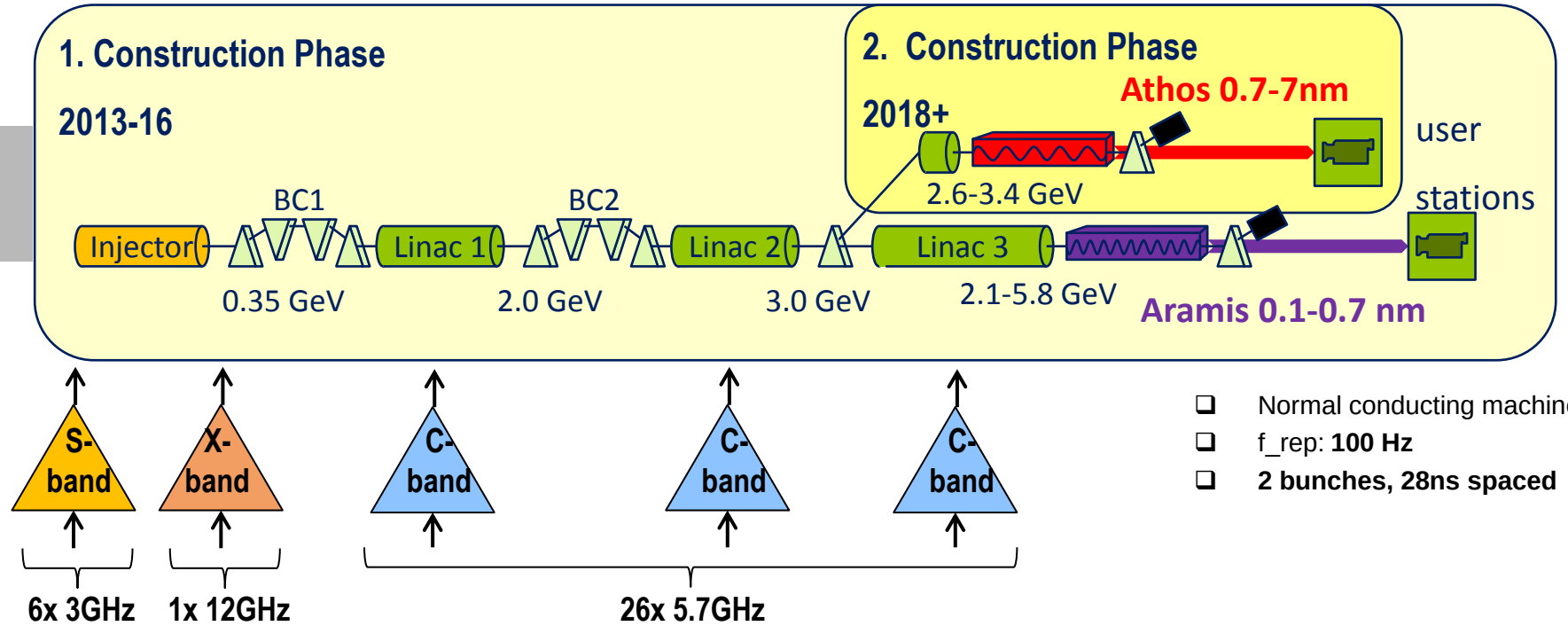
Roger Kalt on behalf of the LLRF team :: Paul Scherrer Institut

An overview of the SwissFEL LLRF system and its potential use in the SLS

17.11.2016 – 20th ESLS-RF Workshop

Content

1. Overview Machine+Stability Requirements



- Normal conducting machine
- f_rep: **100 Hz**
- **2 bunches, 28ns spaced**

SwissFEL performance calculations based on "expected performance" of RF stations [CDR]:

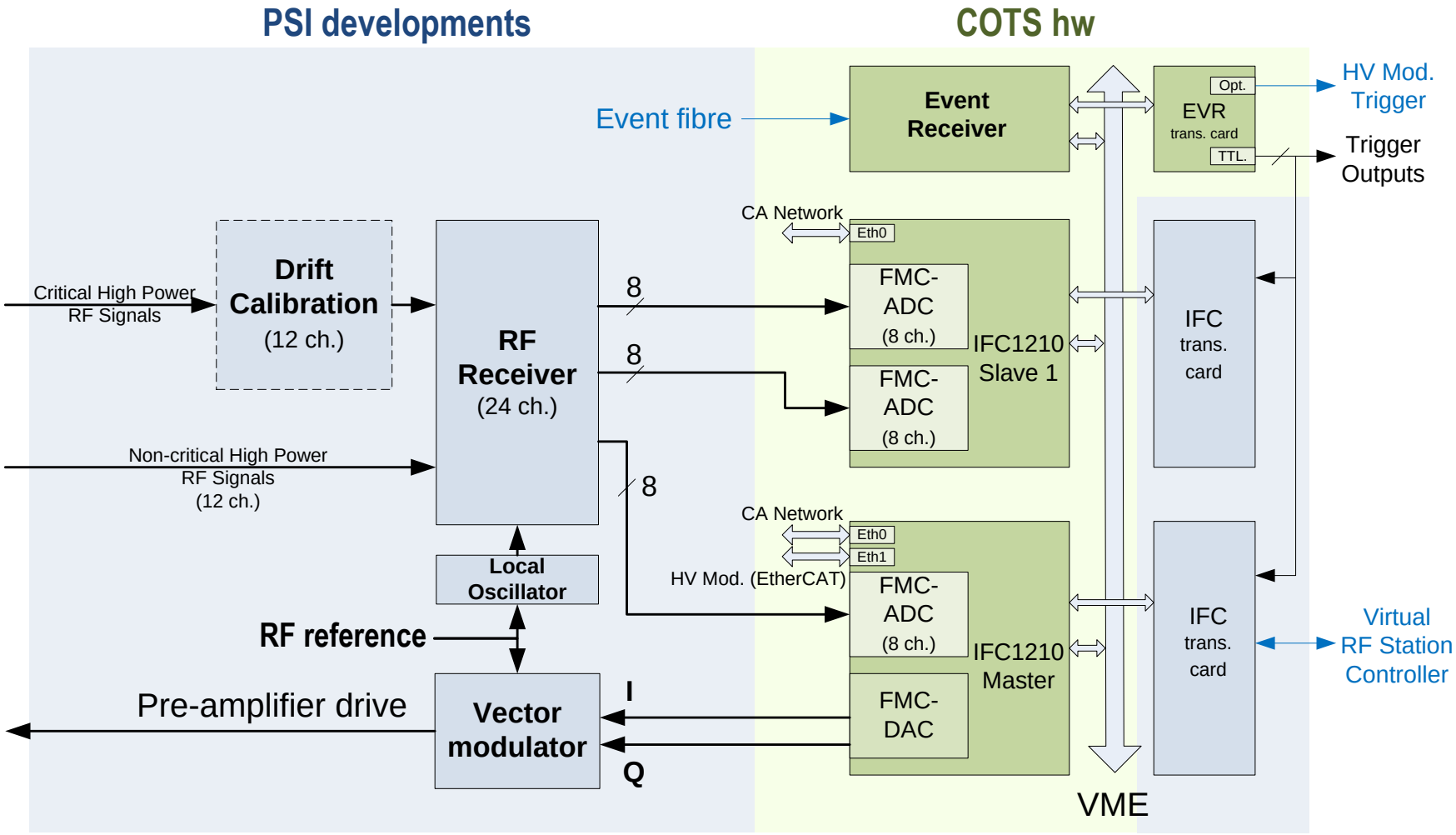
	Pulse-to-pulse stab.
S-band Phase*	0.018° rms
S-band Voltage*	1.8e-4 rms
X-band Phase	0.072° rms
X-band Voltage	1.8e-4 rms
C-band Phase	0.036° rms
C-band Voltage	1.8e-4 rms

LLRF requirements

LLRF actuator	stability
S-band Added Ph. Noise	0.009°
X-band Added Ph. Noise	0.038°
C-band Added Ph. Noise	0.017°
Amplitude (all bands)	1.6e-4

LLRF measurement	resolution
S-band Phase	0.007°
X-band Phase	0.02°
C-band Phase	0.01°
Amplitude (all bands)	1.0e-4

1. Overview LLRF Hardware Architecture

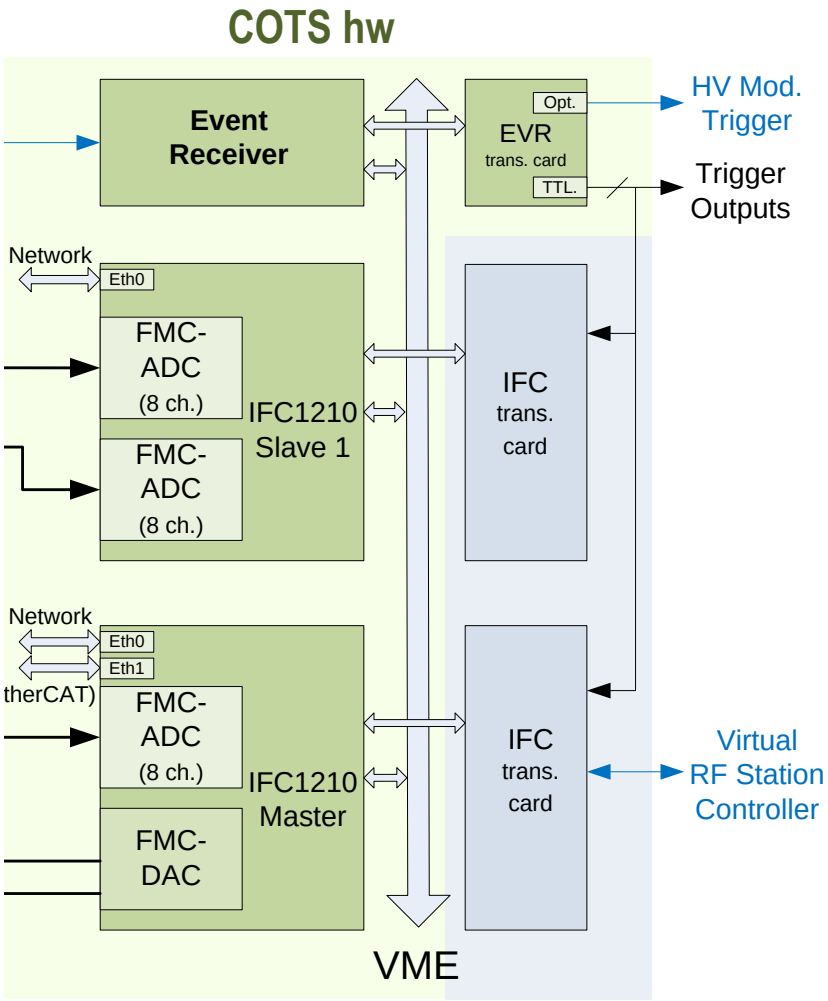


1. Overview LLRF Hardware Architecture Dig.

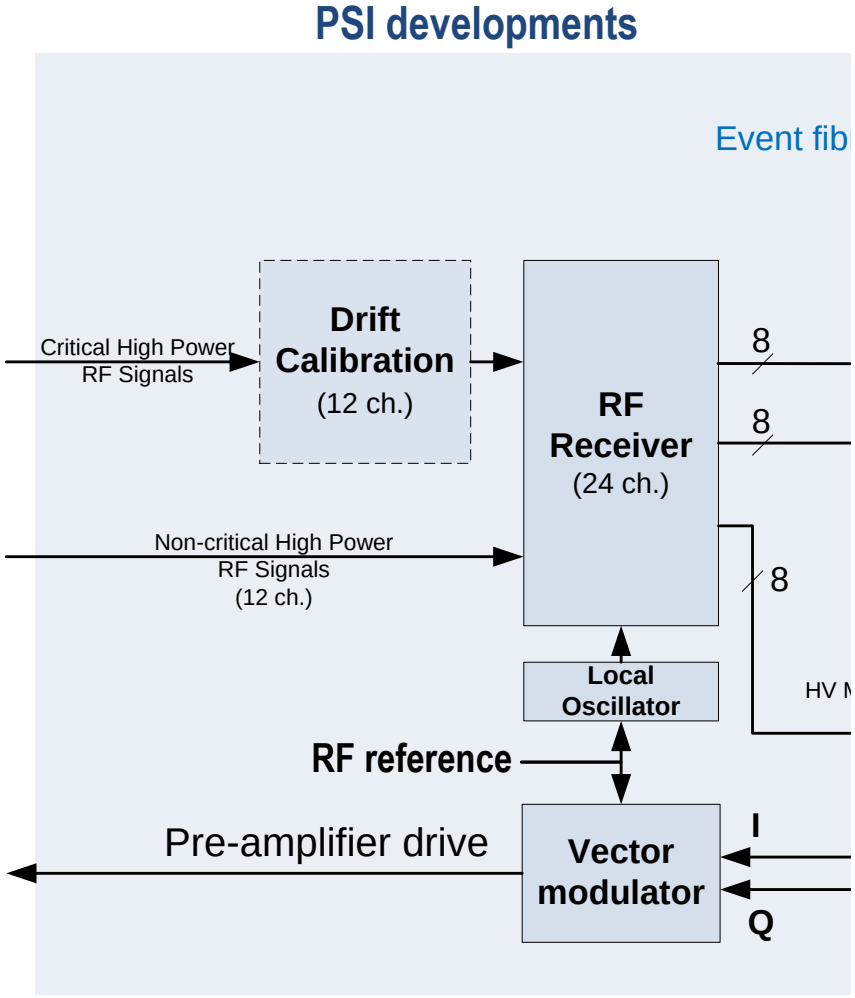
Basic Features:

- IF based digital system ~ 40 MHz
  - f_{IF}=41.65 MHz for injector
  - f_{IF}=39.67 MHz for linac
- commercial VME64x based FPGA/CPU processing board (PSI controls standard board)
- FMC based commercial ADC/DAC
  250 Msps / 16 bit
- 8µs data acquisition window / 250 Msps
  (defined in FPGA firmware and limited by FPGA on-chip SRAM)
- 100 Hz pulse-to-pulse RF feedback
- Vanilla Linux based operating system, EPICS on each processing board
- Custom designed digital interface transition card

➔ Hardware, Firmware and Software are independent of RF frequency



1. Overview LLRF Hardware Architecture Anlg.

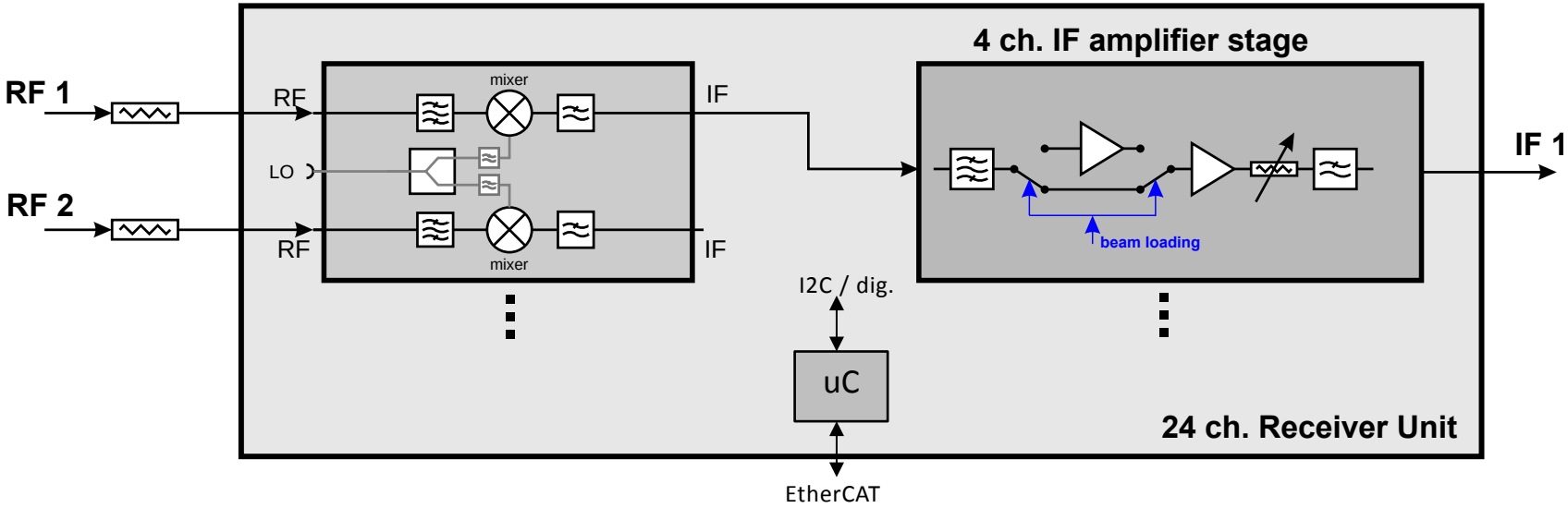


Basic Features:

- in-house developed RF front-ends for S- and C-band
  - 24 channel RF receiver
  - LO & clock generation
  - vector modulator / LLRF actuator
- CW low noise RF reference signal required
- Due to common IF around 40 MHz
  → some hardware components are the same for all bands.
- **postponed**: drift calibration unit

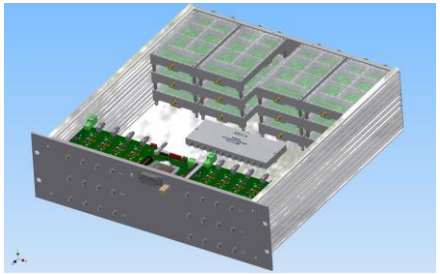
➔ Pizza box design which ensured performance and keeps flexibility / minimizes cost if RF frequency needs to be changed.

1. Overview LLRF receiver concept

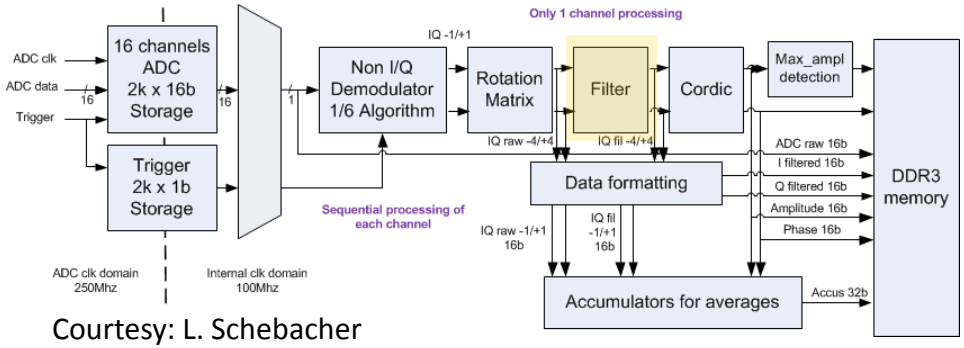


Basic Features:

- 24 equal receiver channels
- Dual channel down converter modules
- Internally I2C and digital / static control used
- IF gain PCB is common for S- and C-band
  - Controllable digital attenuator
    0 .. -7dB in 1 dB steps
  - +60dB pre amplifier for beam-loading measurements
- Control und status monitoring interface over EtherCAT fieldbus

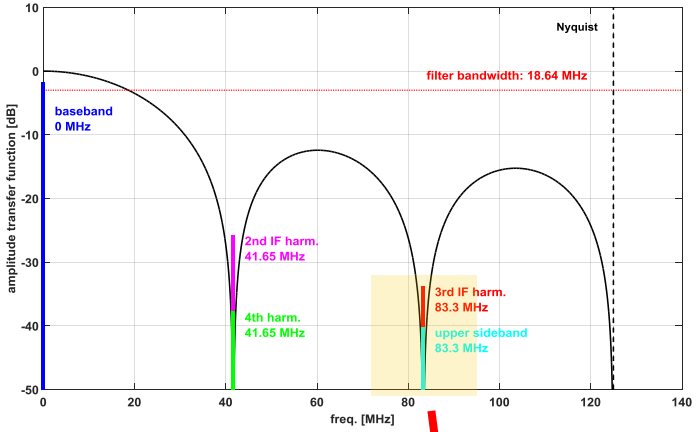


1. Overview non-IQ demodulation bandwidth



Courtesy: L. Schebacher

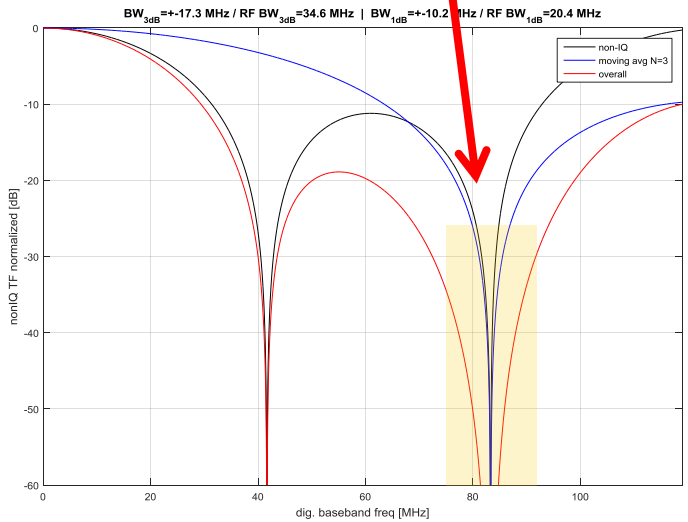
Fig: Non-IQ demodulation



1. Trigger based DAQ 8µs duration
   S-band: sampling 249.90 Msps

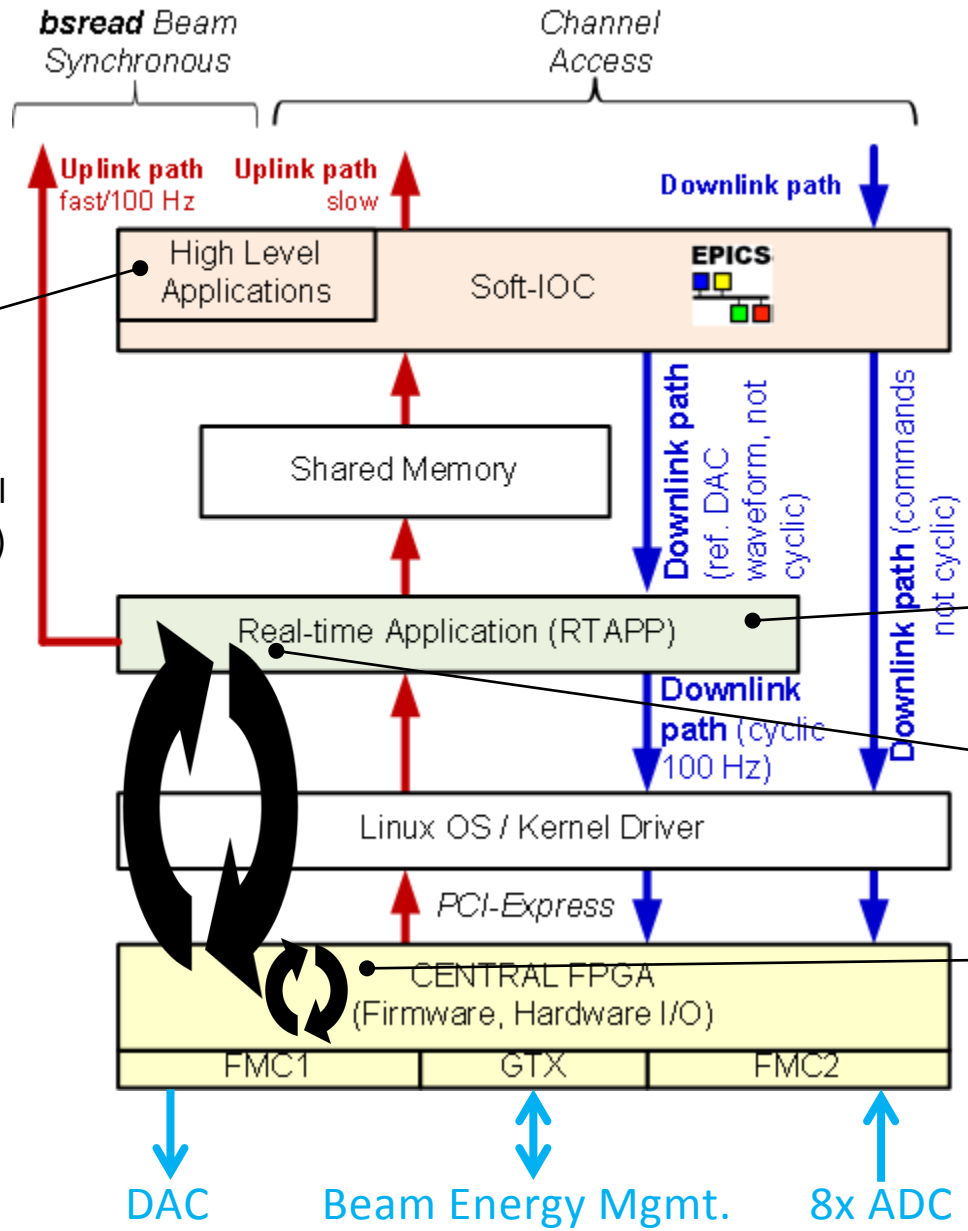
2. Sequential FPGA controller for data pre-processing (~ 350 µs)
3. Non-IQ demodulation 1/6 Bandwidth 37.2 MHz
4. Additional FPGA filtering to remove upper sideband of IF
   → **New Bandwidth 34.6 MHz**
5. IRQ over PCIe to CPU

Fig: Additional FIR filtering



1. Overview LLRF DAQ + Feedback on 1 Slide

34x
for each RF Station



RF station local automations

- Start/stop procedures
- Iterative Learning Control (ILC, e.g. flatten RF pulse)
- Various slow algorithms
  - RF pulse setup
  - Measure klystron
  - IQM imbalance corr.
  - Cavity detuning calc.

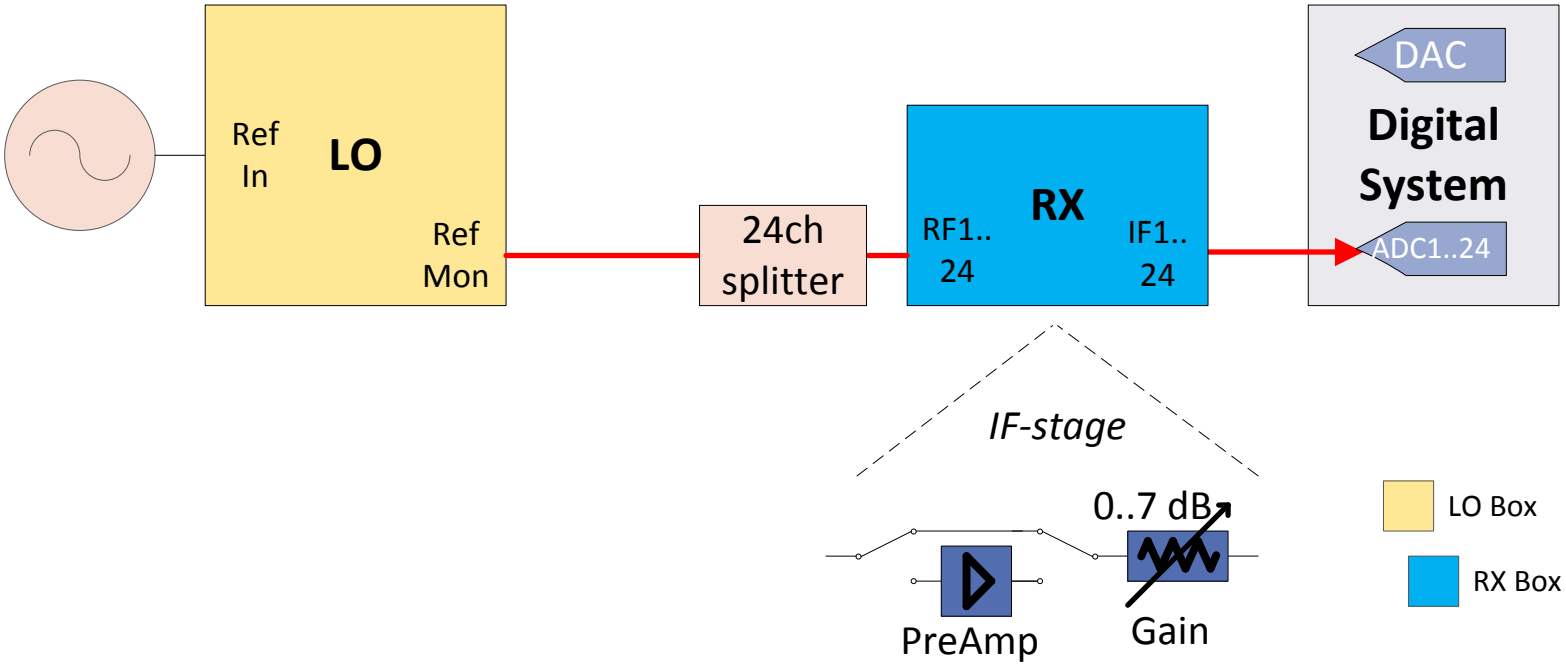
100 Hz data processing and statistics

100 Hz pulse-to-pulse feedback on vector-sum

- OPD: klystron set-point calculation
- FPGA alternative

2. Performance Measurements

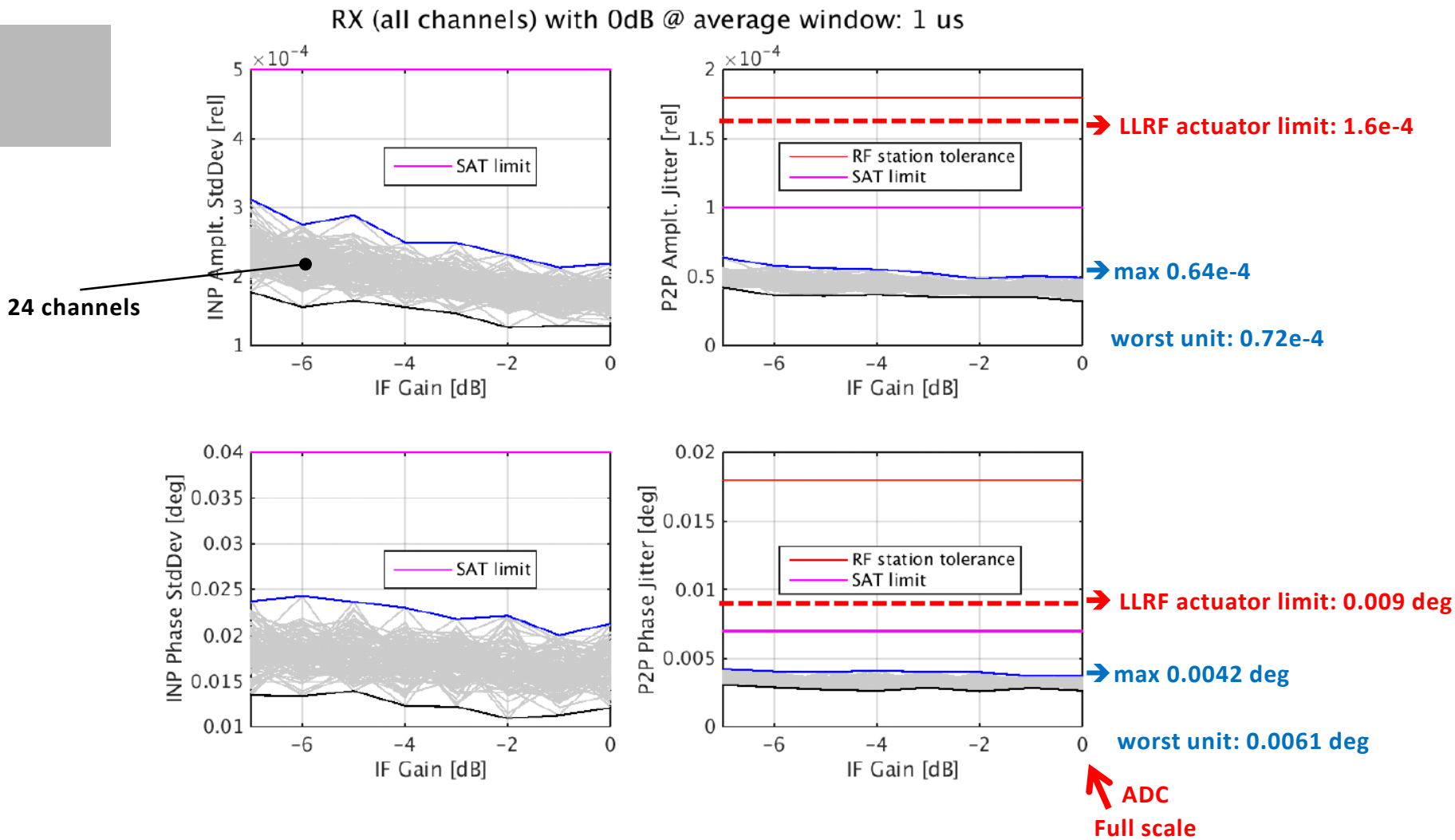
2. Performance Setup for Measurement System



Courtesy: F. Gärtner

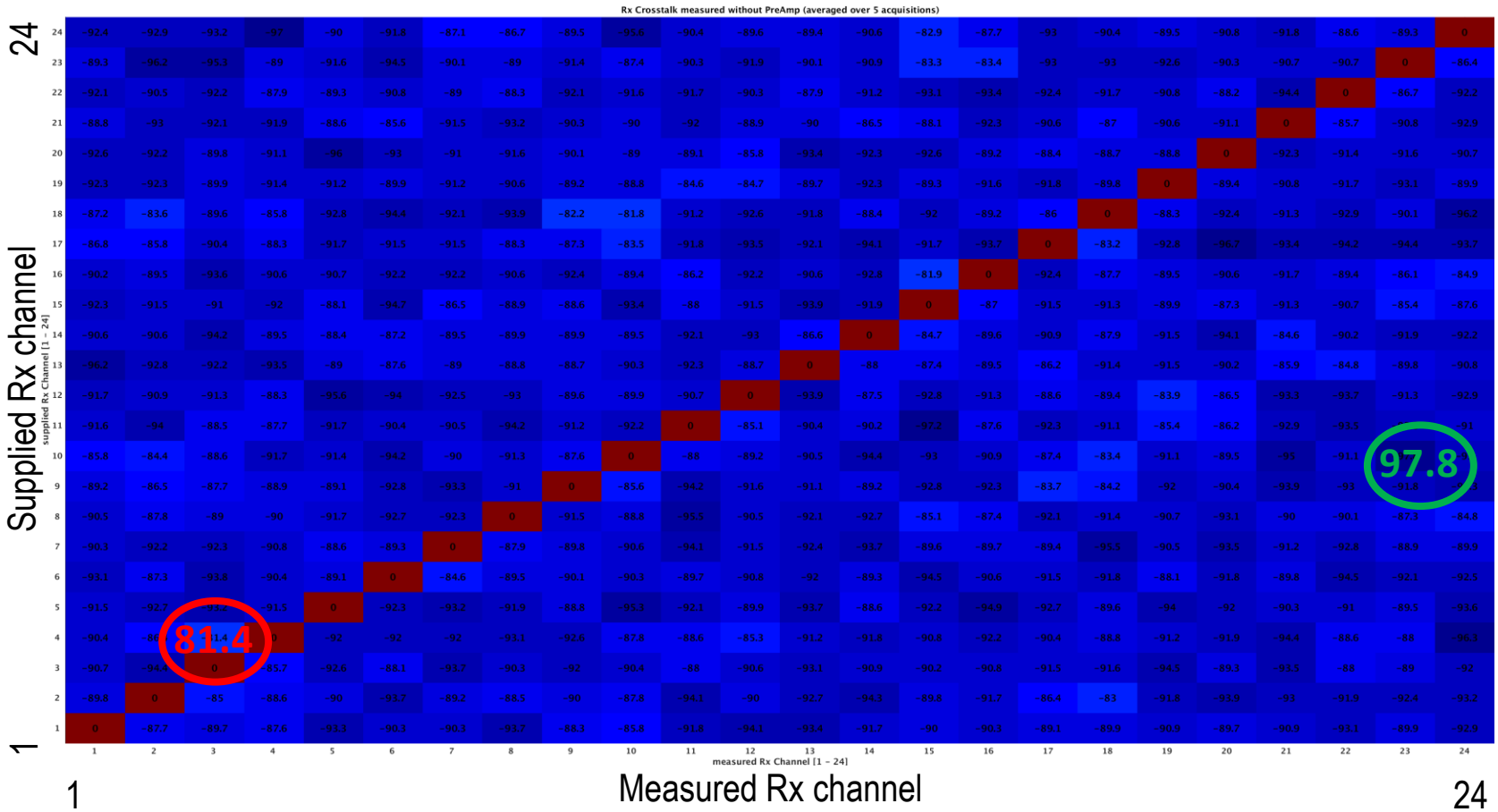
2. Performance LLRF Rx Perf. (S-band)

INP = Intra Pulse **Pulse-to-Pulse 100 Hz / 100 Pulses**



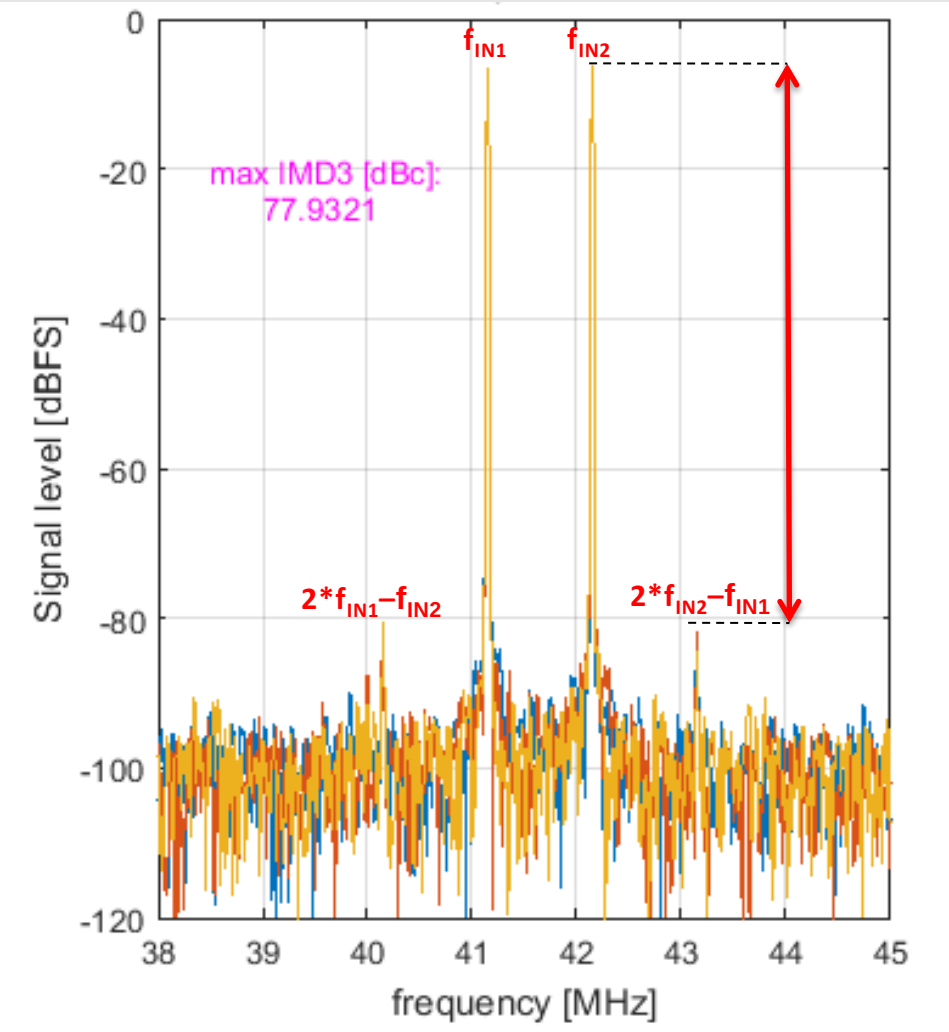
Courtesy: F. Gärtner, Series Charac. [3], LO0086, RX0200

2. Performance Rx Crosstalk



Parameters	S-band series [3]	S-band prototype [1]
Crosstalk [dB]	> 80	> 70

2. Performance Rx Intermodulation Distort.



Two-Tone Intermodulation distortion 2nd & 3rd order

Parameters	S-band series [3]
IMD2 *[dBc]**	**> 65**
IMD3 *[dBc]**	**> 70**

* @$P_{IF\ OUT}$ = 5dBm

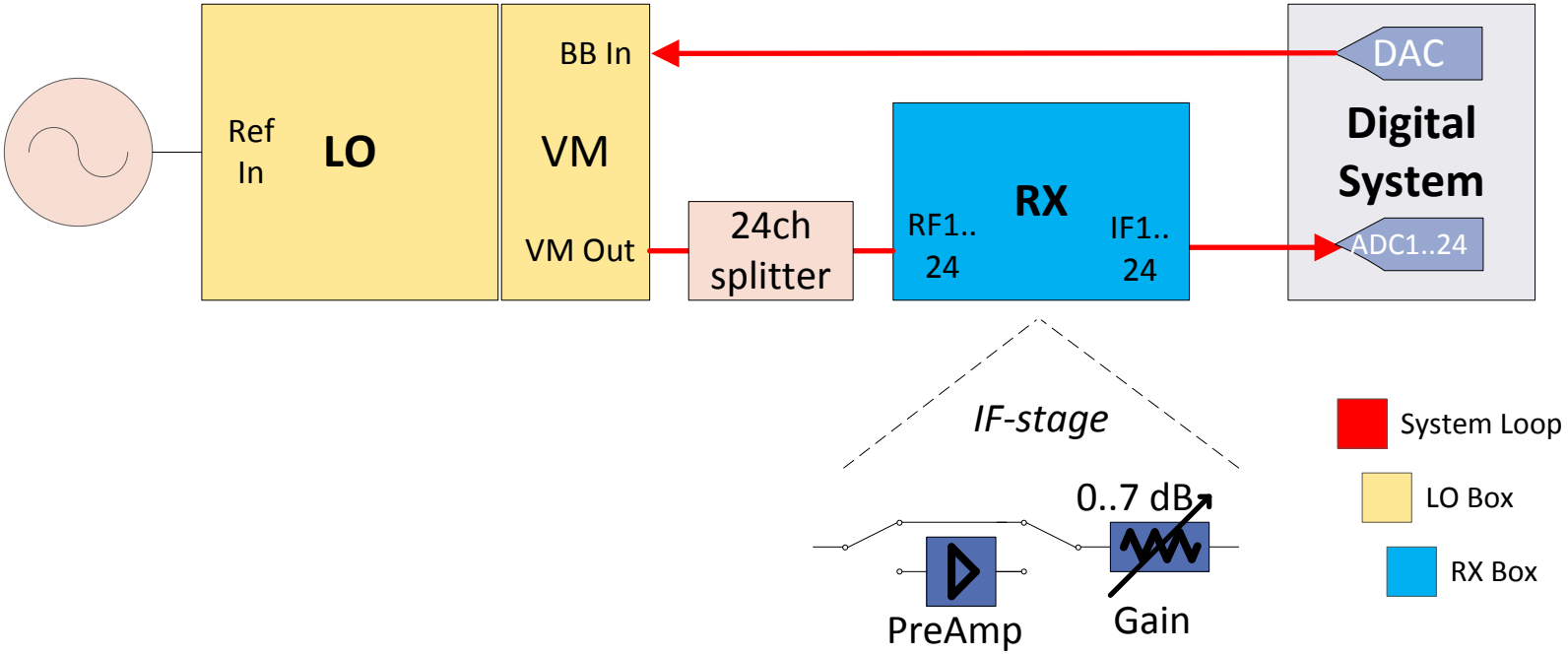
$$OIP_3 = P_{OUT} + \frac{IMD_3}{2} =$$

$$OIP_3 = -7\ \text{dBFS} + \frac{75\ \text{dB}}{2} =$$

$$OIP_3 = 5\ \text{dBm} + 37.5\ \text{dB} =$$

$$OIP_3 = 42.5\ \text{dBm}$$

2. Performance Setup for System Loop

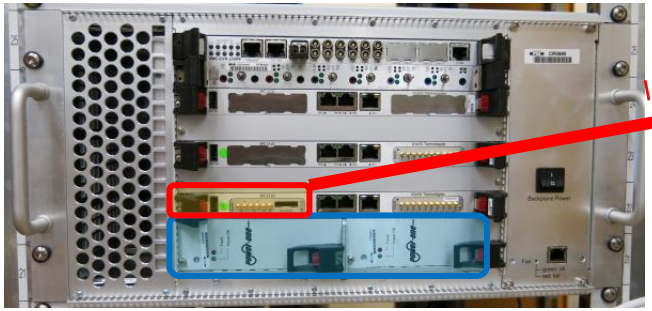


Courtesy: F. Gärtner

2. Performance System Loop Improvement

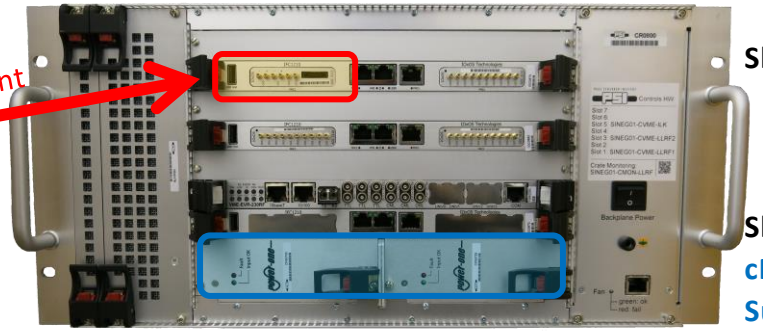
Standard Controls 7-Slot VME Crate from Trenew, ~ 2kCHF

DAC @ Slot 1



Improvement

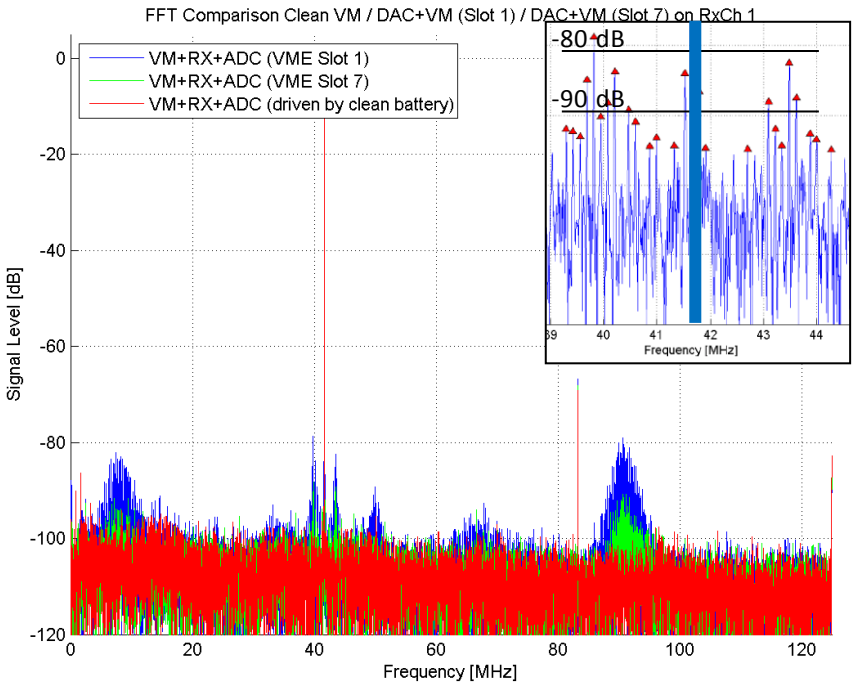
DAC @ Slot 6,7

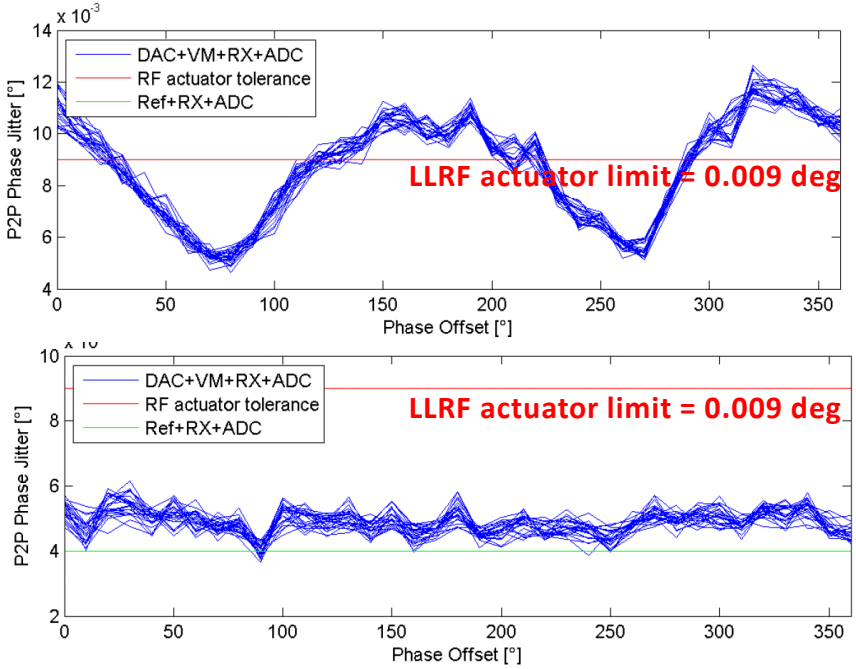


Slot 7

Slot 1

cPCI Power Supply





Improvement

Courtesy: F. Gärtner, S-band PreSeries VM Jitter Analysis [2]

3. Summary & Outlook

3. Summary Conclusion SwissFEL LLRF

- The LLRF basic system fulfills the defined RF stability requirements (1µs gate)

LLRF actuator	Stability required	Stability measured (worst)
S-band Phase	0.009° (added)	0.009° (absolute)
Amplitude	1.6e-4	1.2e-4

LLRF measurement	Resolution required	Resolution measured (worst)
S-band Phase	0.007°	0.0061°
Amplitude	1.0e-4	0.72e-4

- Robust system design which is able to run 24/7/365
- Able to provide real time beam synchronous waveform data for each ADC ch.

- **Possible future improvements are:**
  - Reduce influence of standard switching cPCI power supplies
  - Extend fw/sw and add more algorithms for data preprocessing to FPGA and CPU to provide real-time data analysis
  - If required, replace FMC cards with new ADC/DAC chips with better parameters

3. Summary SLS Linac LLRF Upgrade Outlook

Parameter	Spec. SwissFEL	Spec. SLS	Comment
RF frequency	2.9988 GHz	2.99782 GHz 500 MHz	TW: match Buncher: TBD
Operation mode	100 Hz pulsed	3 Hz pulsed	Match
DAQ pulse length	up to 8µs	4.5µs	Match
RF Station tolerances	Amplt: 1.8e-4 Phase: 0.018 deg	Amplt: 2.0e-4 Phase: 1.0 deg	Match, also measurement sys.
No. of ADC ch.	24	~ 12	Match, scalable
RF frontend	2.99712 GHz for test facility, hw available	2.99782 GHz	Match, various options for auxiliary channels
RF reference input	2.99712 / 2.9988 GHz CW	2.99782 GHz CW	SLS provides pulsed RF ref. signal → upgrade
System Integration	EPICS	EPICS	adaption required

3. Summary SLS BO/SR LLRF Upgrade Outlook

Parameter	Spec. SwissFEL	Spec. SLS	Comment
Digital backend	IF ~40 MHz FPGA/CPU FMC ADC/DAC	TBD FPGA/CPU FMC ADC/DAC	Match, part of infrastructure can be re-used
No. of ADC ch.	24	~ 12	Match, scalable
RF frequency	2.9988 GHz	~ 500 MHz ?	Adaption required
Operation mode	100 Hz pulsed	CW	Firmware adaption required
RF frontend	2.9988 GHz	500 MHz	New frontend required
Tuning Loop	Not included	Required	Required, can profit from already used EtherCAT
System Integration	EPICS	EPICS	Adaption required

3. Summary SLS LLRF Upgrade Outlook

- The projects can be separated into:
  - Linac
  - BO+SR
- We can profit from already built-up hardware, firmware, software and knowledge from
  - SwissFEL from the COTS hardware and fw/sw infrastructure
  - HIPA proton accelerator from the CW operation mode firmware, feedback and tuning loops
- There is no 1:1 drop-in replacement.

My thanks go to

- LLRF team
- Lukas Stingelin for information about SLS RF/LLRF plants

References

[1] System Characterization Report S-Band PreSeries System, (Publication date 17-Jul-2015 18:17:51)

[2] FEL-S-Band-VM-Jitter, S-Band PreSeries Vectormodulator jitter analysis, 31.7.2015

[3] System Acceptance Test Report S-Band Series System, (9x series systems, Nov. 2015 – Feb. 2016)

[CDR] SwissFEL Conceptual Design Report, V20, April 2012