PAUL SCHERRER INSTITUT

PSI

Martin Brückner :: Paul Scherrer Institut

Data Processing in the Detector and Data Transfer to the Backend

New concepts in ultra fast data acquisition

10-11 April 2018

Outline

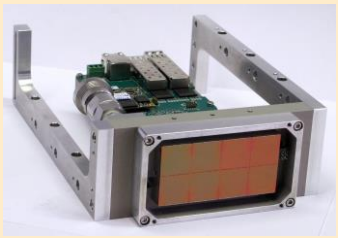
Transmission

Detector

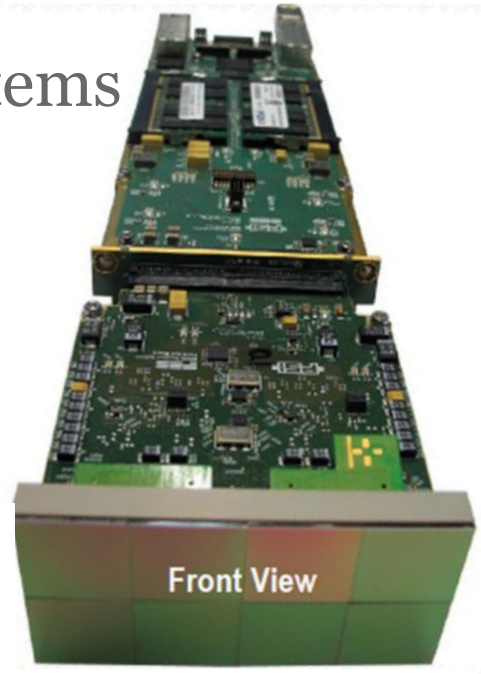
Receiver/Backend

- Eiger and Jungfrau as Examples for Modular Detectors
- Online Processing Onboard (Detector)
  - Online Compression
- Transmitting Data
  - Round Robin in Eiger
  - Module and Frame Delay
- FPGA based Network Card (Receiver/Backend)

Eiger and Jungfrau Detector

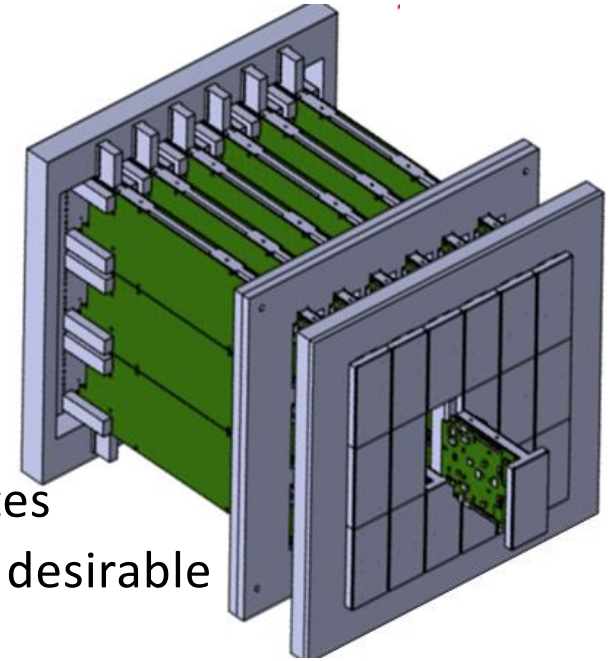
	Eiger	Jungfrau
		
Type	Single photon counting Modular design	Charge integrating Modular design
Pixel size	75 x 75 µm²	75 x 75 µm²
Dynamic range	4bit/8bit/12bit (32bit)	3 gain stages
Maximum frame rate	23 kHz (4 bit) burst 10 kHz (4 bit) continuous	2.4 kHz continuous
Maximum data rate per module	2x 10 Gbit/s (internal: 2x 23 Gbit/s)	2x 10 Gbit/s
Pixel per module	512 kPixel	512 kPixel

Eiger and Jungfrau Readout Systems



- Module based detectors
  - Independent data taking
  - Parallel data sending
  - Larger detectors with more modules mean higher data rates with the same frame rate
  - Simple module based data processing can be applied

	Eiger	Jungfrau
Fastest detectors	9 MPixel 18 modules 360 Gbit/s	10 MPixel 20 modules 400 Gbit/s



➔ Simple to build large detectors with huge data rates

➔ Onboard data processing and smart data transfer desirable

Onboard Data Processing

Eiger and Jungfrau Data Processing

- Descrambling
- UDP network packet generation
- **Round Robin** (frame transmitting to several servers consecutively)

Eiger Data Processing

- Rate Correction (counting problem if 2 photons arrive too close)
- Data buffering (2000-8000 images)
- Image summation
- Under development: Simple **online compression** (count contiguous zeros)

Jungfrau Data Processing

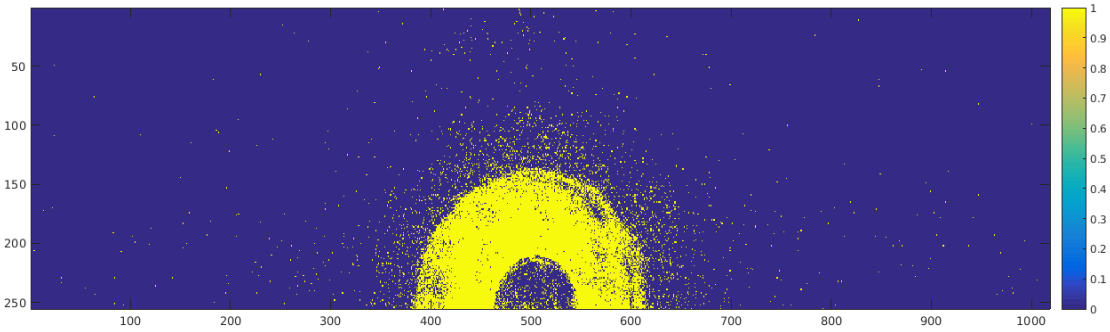
- Planned: Count number of pixels of each gain state

Eiger Onboard Compression

To reduce network traffic or to widen the 20Gbit/s bottleneck
an online compression is being developed

Bit Mode	Max Frame Rate [kHz]	Continous max Frame Rate [kHz]	Factor
4	22	10	2.2
8	11	5	2.2
12/16	6	2.5	2.4

Eiger is limited by its two 10 Gbit/s Ethernet ports by a factor of about 2.2-2.4



Typical ptychography image

a lot of zeros and nice to compress
Usual case: compress ratio > 4

Yellow Pixel ≠ 0

Blue = 0

Eiger on Board Compression

A simple zero suppression algorithm:

- Token FF + Zero Counter
  - 00 → 00
  - 00 00 → FF 02
  - 00 00 00 → FF 03
  - 00 ... 00 → FF FF 00

  - FF → FF 00 (Token masked as “0 Zeros”)

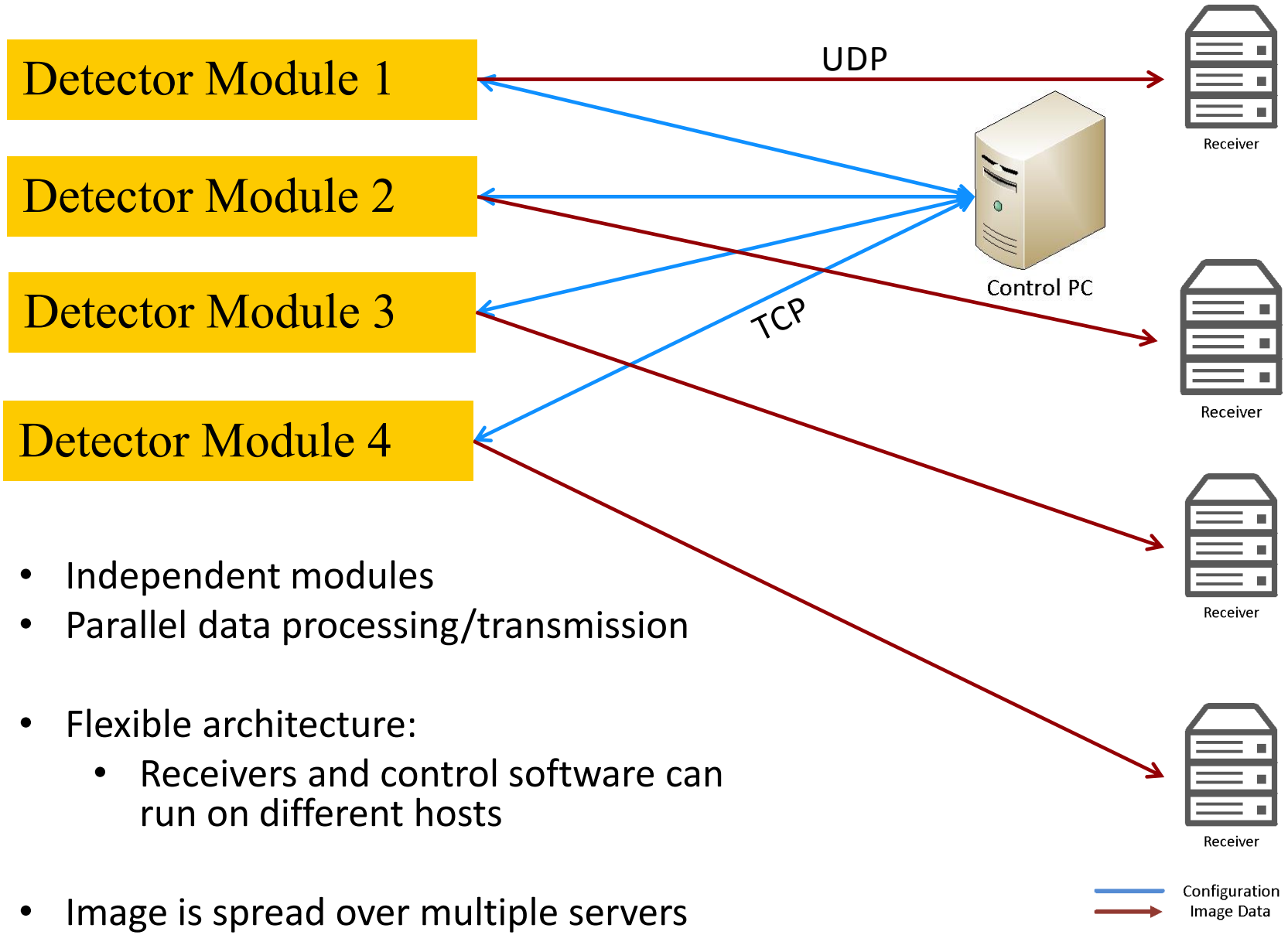
Best case: Image with all zeros

Worst case: Image with a lot of 254 (0xFF)

Non-standard compression
decompressing on receiver necessary

→ Network data rate can be reduced by a factor of 4 or more

Data Transfer to Receivers

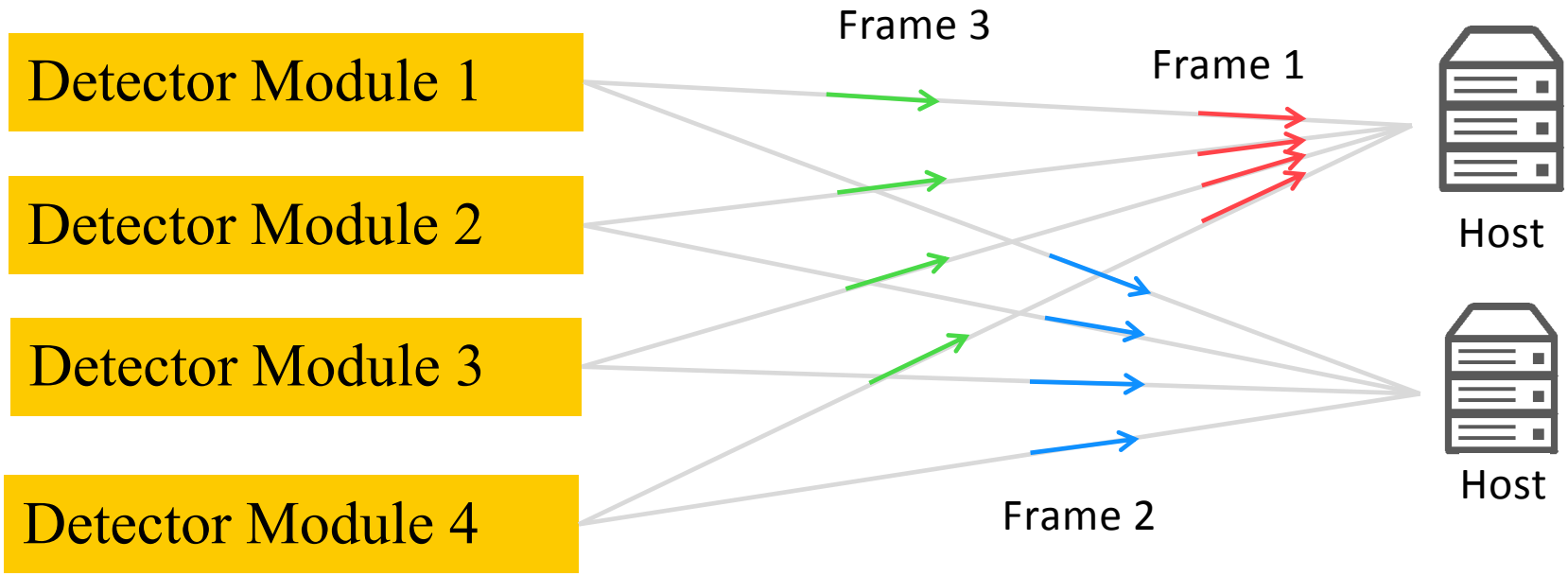


- Independent modules
- Parallel data processing/transmission

- Flexible architecture:
  - Receivers and control software can run on different hosts

- Image is spread over multiple servers

Round Robin

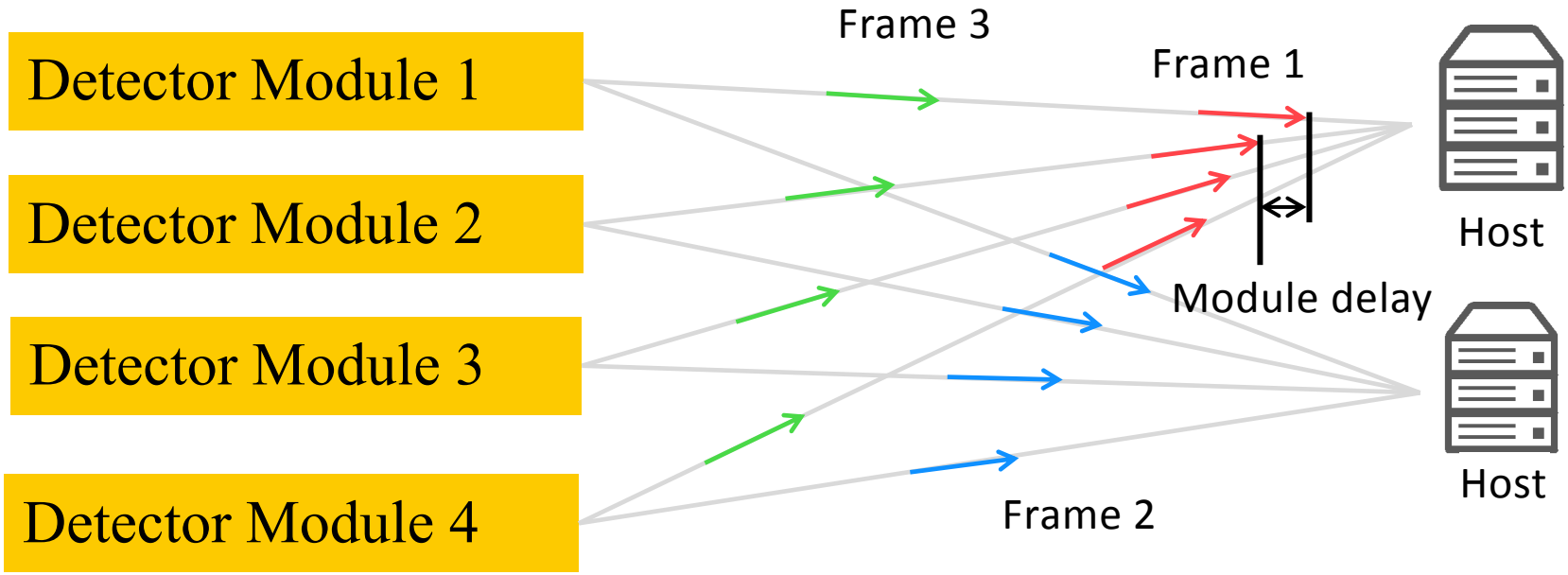


Round Robin

- One server can hardly handle big multi module detectors
- Therefore several destination headers can be stored in the FPGA

- Data from all modules arrive at the same time

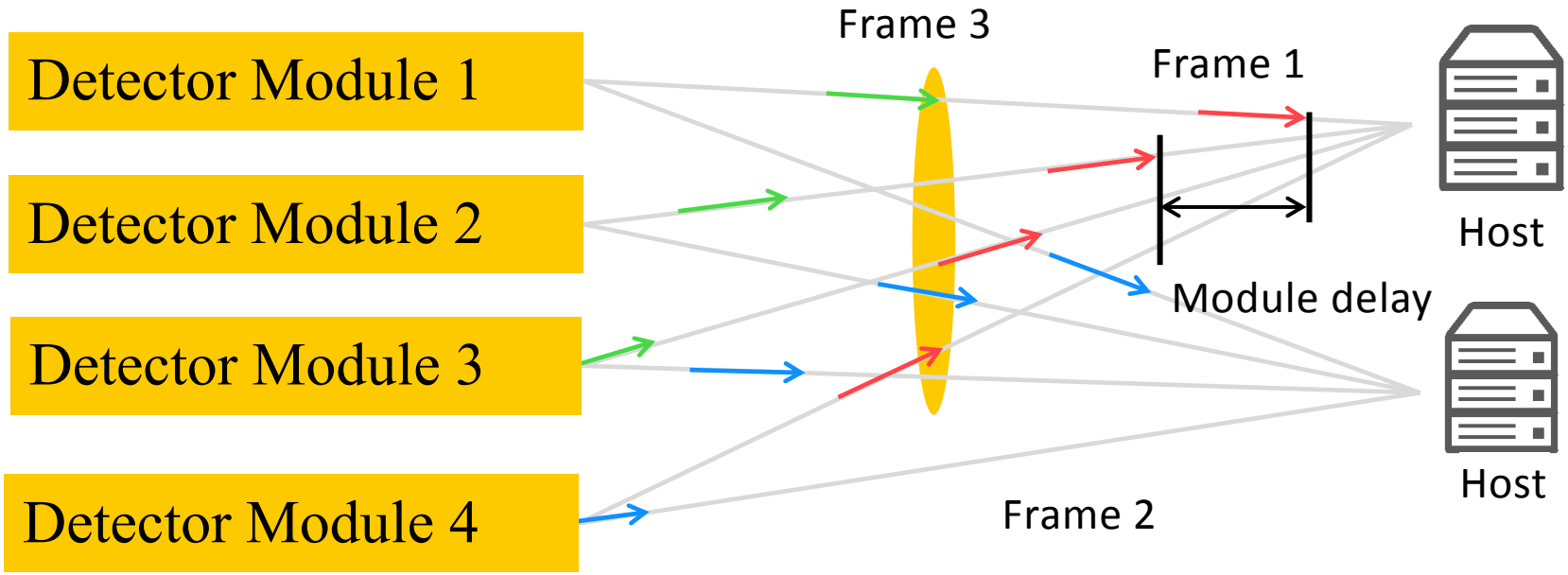
Round Robin with Module Delay



Individual module delay

- Time after a frame has been acquired before sending it
- Avoids load peaks on receiver side

Round Robin with Module Delay

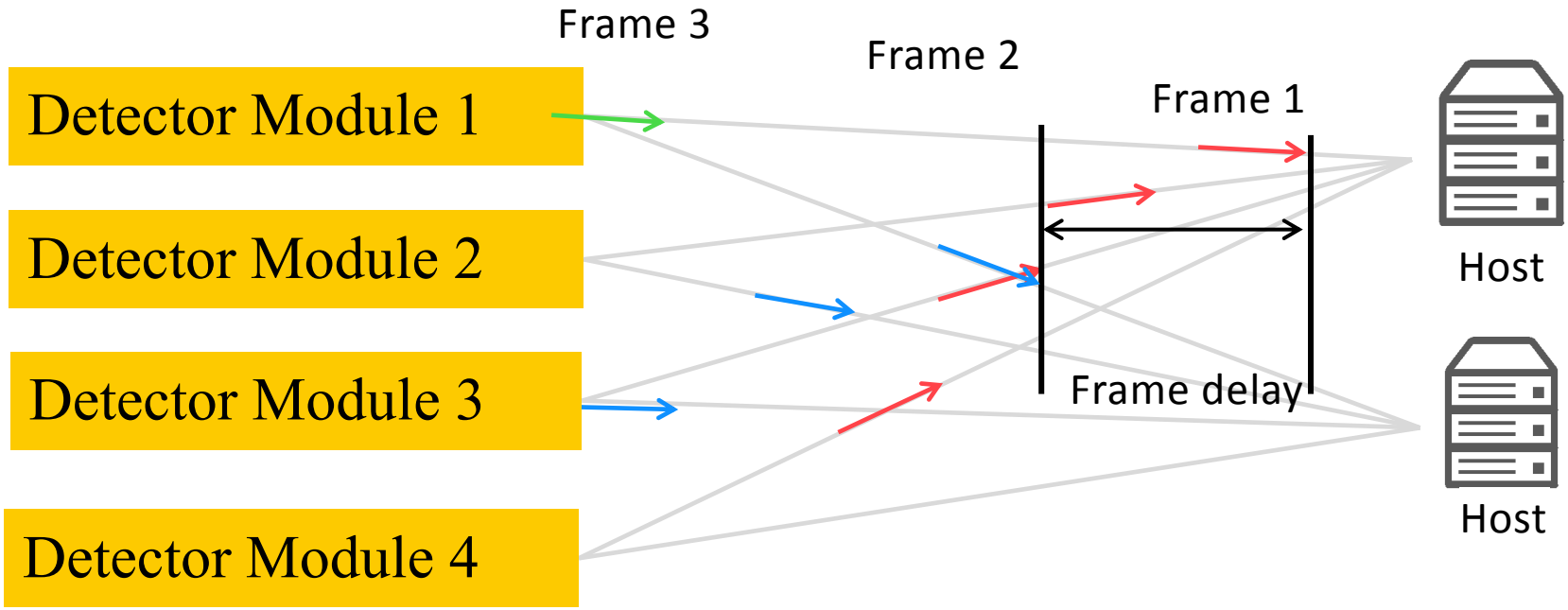


Individual module delay

- Time after a frame has been acquired before sending it
- Avoids load peaks on receiver side

- Limit: Delaying more than the frame rate per receiver

Round Robin with Module+Frame Delay



Frame delay

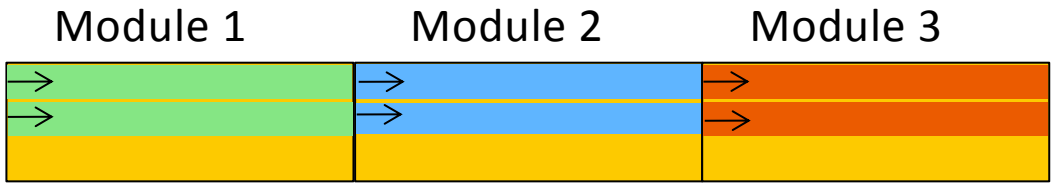
- Time between sending 2 frames
- Decelerate sending of high frame rate acquisitions
- No continuous data taking possible anymore
  (frames are buffered in the detector)

- Better option: Unload CPU from receiving network packets and assembling images

FPGA Based Network Card

- PSI detectors send UDP packets
- Normal reception
  - Host receives packets in a random order
  - Several memcopy operations
  - Packet inspection/sorting to reassemble the images
  - 1 address per line per module

Packet Header				
Frame Number (8 Bytes)				
Exposure Time (4 Bytes)		**Packet Number (4 Bytes)**		
Bunch ID (for FELs)				
Mod ID	X	Y	Z	
Debug		Server (RR)	DT	HV



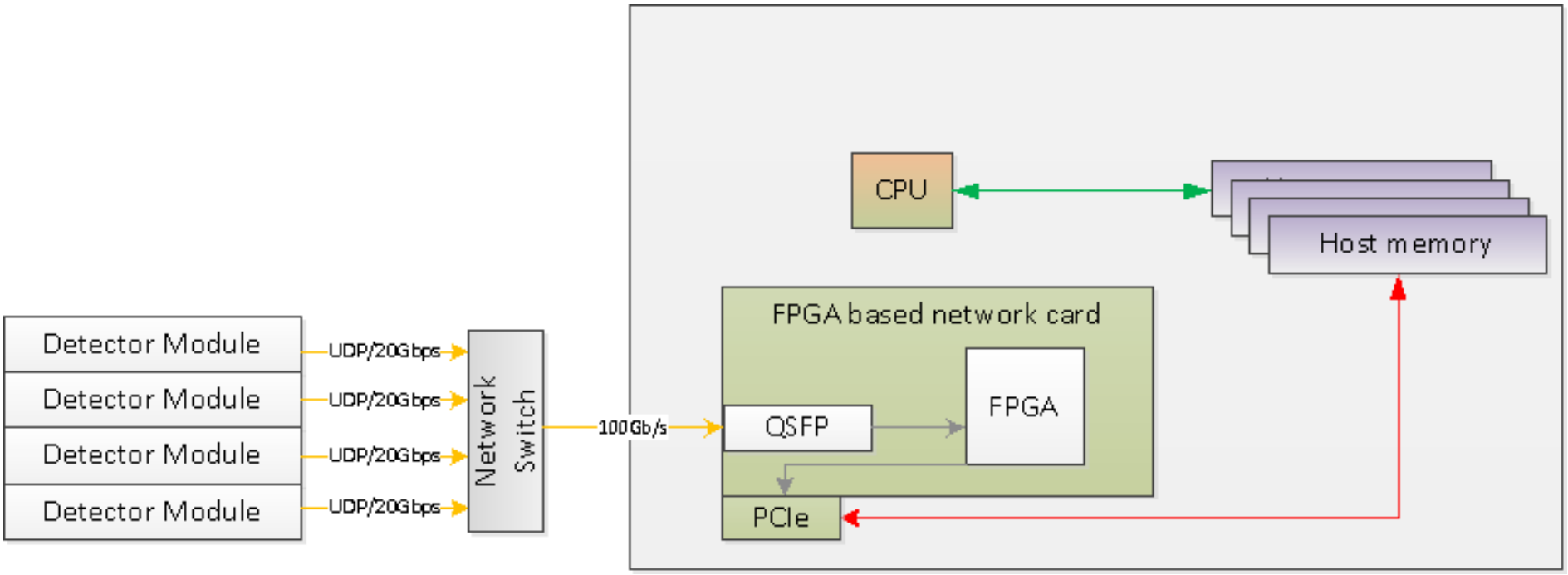
4 Bit/Pixel	8 Bit/Pixel	16 Bit/Pixel	32 Bit/Pixel
16 lines/packet	8 lines/packet	4 lines/packet	2 lines/packet

→ Keeps the CPU busy

→ Realizable on an FPGA

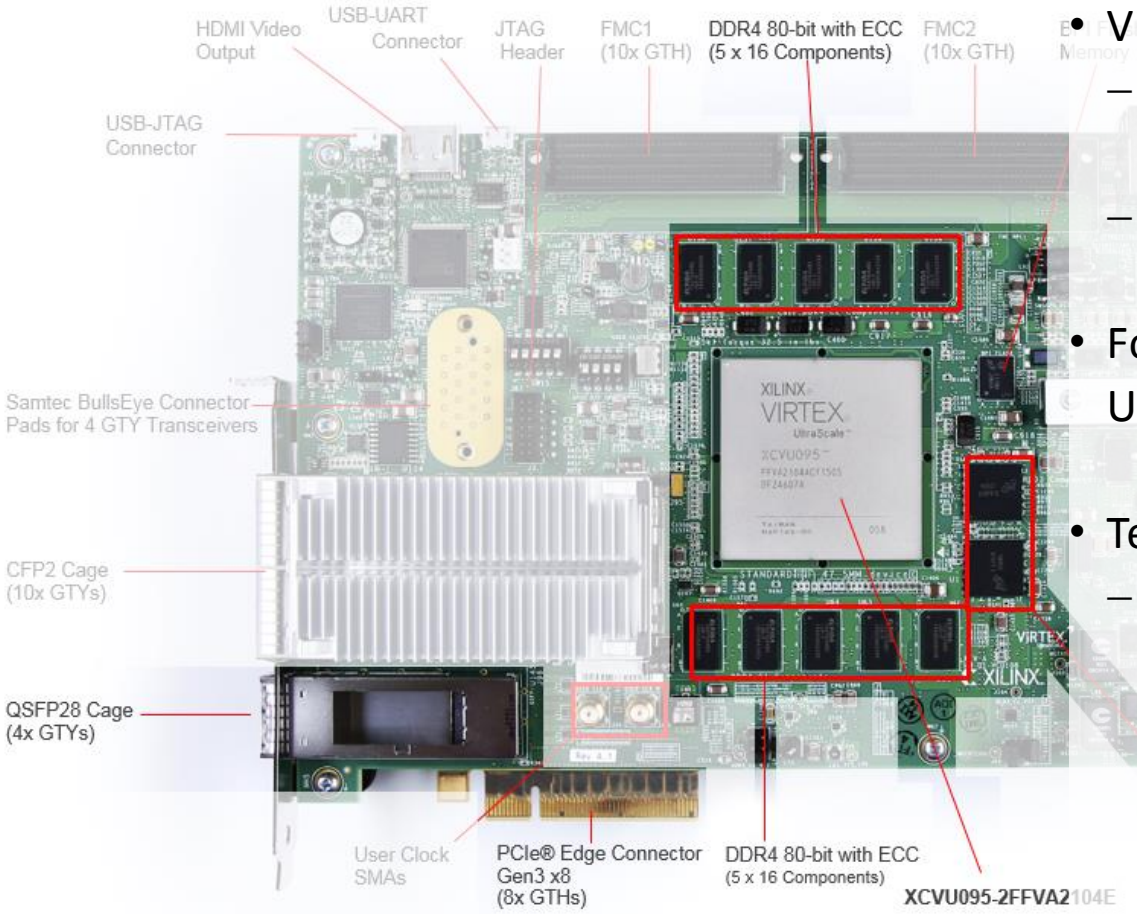
FPGA Based Network Card

- FPGA based network card
  - Can analyze packet headers and assemble images in host memory
  - Writes a proper image header for each image and discards packet headers
  - CPU receives a pointer to the final image



FPGA Based Network Card

Xilinx VCU108 Evaluation Board

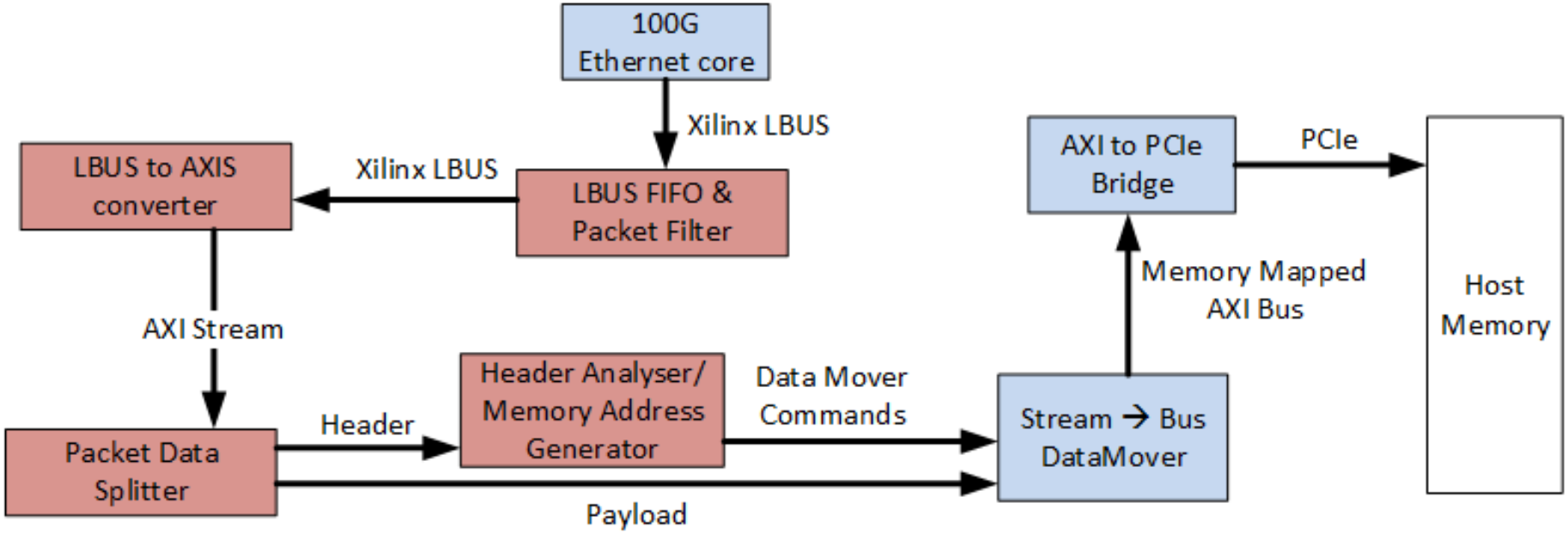


- Used for evaluation
- Virtex Ultrascale Hard IP cores
  - 100Gbit/s Ethernet but no RS-FEC, no 40Gbit/s nor 10Gbit/s
  - 8xPCIe 3.0 (64Gbit/s only)
- For new design better use a Ultrascale+ with FEC and 16xPCIe
- Test setup:
  - Eval board plugged into PCIe slot and connected via fiber with a Mellanox 100Gbit/s card (same PC)

FPGA Based Network Card

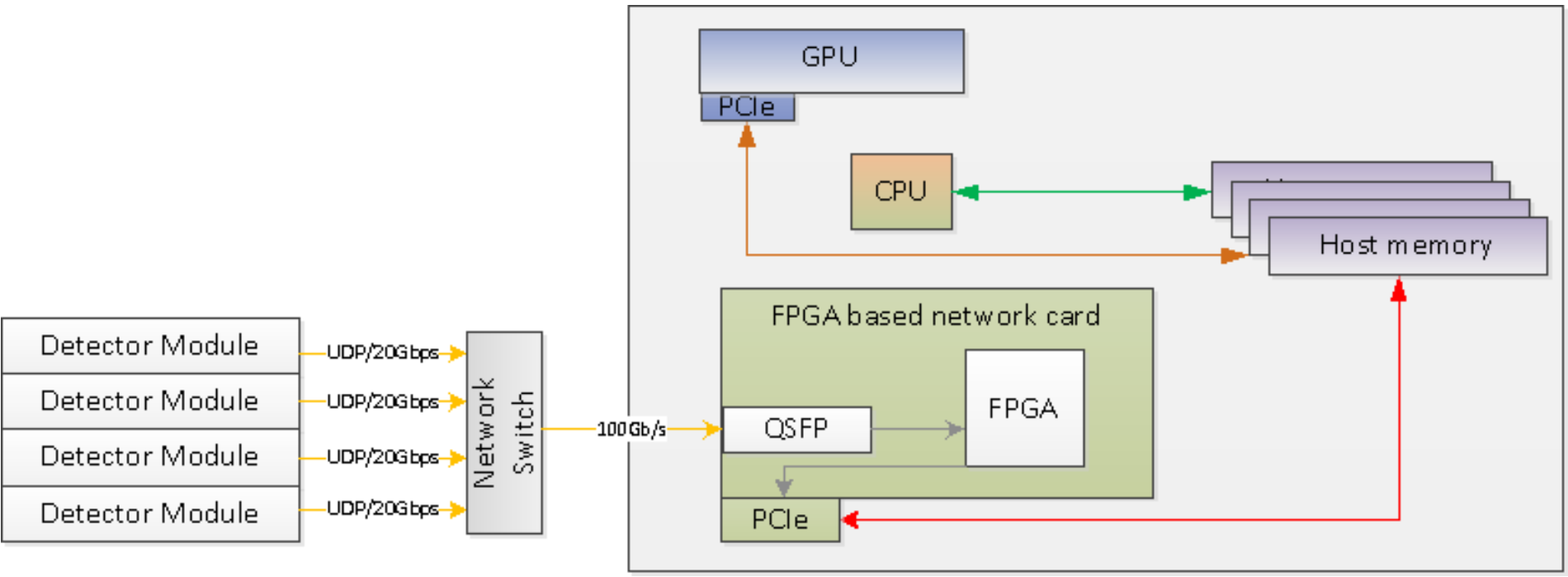
FPGA design:

- *Packet Filter* acts like a firewall
- *Packet Data Splitter* splits packet header from packet payload
- *Header analyser* generates the destination memory address from packet header
- *Xilinx DataMover* copies payload to given memory address
- *Xilinx AXI to PCIe Bridge* is a transparent bridge to host PC address space
- Future: Decompress proprietary detector compression



FPGA Based Network Card

- Future:
  - FPGA based network card copies data directly into GPU memory
  - GPU for advanced image processing (see Carlos' talk)



Conclusion

- Eiger and Jungfrau are modular detectors
  - Large detectors can be built up easily
  - Independent read out systems
  - Large detectors produce high data rates (360Gbit/s Eiger 9M, 400Gbit/s Jungfrau 10M)

- Eiger onboard data processing
  - Online compression to shrink network data rates by a factor of 4 or more

- Transmitting data
  - Round Robin spreads the load (and not the frames) to several receivers
    - Module and frame delay can further adjust the servers' load

- FPGA based network card
  - Offloads CPU with reassembling the detectors image in the FPGA and host memory