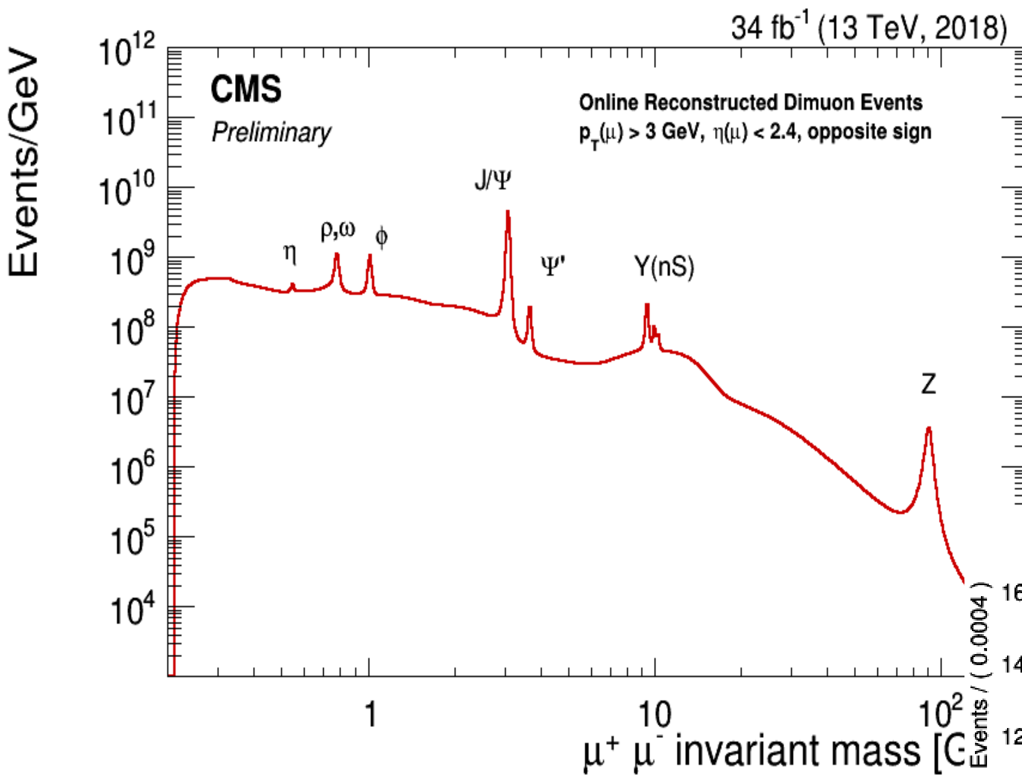
CMS Pixel Detector
Phase-1 upgrade, status & plans
Danek Kotlinski
PSI 29/10/2018

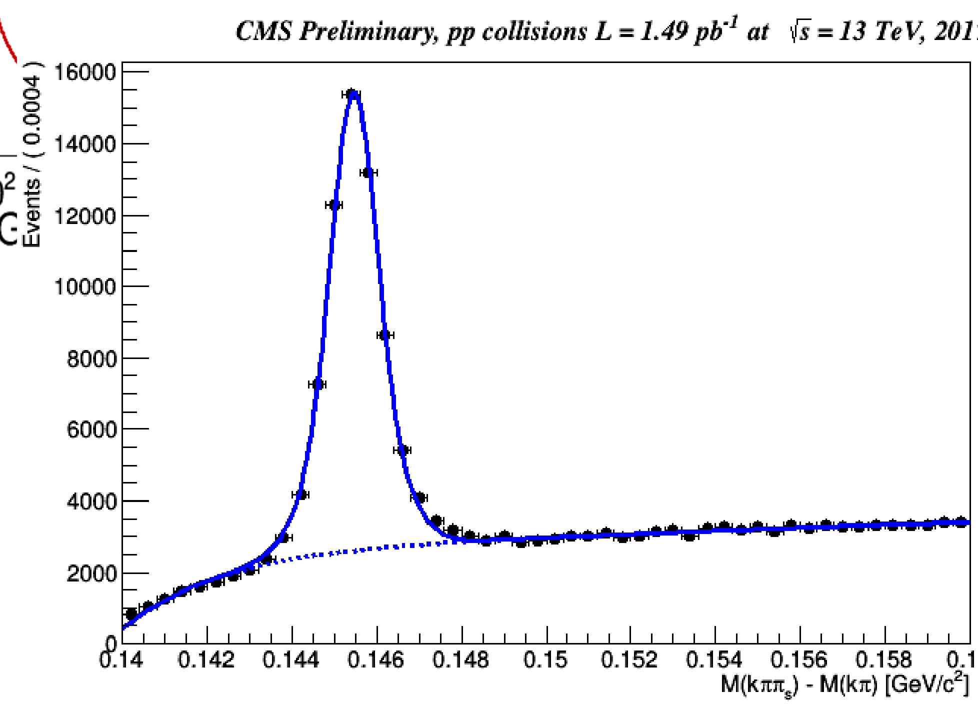
Disclaimer/Warning:

Some of you might have heard rumors/comments about the problems that we faced with the phase-1 pixel detector.
I will be honest and describe all problems that we had but please do not get a wrong impression.
The detector has worked very well, as illustrated in the next few slides.

CMS - Run2



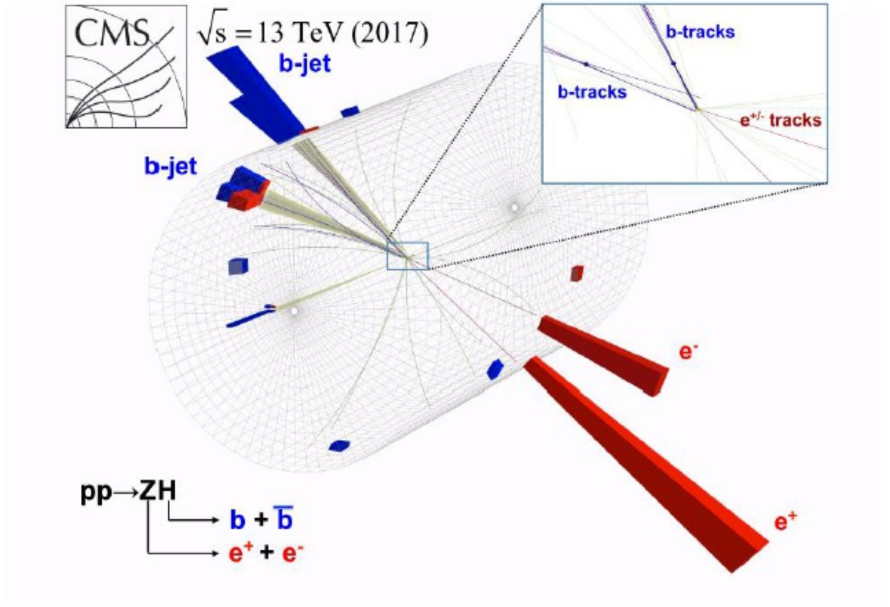
Dimuon mass spectrum at the trigger level



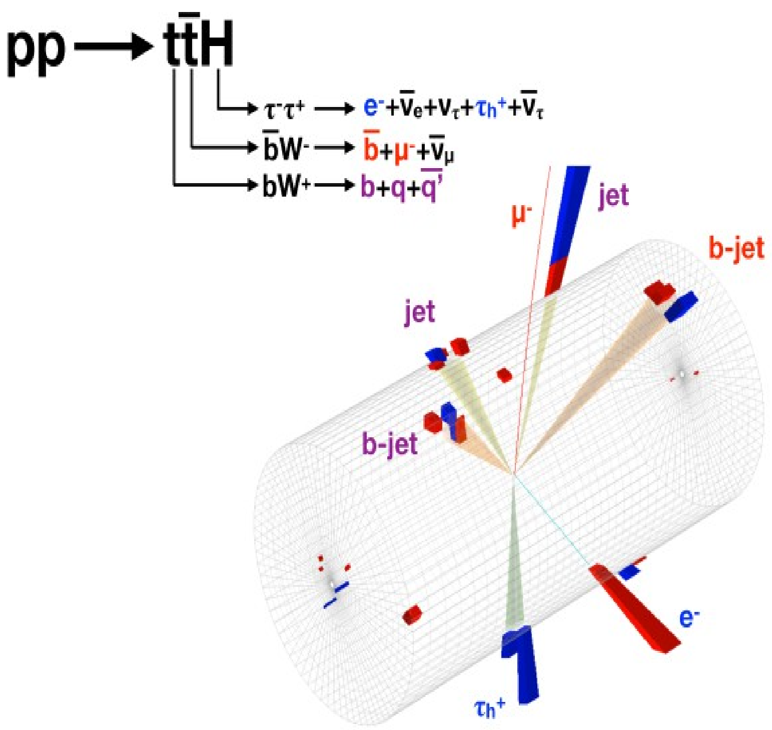
Mass difference between
D* and D_0

Two highlight analysis from 2018

Candidate event for Z(ee)H(bb)



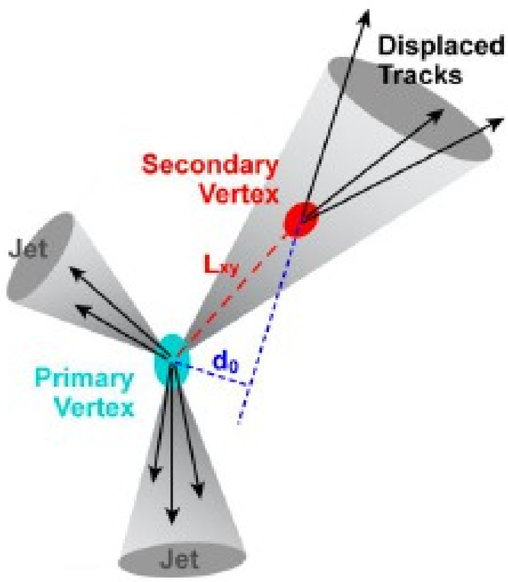
H -> bb

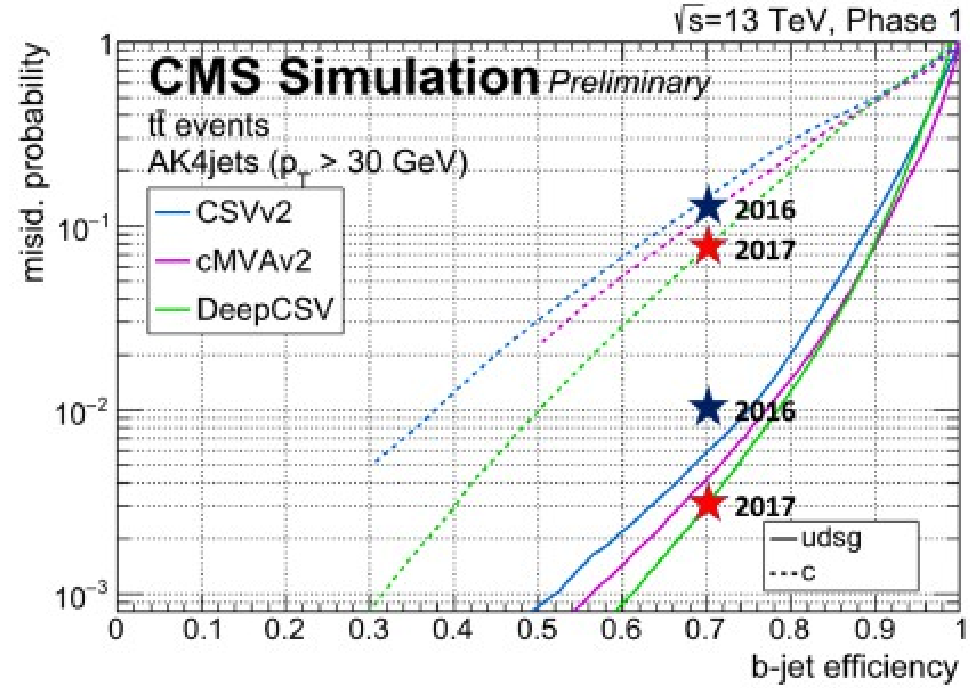


pp -> Htt

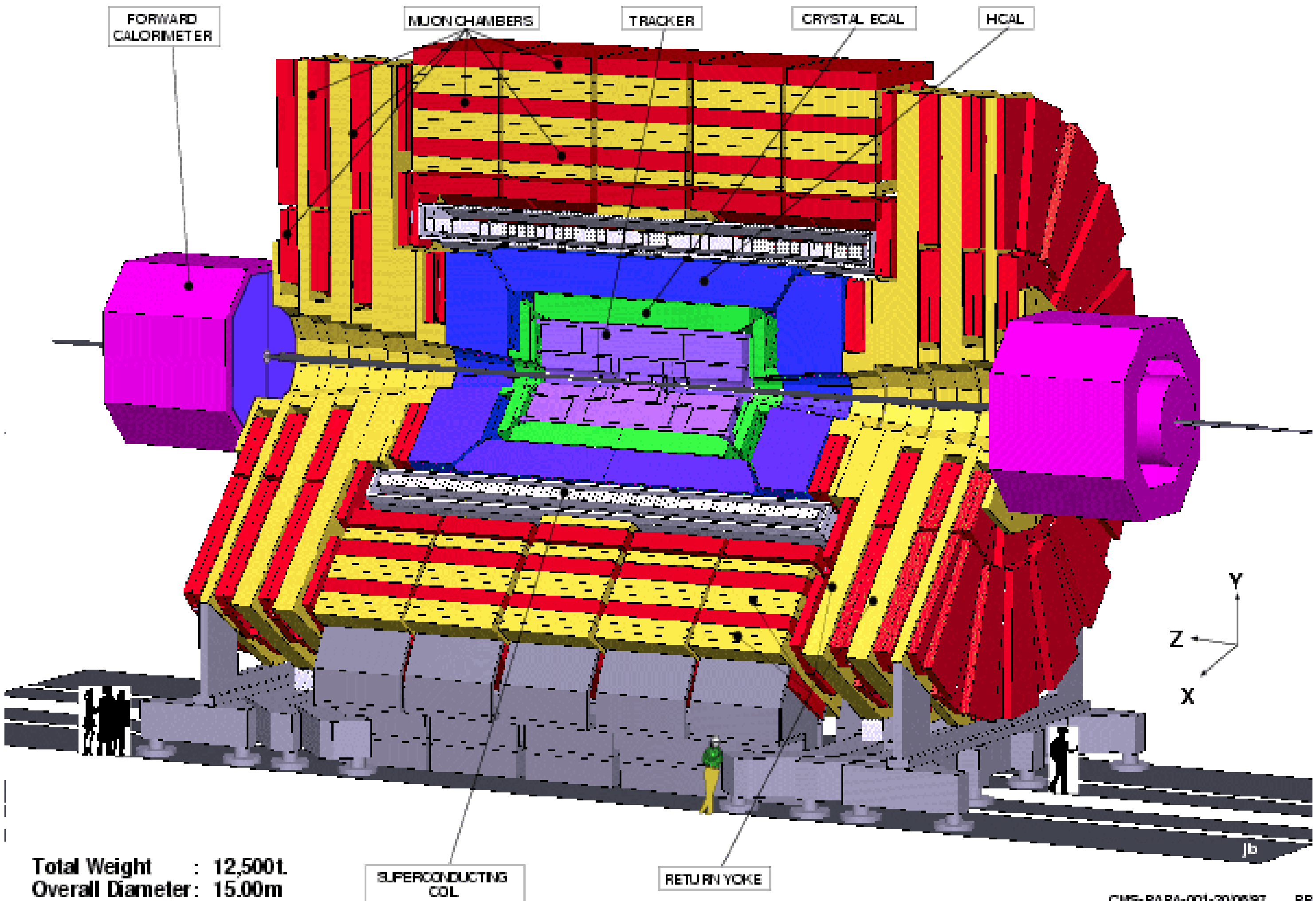
b-jet identification

- **Continuous effort to improve b-tagging at CMS**
  - **New pixel detector** (4 layers)
  - **DNN algorithm (DeepCSV) with additional per-track information**
  - **Contamination from q/g < 1% for efficiency ~70%**
- MC corrections derived on data with $t\bar{t}$ events
- Good agreement between data and MC verified in all analysis regions



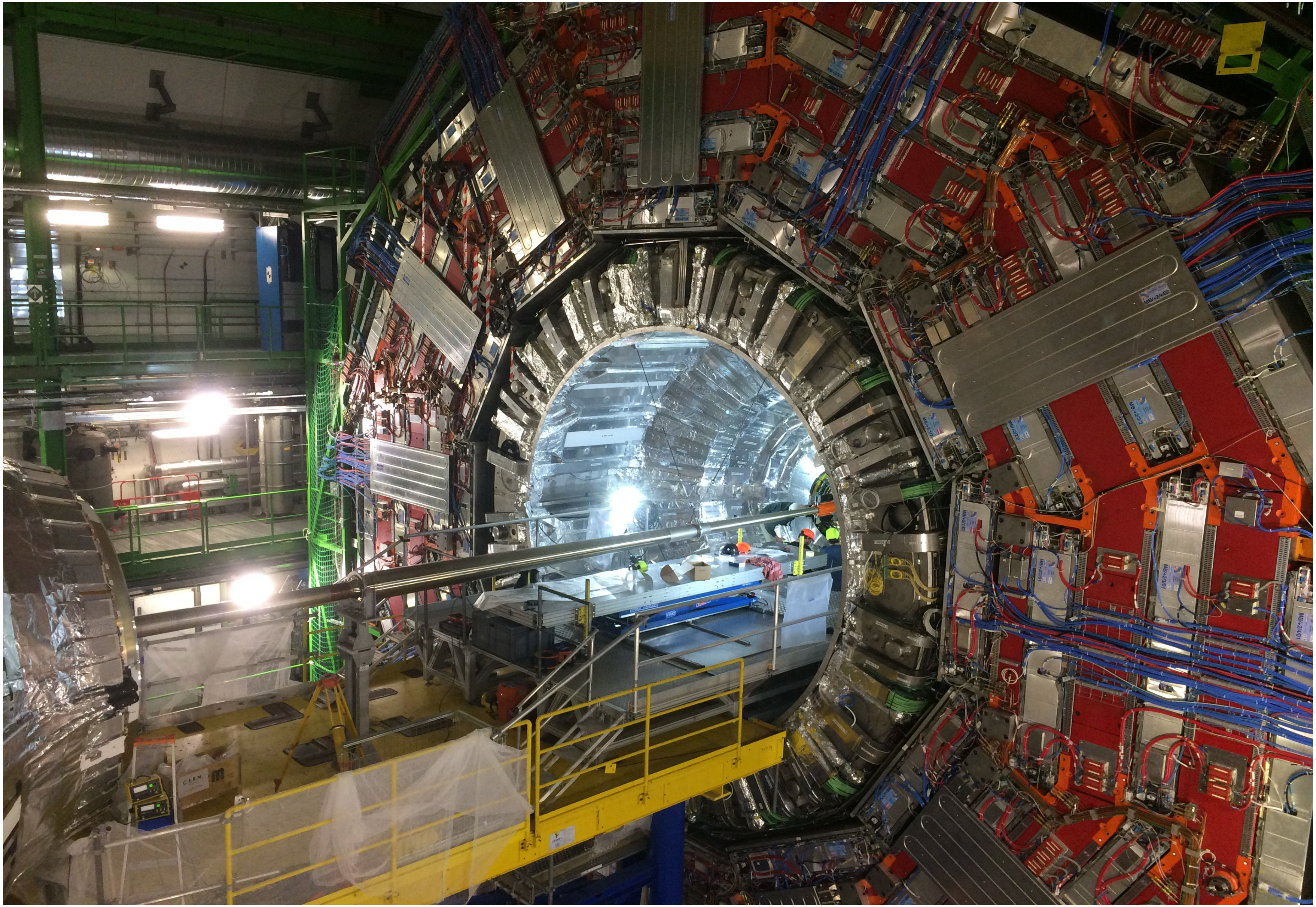


CMS

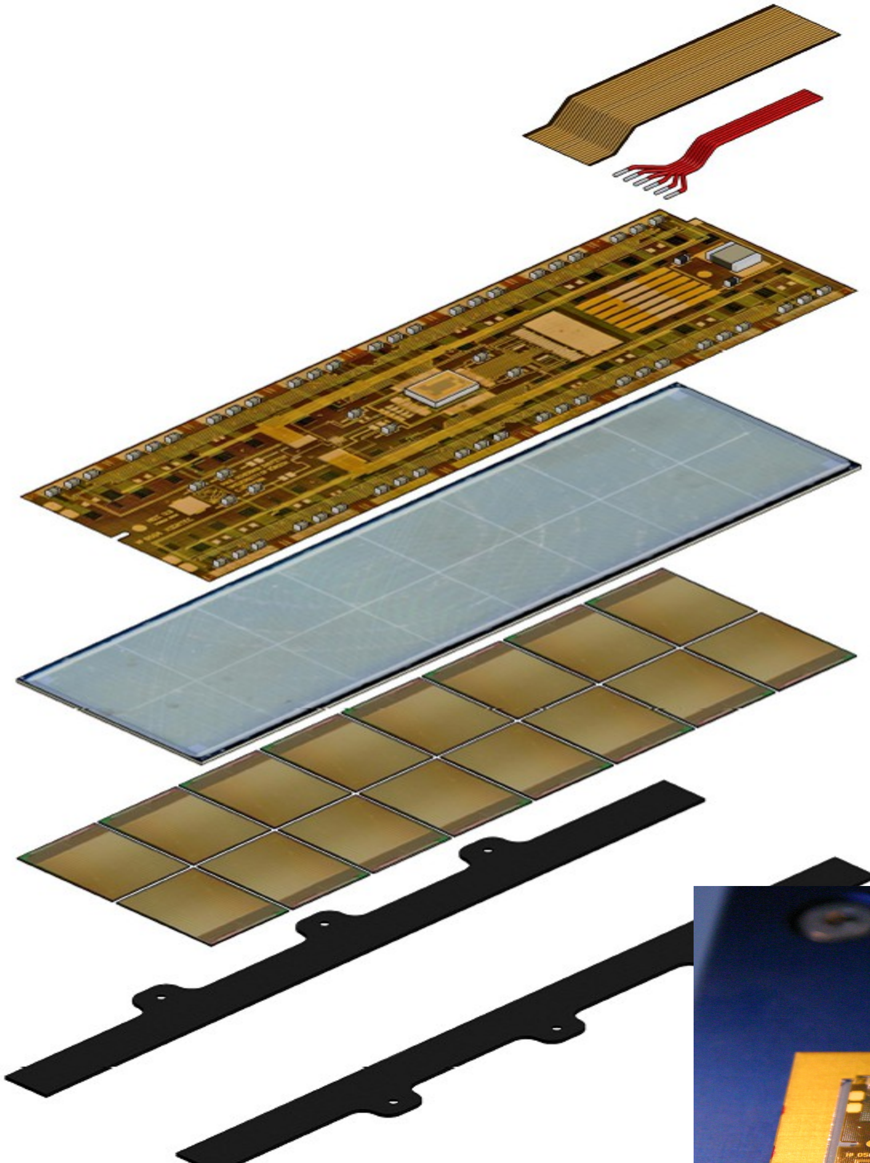


Total Weight : 12,500t.
Overall Diameter : 15.00m
Overall Length : 21.60m
Magnetic Field : 4Tesla

CMS



CMS Module Design



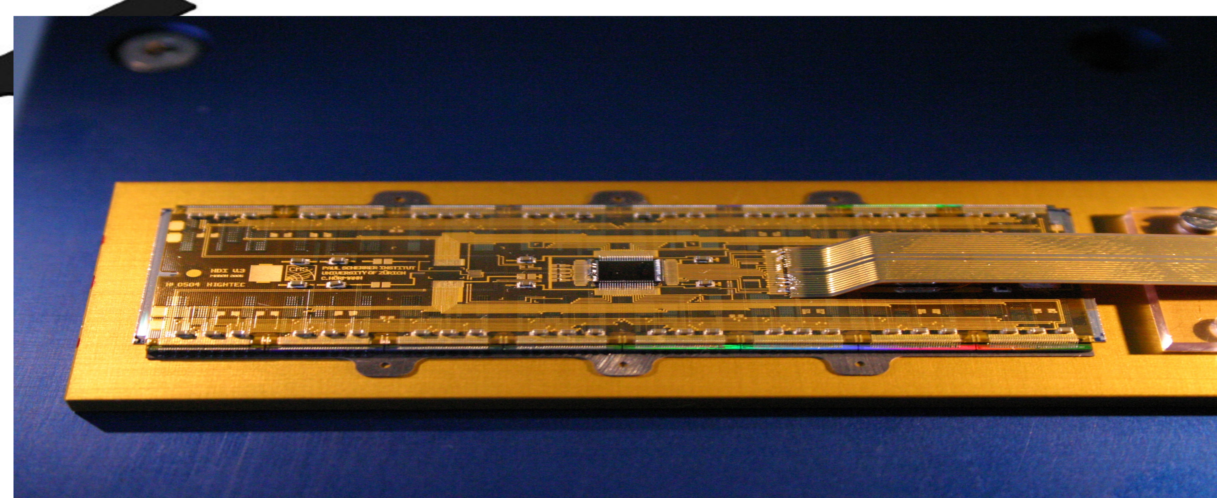
Cables: signals & power

HDI print with the TBM chip

Si sensor (280um)

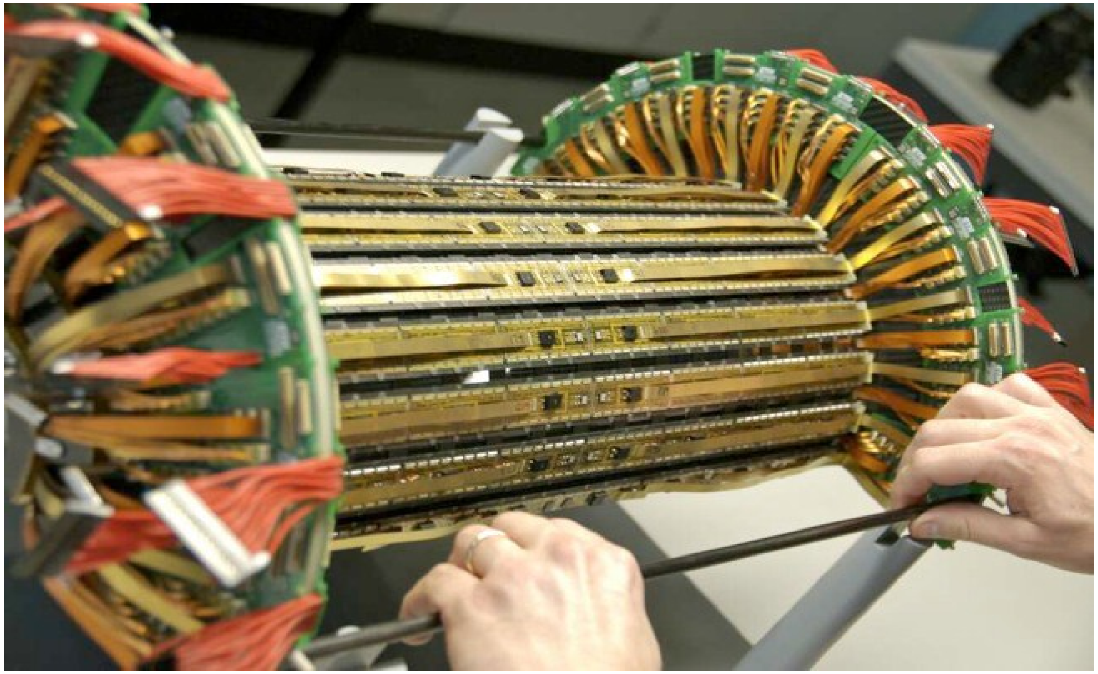
16 ROCs (180um)

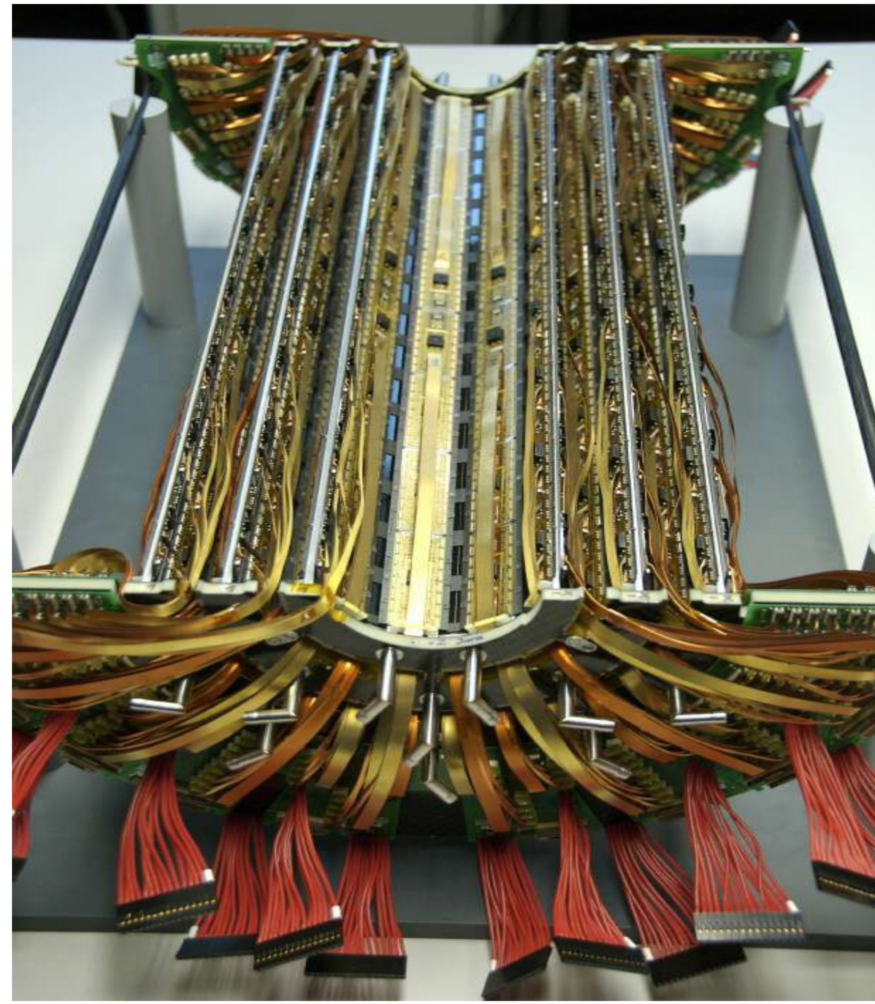
Ready module (1200 produced @PSI)



Base strips: Si_3N_4

The whole pixel barrel





First "Phase-0" barrel pixel detector,
build in 2008-2016 at PSI,
with the help from ETHZ & UZH.

History

1992 – CMS is born, letter of intent, presented at the LHC workshop in Evian

1994 – PSI group joins CMS (tracker & ecal)

1998 – Tracker TDR, PSI starts with the design and construction of the barrel pixel detector (BPix)

2008 summer – Pixel detector installed in CMS, ready for collisions
2008 fall – LHC breaks

2009 fall – first LHC collisions

2010 - collisions at 7TeV

2011-2012 – collisions at 8TeV

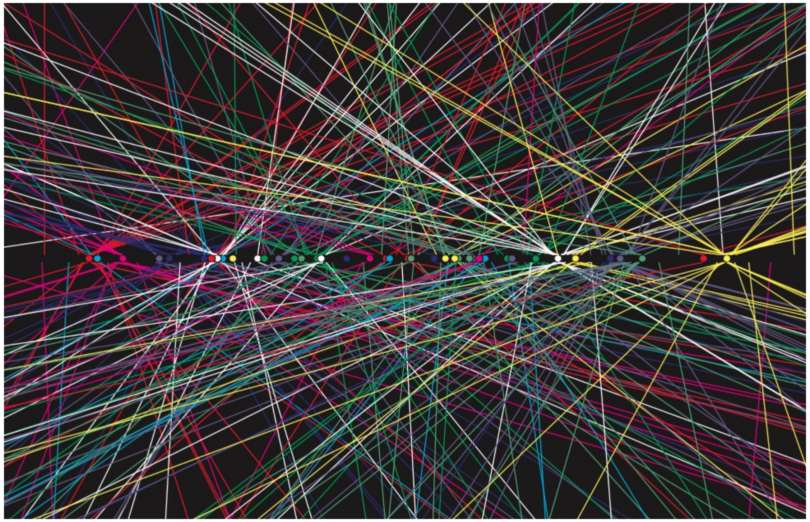
2013-2014 – long shutdown 1 (LS1), after a humidity accident many modules had to be repaired/replaced.

2015-2016 - collisions at 13TeV

A very successful program for CMS & the pixel detector

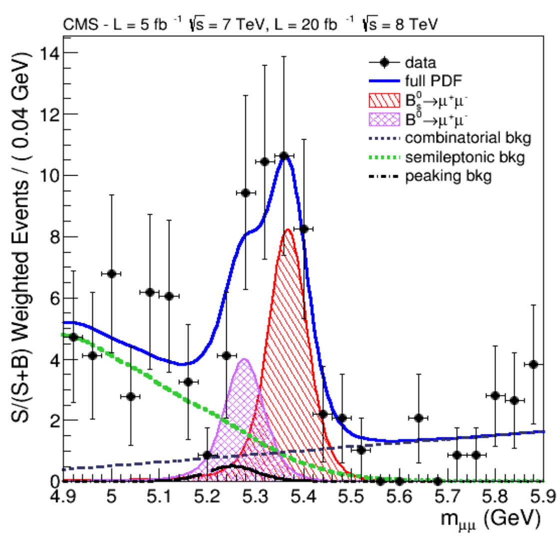
The importance of pixel detectors

Charged tracks from a typical CMS event

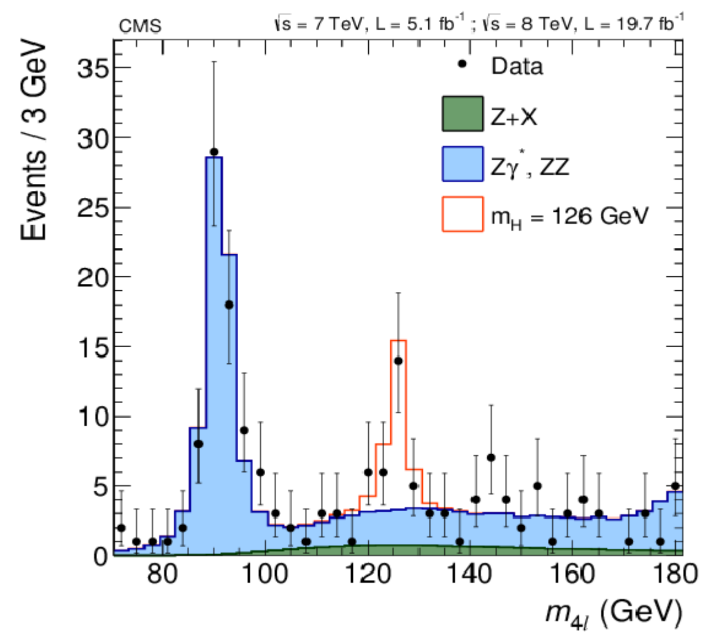


LHC experiments have to deal with simultaneous multiple interactions. Pixel detectors make it possible to separate charge particles from individual interactions. <u>This feature is essential for almost all analysis.</u>

Example I
BF(BS0➔μμ) = 3.0(+1.0,-0.9) × 10-9
(PSI analysis)



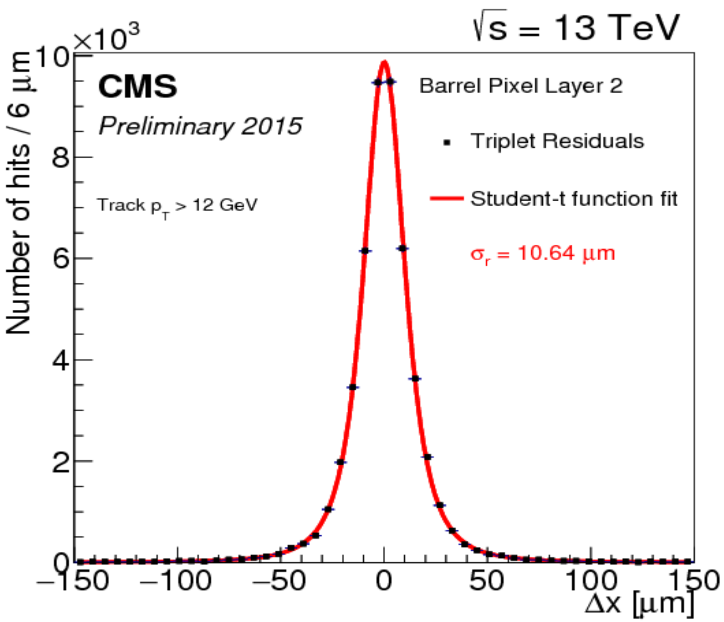
Example II: H ➔4 leptons



Phase-0 pixel detector: performance evolution

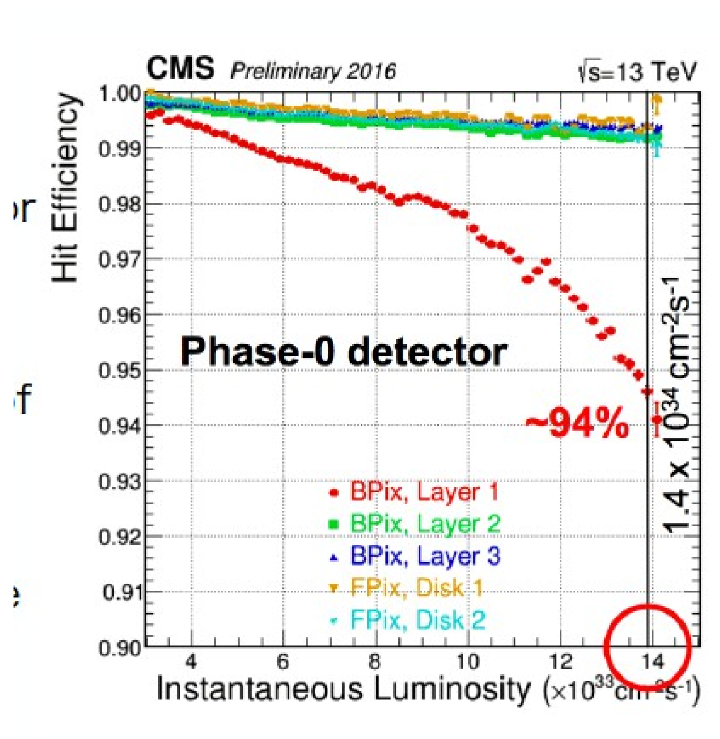
Pixel barrel position resolution measured with 2015 collisions.

Transverse (rϕ) direction



Position resolution – 10.6 µm

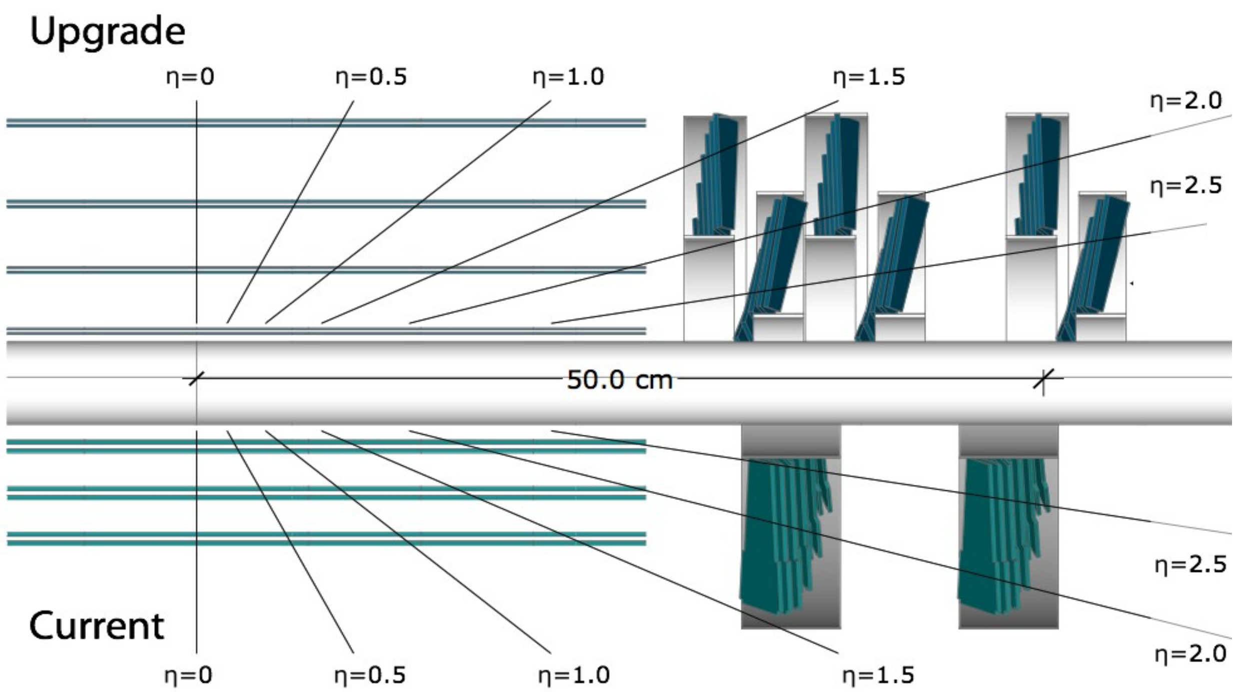
Hit efficiency versus luminosity



Loss of efficiency beyond 10^{34}

Upgrade project

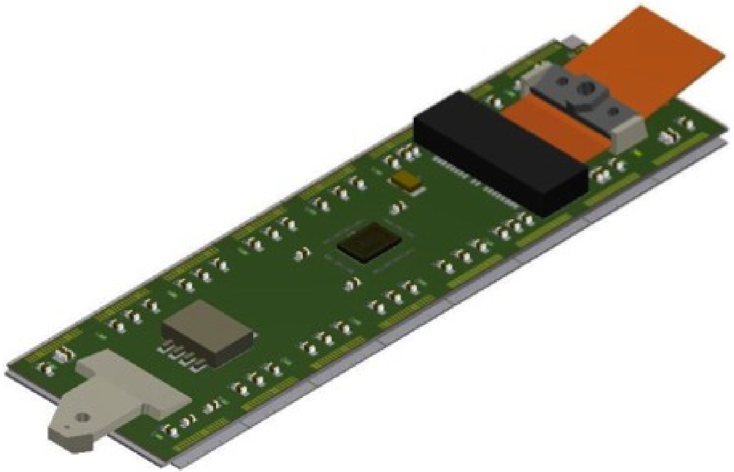
New upgraded pixel detector (“phase-1”) Build in 2013-2016

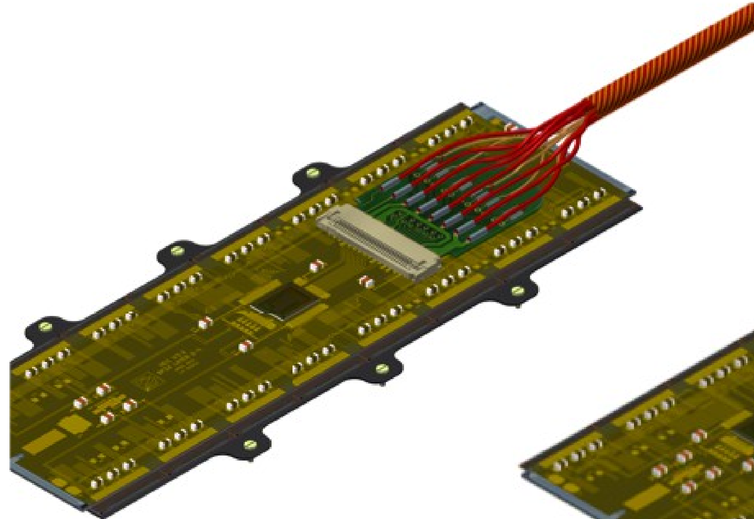


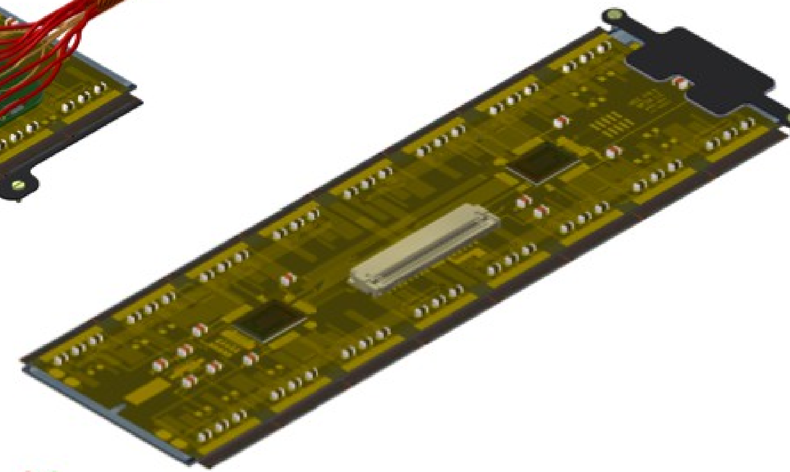
4 barrel layers instead of 3. 3 forward disks instead of 2.

<u>BPix was mostly done by the CH-consortium (PSI, ETHZ/R,Wallny, UZH/Canelli&Kilminster)</u> plus groups from Germany (DESY, UH, Aachen, Karlsruhe) and INFN/Italy.

Pixel Modules







Disk 1-3

672 modules

40 – 100 MHz/cm²

PSI46dig

TBM8b

50 Mrad

672 f bers

Layer 2-4

1088 modules

40 – 120 MHz/cm²

PSI46dig

TBM8b / TBM9 (L2)

50 Mrad

1312 f bers

Layer 1

96 module

580 MHz/cm²

PSI46dig+ ->PROC600

TBM9 -> TBM10

480 Mrad

384 f bers

Layer 1 - History

The L1 ROC (PROC600) has a different readout scheme comparing to our older ROCs. It is really a new design with a new readout architecture.

Development history (Hans-Christian & Beat Meier from our electronics group):

1) The development of of L1 ROC (PROC600) could start only after PSI46dig.
2) 1st version come back from production in **2/2016.** It had several problems, the most famous one was the "soldering iron" problem, basically a high noise problem.
3) 2nd version come back in **7/2016,** just in time for module production. Very little (none) time was left for testing.
4) Module production started in **9/2016** and they were mounted in **11/2016.**

Design parameters:

chip size 7860um x 10'550um, pixel size 100um x 150um

339 transistors / pixel (268 L24 ROC)

pixel array 52 x 80

DCCD transfer in DC at 40MHz **-> new column readout arch.**

Data Buffer Cluster Cells (4x) 56

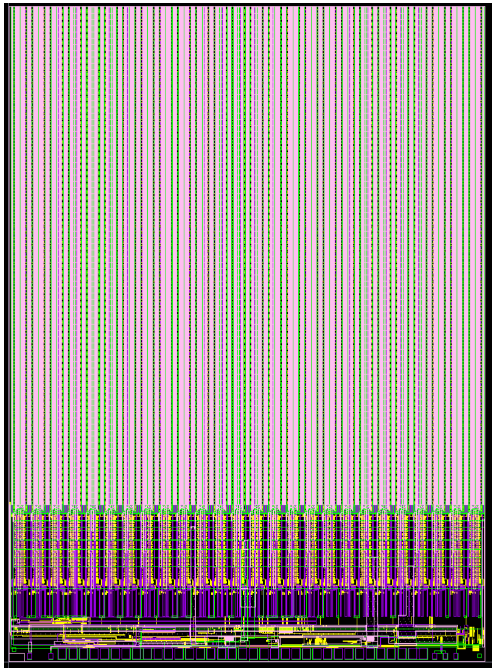
Timestamp Buffer 40, ROC Read-out Buffer 64

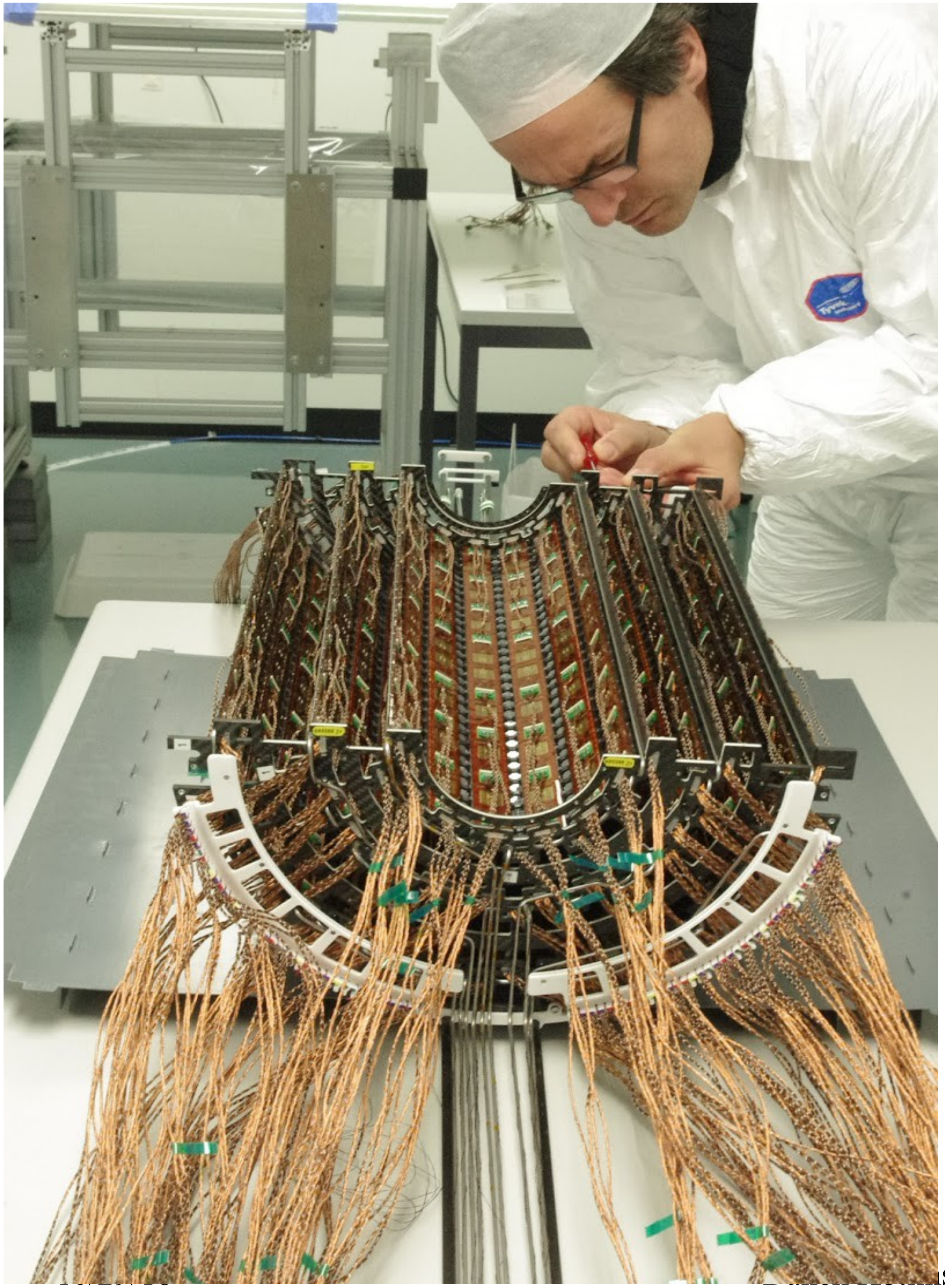
Total transistor count : 2.2 M

analog pulse height : 8 bit ADC

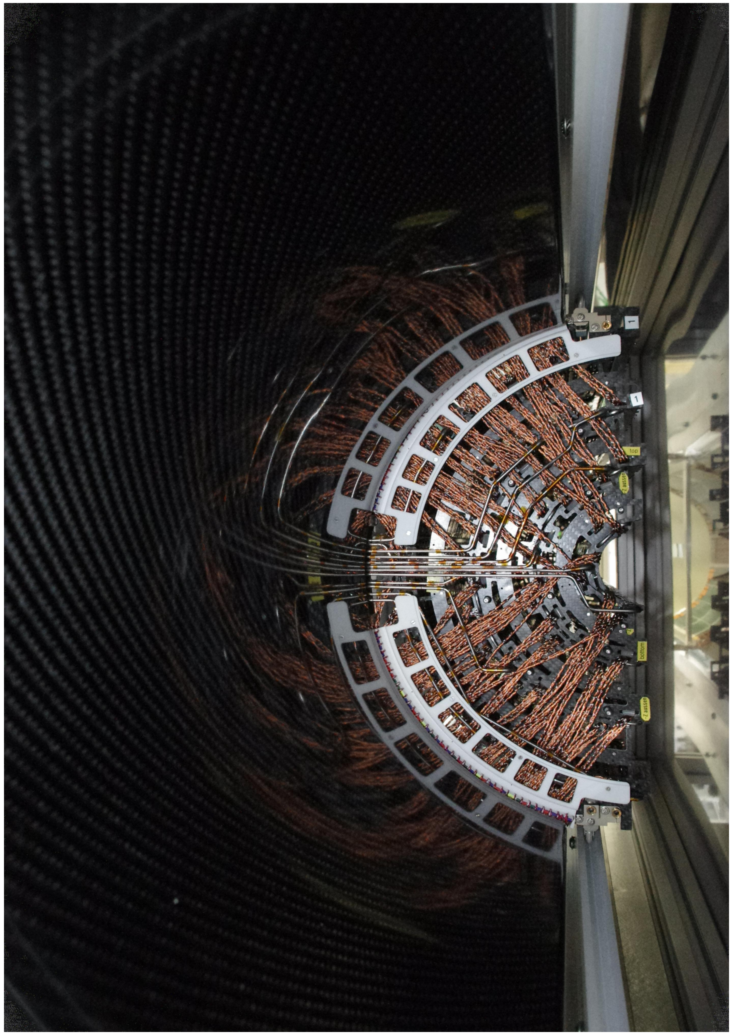
pixel rate ~600MHz/cm^2

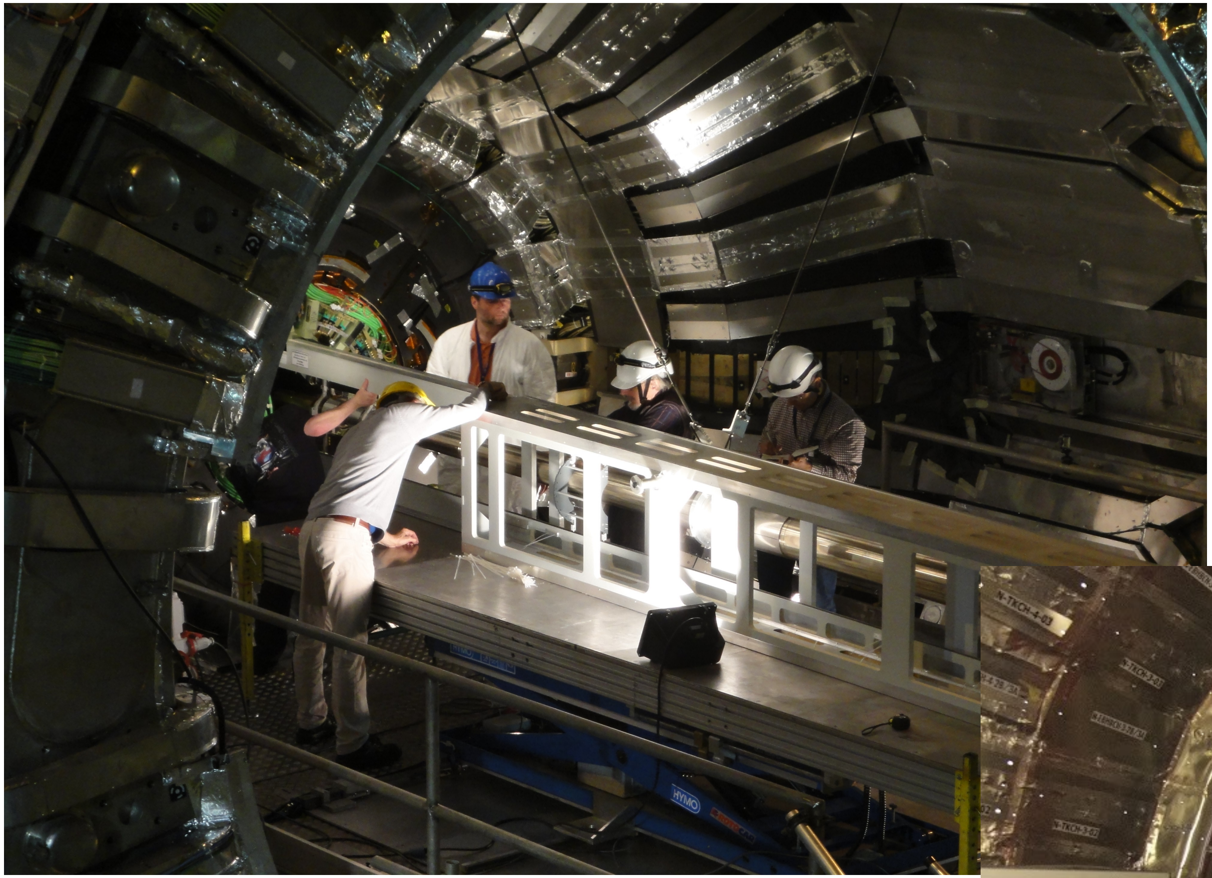
expect rad. hardness ~200Mrad



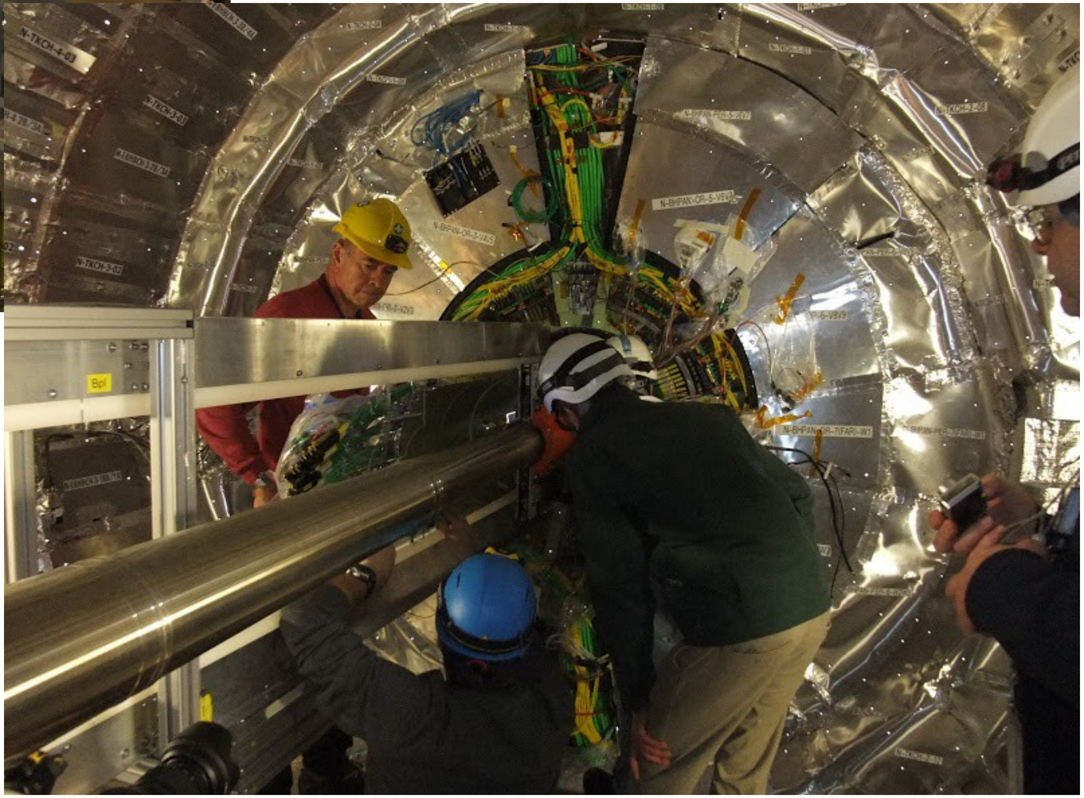


Phase-1 BPix detector
assembled at PSI in 10-12/2016
in Malte's clean room,
with big help from Malte
& his technicians.





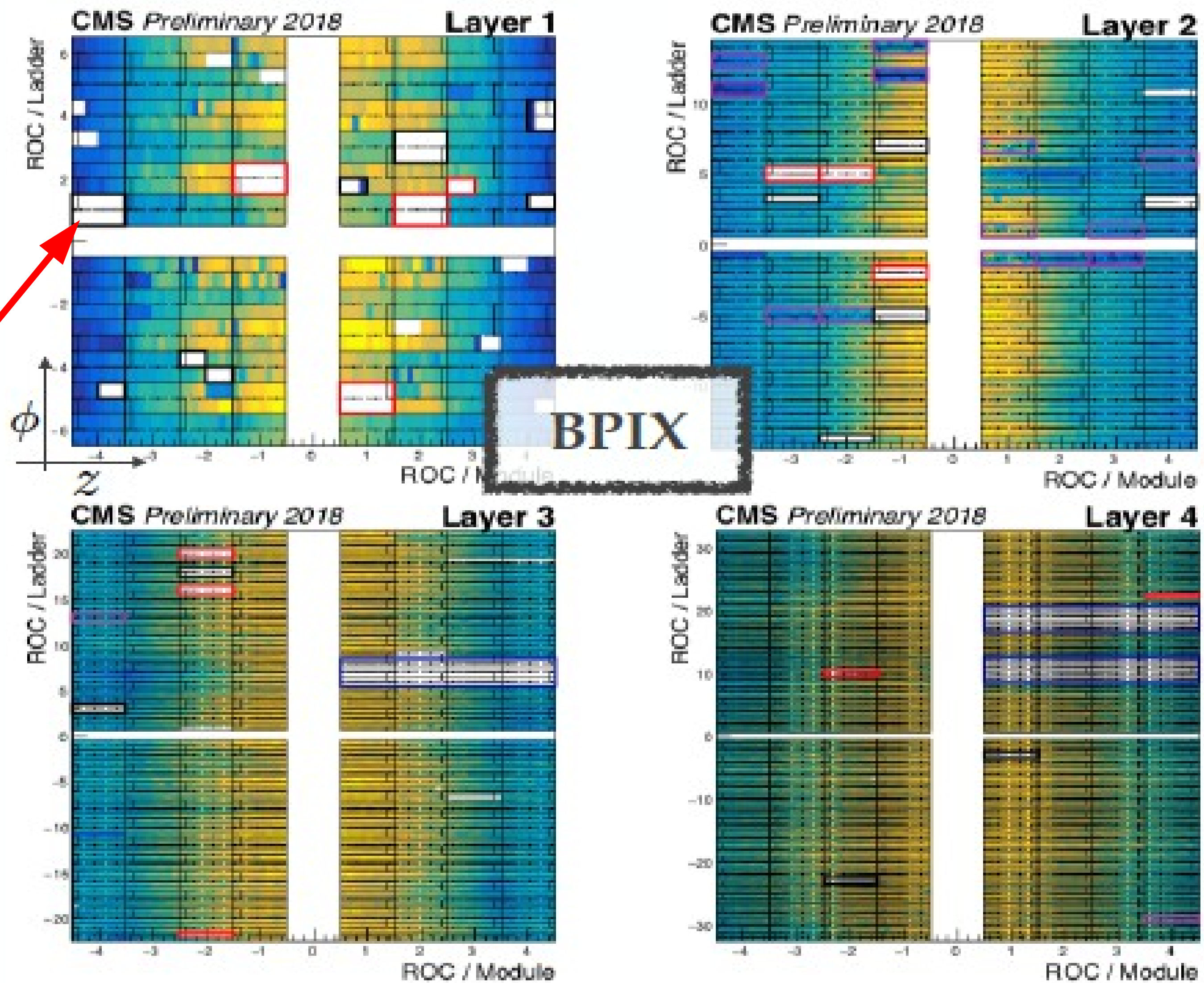
Transported to CERN 7/2/2017
Installation 28/2/2017



Commissioning & calibrations
3/3 – 31/4/2017
First collisions - 23/5/2017

First big surprise already 1 day later!

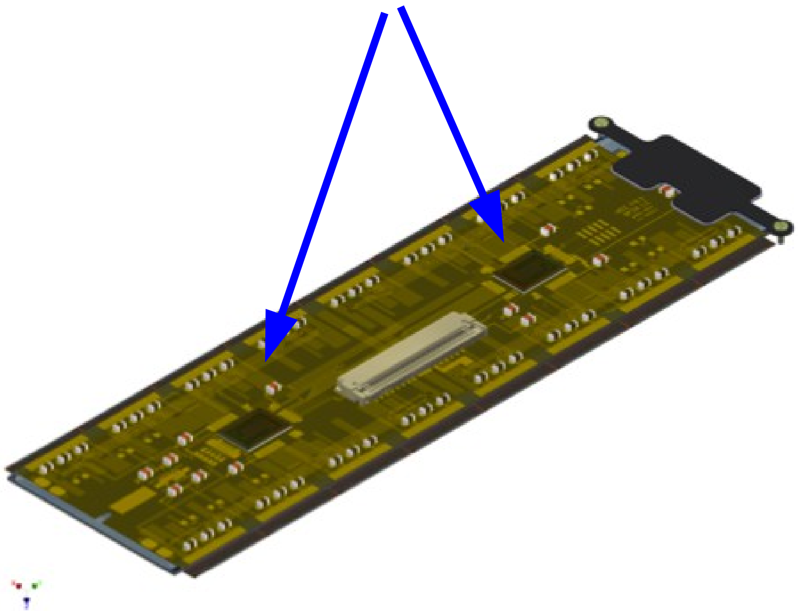
BPix efficiency map

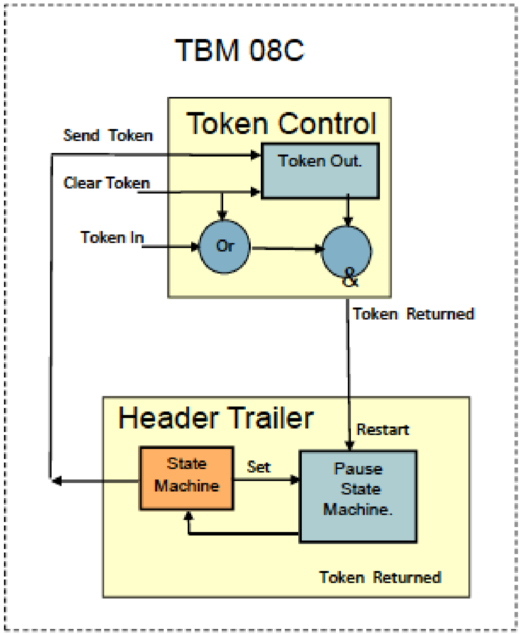


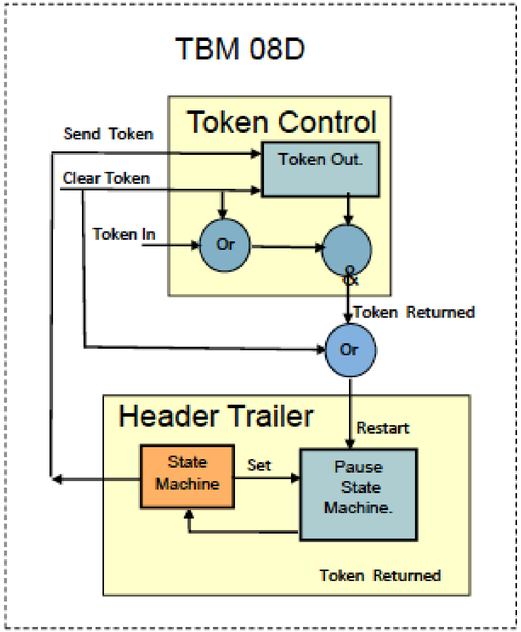
Unexpected new holes. New bad modules!

The modules stayed bad even after repeated resets and reprogramming.
However they recovered a few days later.

Eventually it was determined that a power cycle revives stuck modules.
From the granularity of the failures it was concluded that the problem is in the TBM chip (Rutgers/USA).







A logic mistakes allows for a possible locking of a circuit in the TBM.
A reset does not clear the locking condition.
SEUs can cause the locking & the relevant FlipFlop <u>was not SEU protected -> large rate.</u>

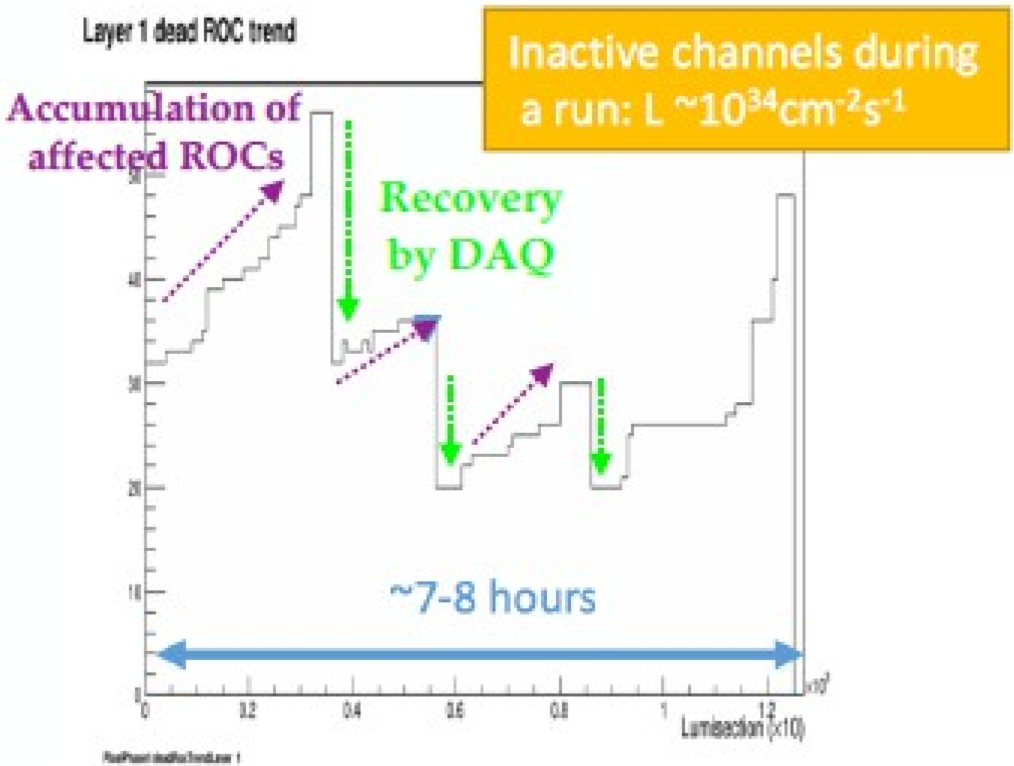
Only a power cycle helps!

Regularly power cycling the detector

Initially manual power cycles were made.
Later we developed a fully automatic procedure which could run while taking data.

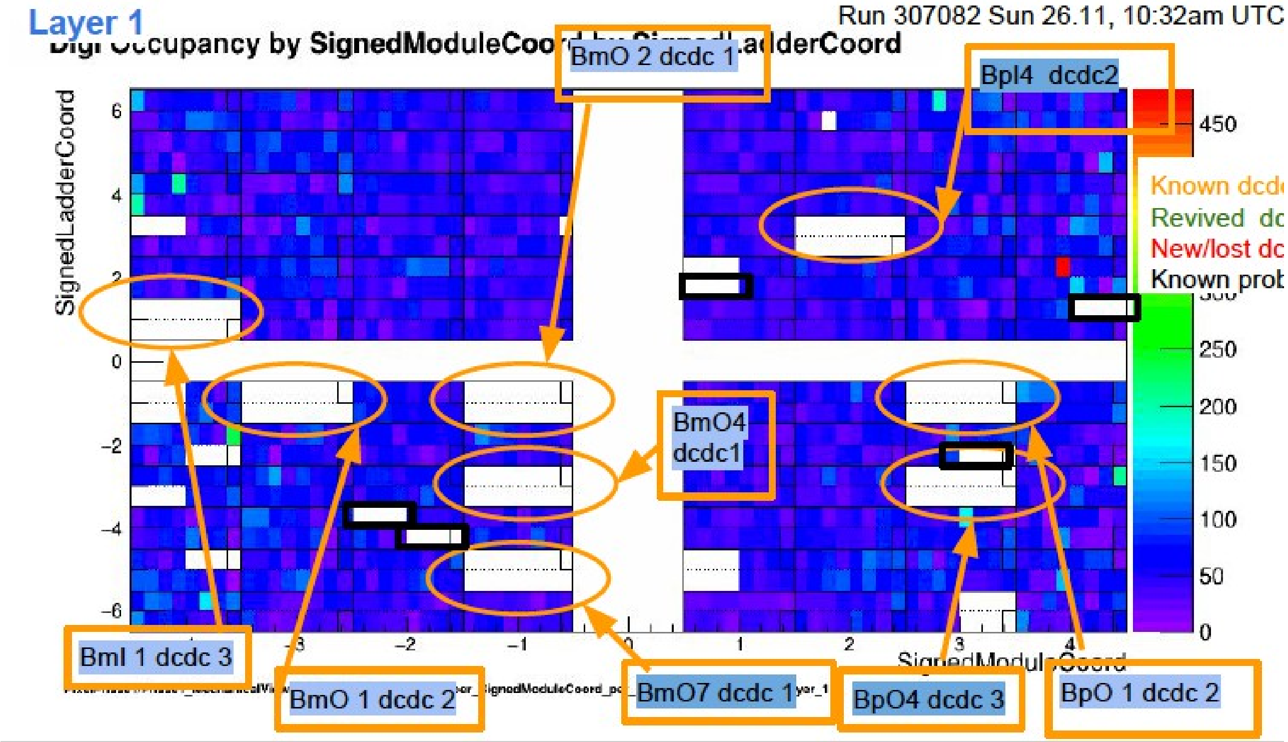
- stop triggers
- power cycle the stuck modules
- reprogram the modules
- start triggers

~ all in < 30 sec.



Power cycling of the pixel detector is a very heavy procedure.
Luckily we had a way to power off/on with a very small granularity.
Or was it unlucky!

We were happily taking data until 5/10.

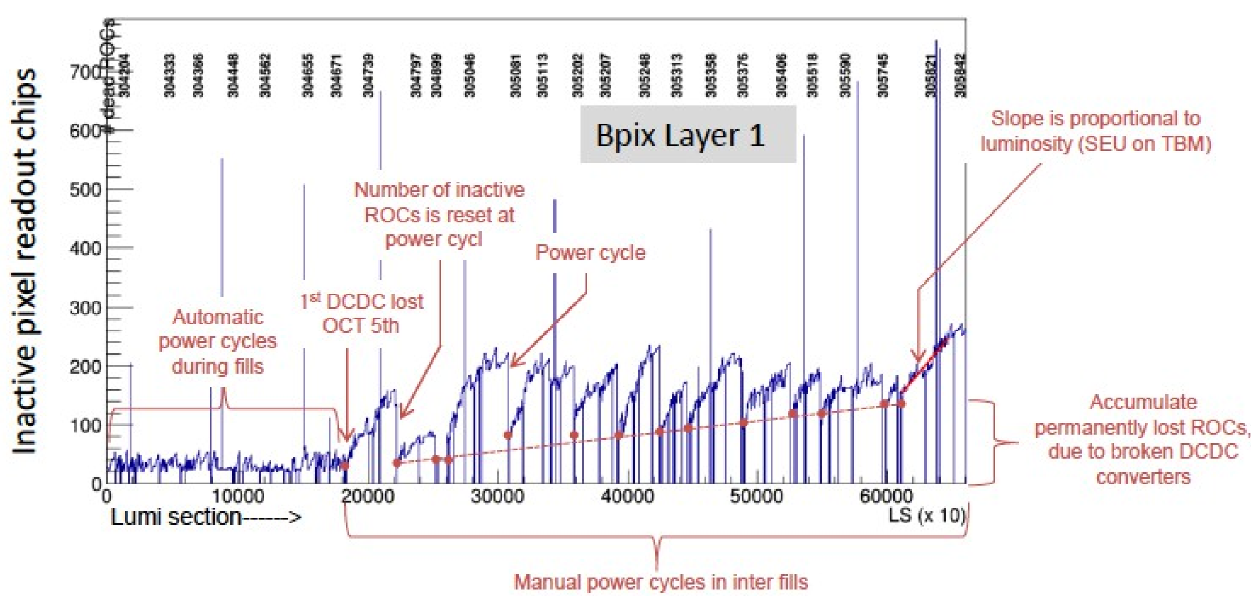


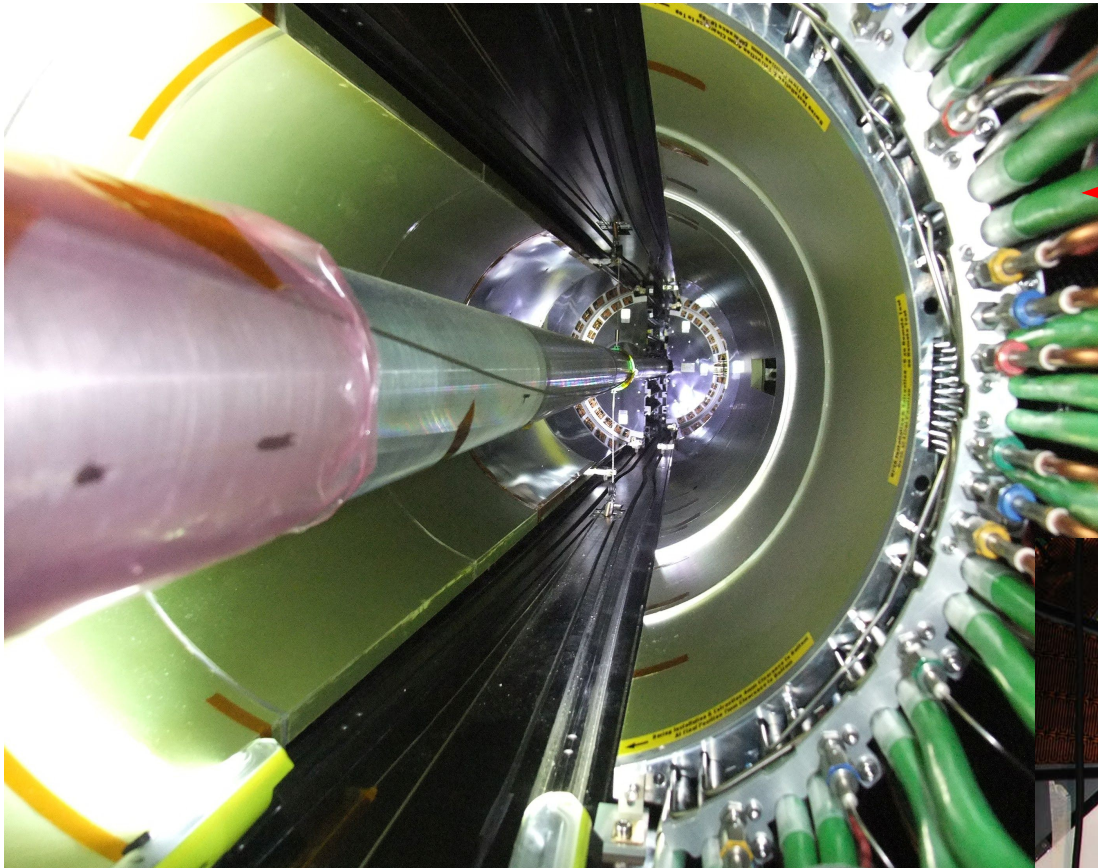
On 5/10 a few FPix modules died, power cycles could <u>not revive them.</u>
On 8/10 BPix modules started failing.

New holes started appearing after every LHC fill!

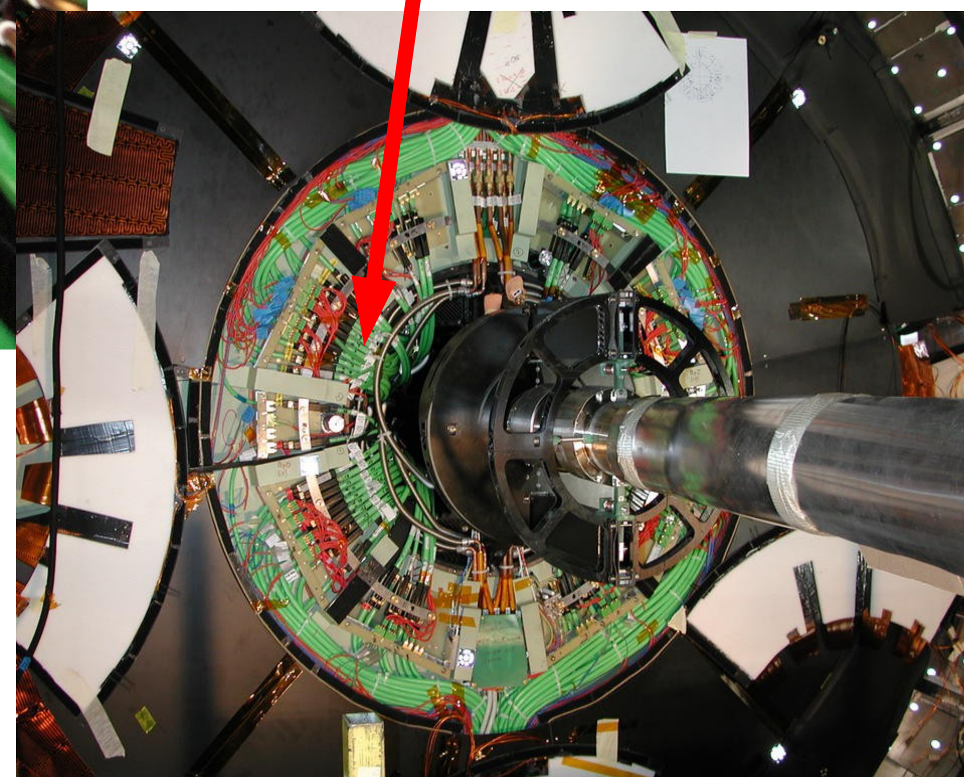
From the granularity it pointed in the direction of failed DCDC converters.

Automatic power cycles were stopped.
Only manual cycle were allowed.



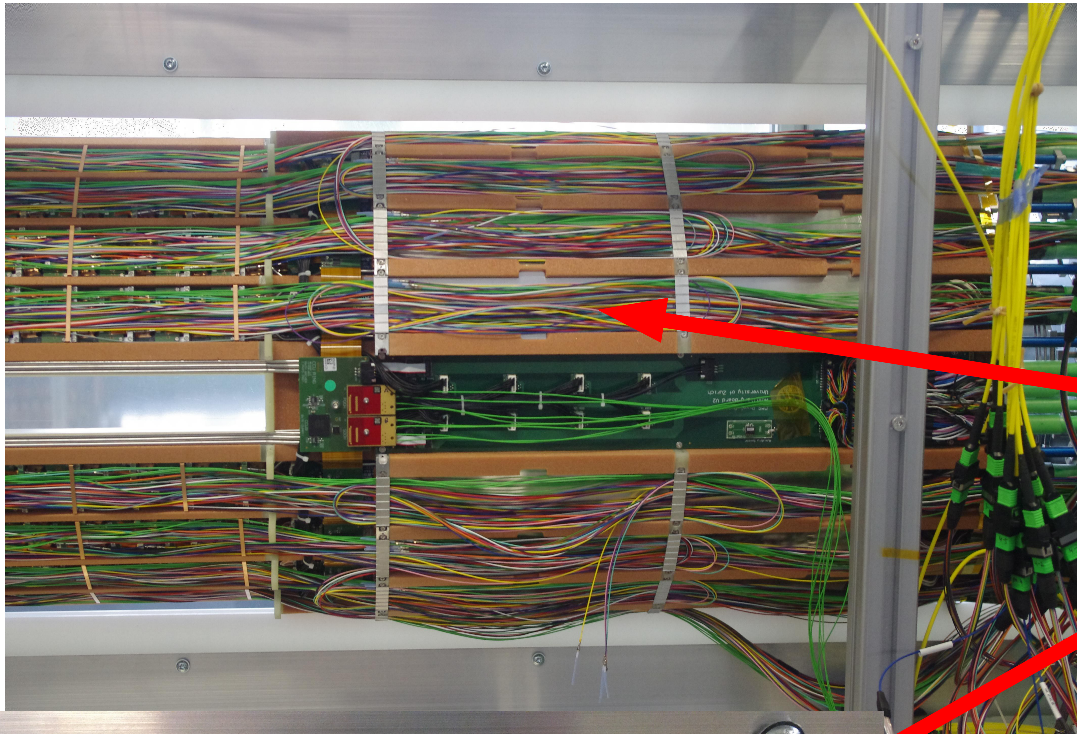


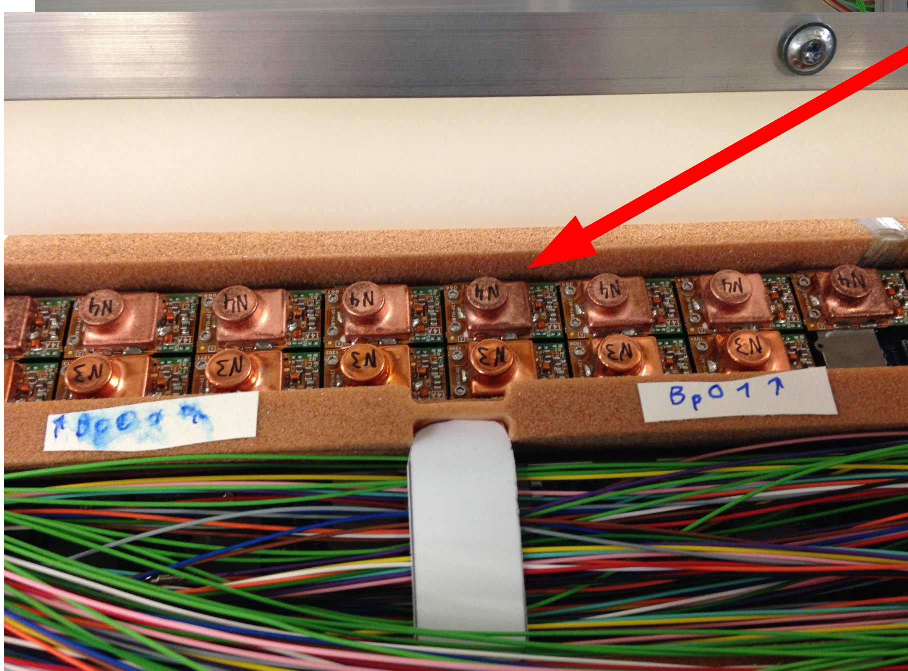
Phase-1 detector has many more modules -> needs more power. But the number of cables was fixed.



These cables could not accommodate more current, voltage drops too big.

Therefore decided to use DCDC converters to step from 10V to 3V.





The DCDC converters are located here

DCDC converters are based on a rad-hard chip FEAST from CERN and were build in Aachen.

There are ~1300 converters.

DC/DC converter / FEAST2 ASIC

Converter circuit for Pixel

FEAST2 ASIC

- Developed by CERN
- Safe for operation in magnetic field (4T)
- Radiation hardness
  - 500 Mrad (Si)
  - 5 x10^{14} n/cm^2 (1MeV eq)
- enable/disable control
- Next version of FEAST ASIC is the baseline for the powering system of ATLAS and CMS pixel and strip tracker for High Luminosity LHC.
  - This upgrade project was the first large-scale application of the chip.

Many thousands of such devices are planned to be used at HL-LHC in 2025-2030.

Our problems caused a storm and triggered large number of activities including e.g. killing converters with 1kV sparks!

Most transistors in the FEAST chip are radiation tolerant by using the so called Enclosed-Layout-Transistors (ELT).
Apparently high voltage transistors cannot be designed in this way.
For the 10V power transistors FEAST uses nLDMOS design which is sensitive to radiation.

These transistors can be protected by adding an ELT transistor to cut the radiation induced leakage current. For one 10V transistor this protection was forgotten making it fail after about 0.5Mrad.

The FEAST chip was qualified by many irradiations, including at the PIF facility at PSI. No failures were observed because the faulty transistor is located in the enable/disable circuit which was not exercised much during “normal” operation.

In CMS pixels we used the disable/enable feature to power cycle the modules affected by the TBM getting stuck!

More details here:
http://project-dcdc.web.cern.ch/project-DCDC/

Understanding the issue and plan

- Eventually, understood as overvoltage at "disabling" converters.
- In an irradiated converter, leakage current increased, and a capacitor is charged up.
  - a 3.3V capacitor charged up to ~11V **when FEAST chip is disabled,** which damage FEAST start-up circuit.
- Workaround for 2018 : Ceased disabling FEAST for power cycle of modules, and use supply power cycle keeping FEAST chip enabled,
  - No DC/DC converter failure this year after accumulating 60 fb^{-1}.
  - Final solution : development of improved FEAST chip ongoing. Will be available during LHC Long Shutdown 2(2019-2020).

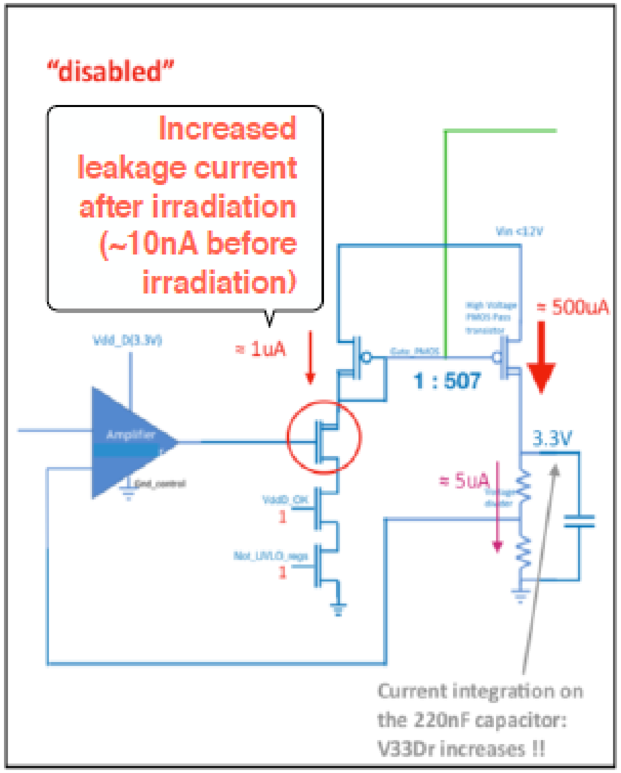
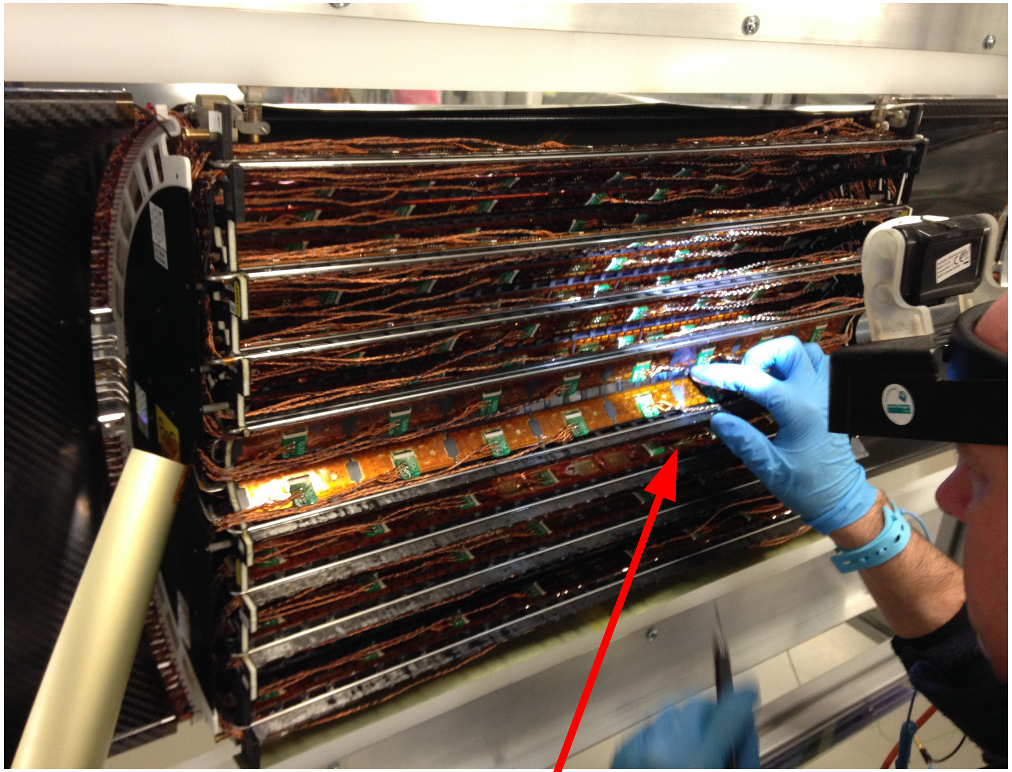
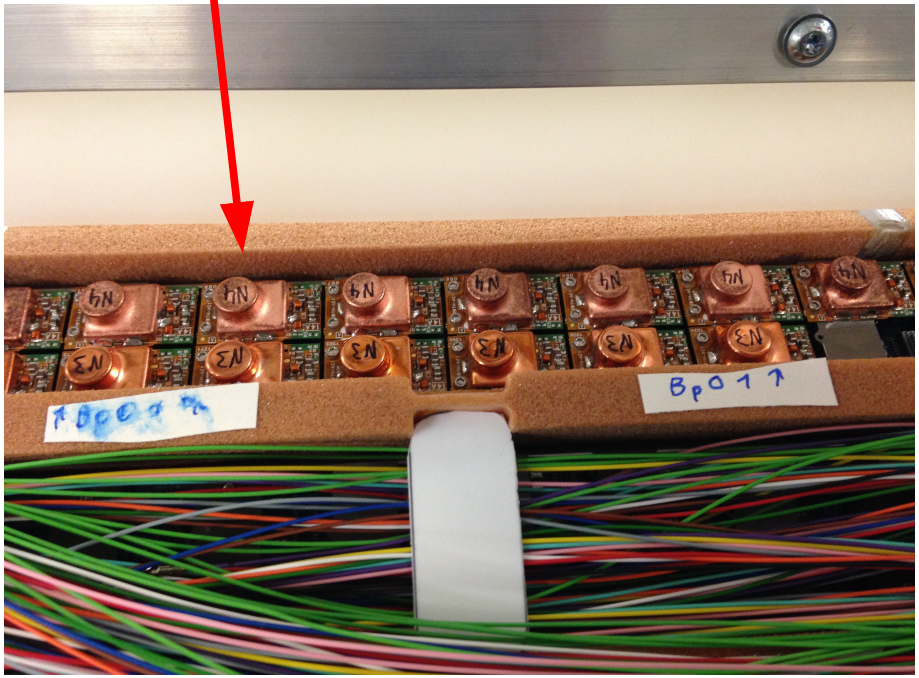


Figure by F. Faccio (CERN)

BPix repairs in winter 2018

Replace all 830 DCDC converters, no only the broken ones.





Replace 6 broken layer-1 modules. The modules were damaged by no LV while HV was ON (see Silvan's hand).

We only had 2 weeks to finish it all

Other problems

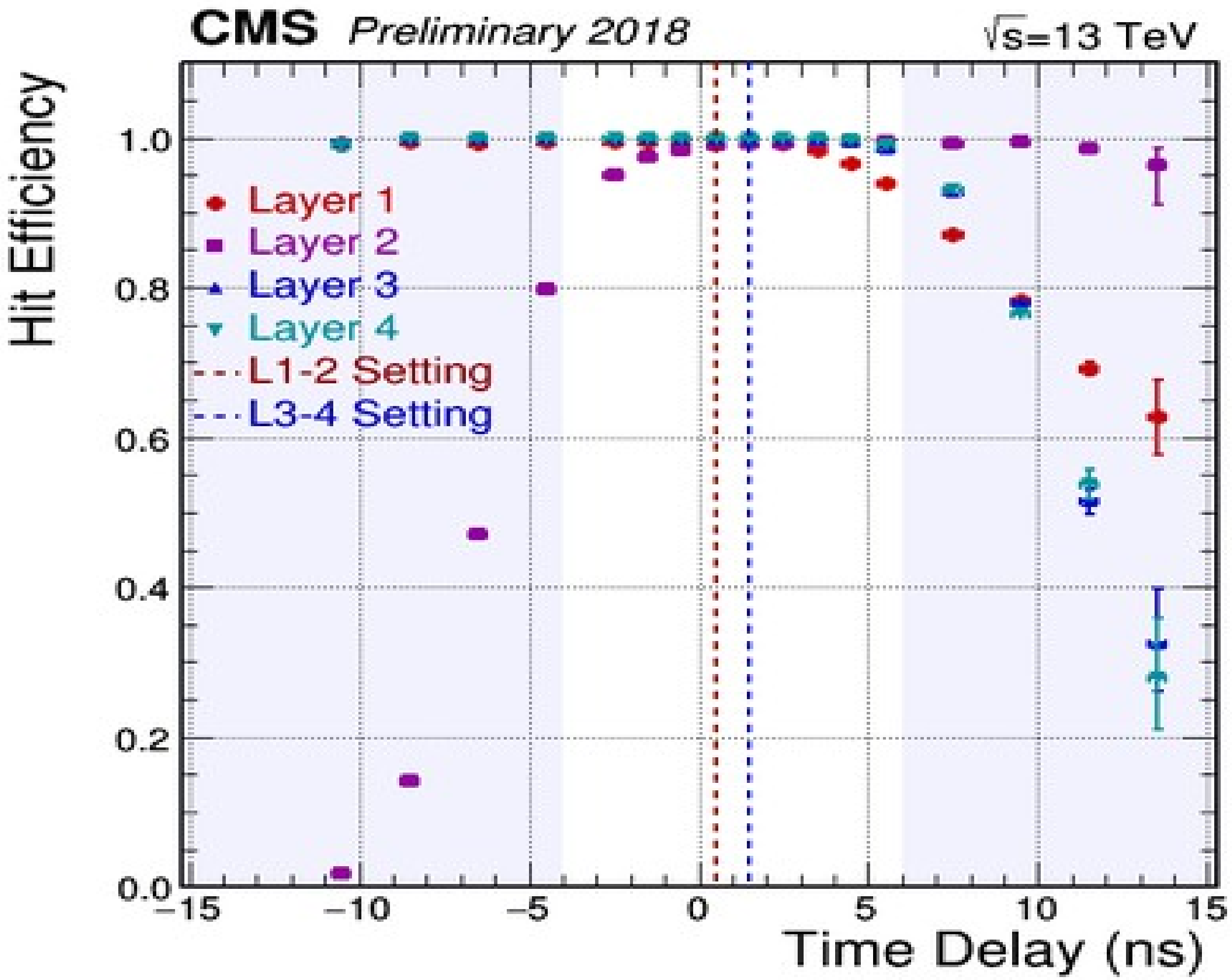
1) Timing difference with respect to Layer 2.
   Layer 1 PROC is 1/2 clock faster than the Layer 2 ROC

2) Larger cross-talk than expected, leads to higher thresholds

3) Hit inefficiency:
   (3a) low luminosity (~ 1E33)
   (3b) high luminosity (>1.4E34)

Contrary to the two previous these three were our responsibility.

Timing Problem



Layer 1 ROC shifted by ~12ns with respect to layer 2-4 ROC.

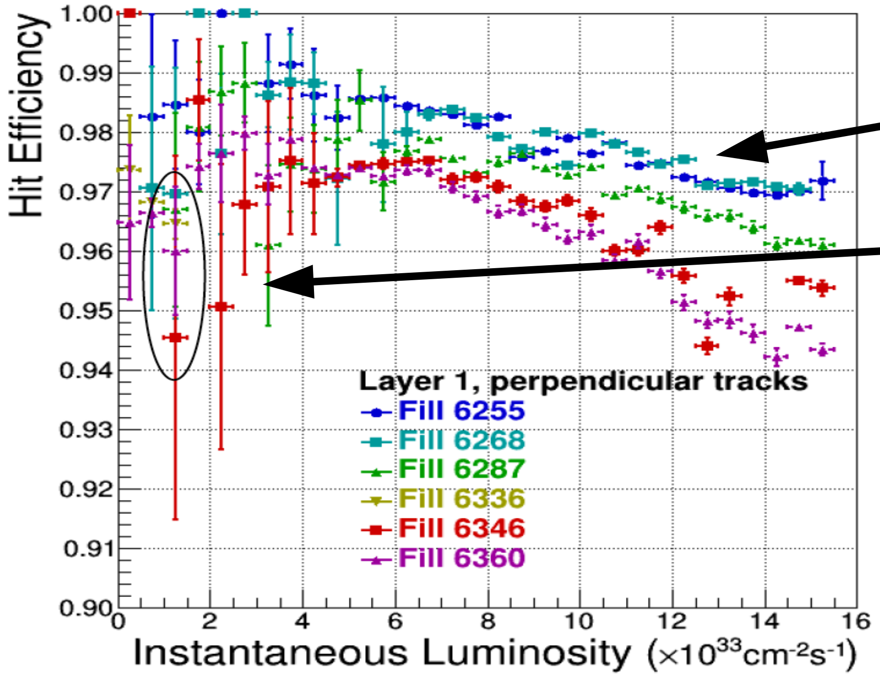
The shift comes from the PROC being faster.

Cannot be compensated because Layers 1 & 2 are on the same clock line.

Manged to find a common working point nevertheless there are some negative consequences.

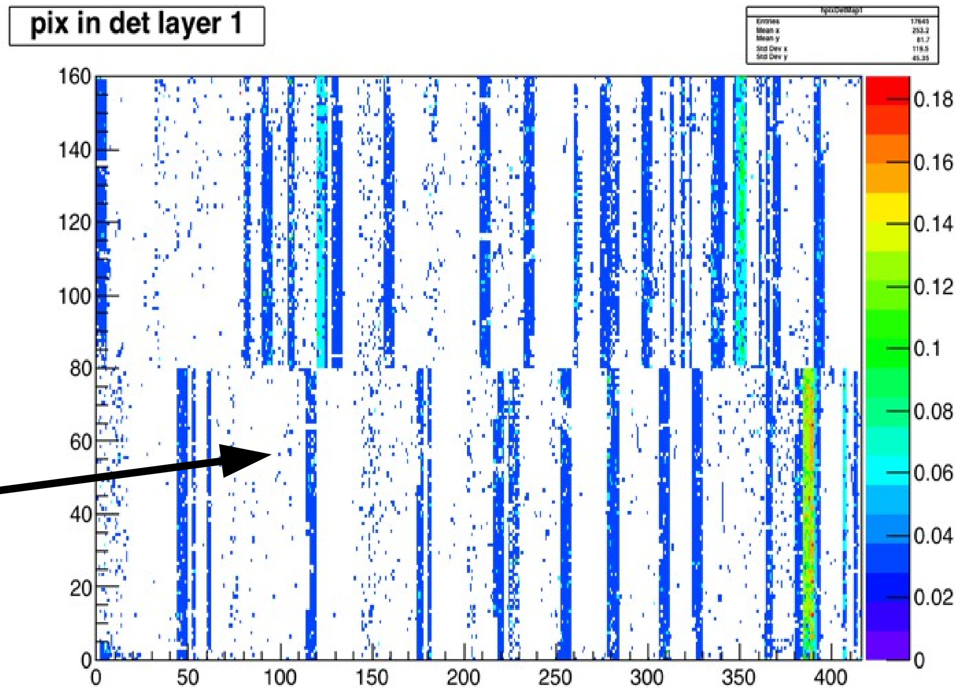
Hans-Christian calls it a “communication problem”.

Efficiency & cross-talk problem



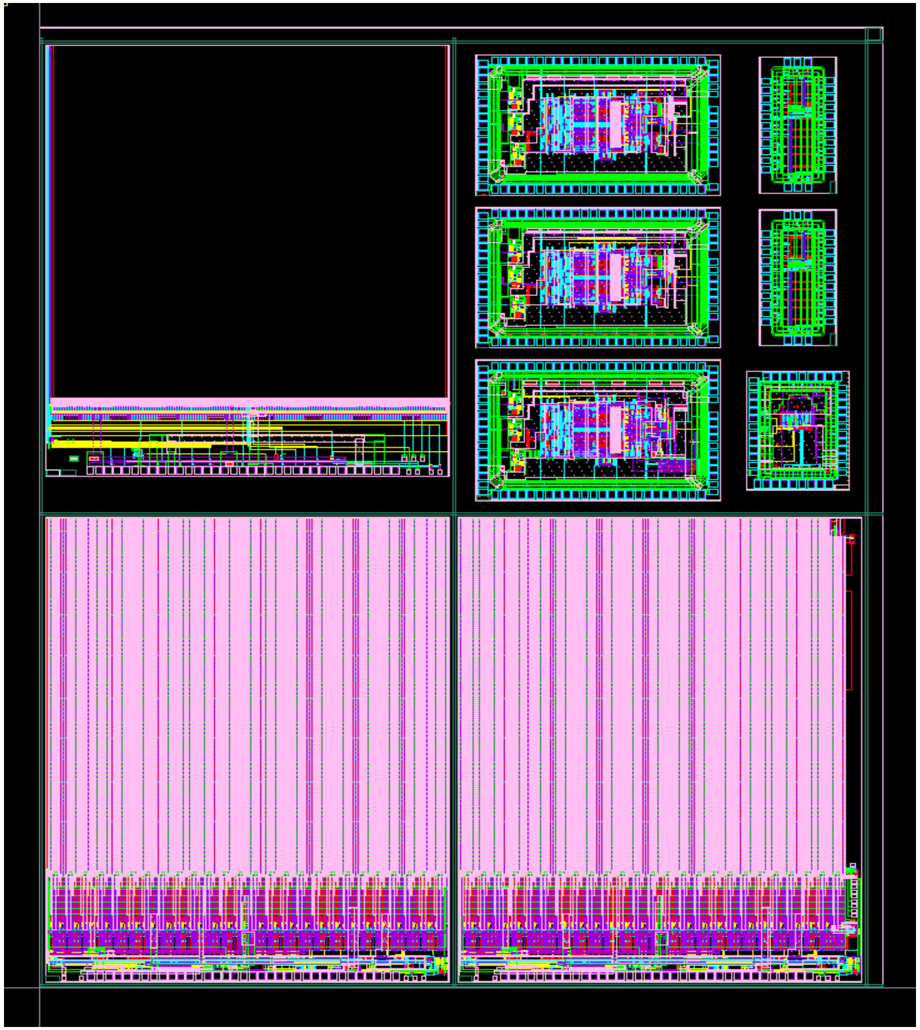
High rate inefficiency

Low rate inefficiency



Cross talk “noise” hits appear several clocks after the real hits.
They tend to fill whole double-columns with hits.
A very non-physical pattern.

Solution – a new PROC600 chip V3

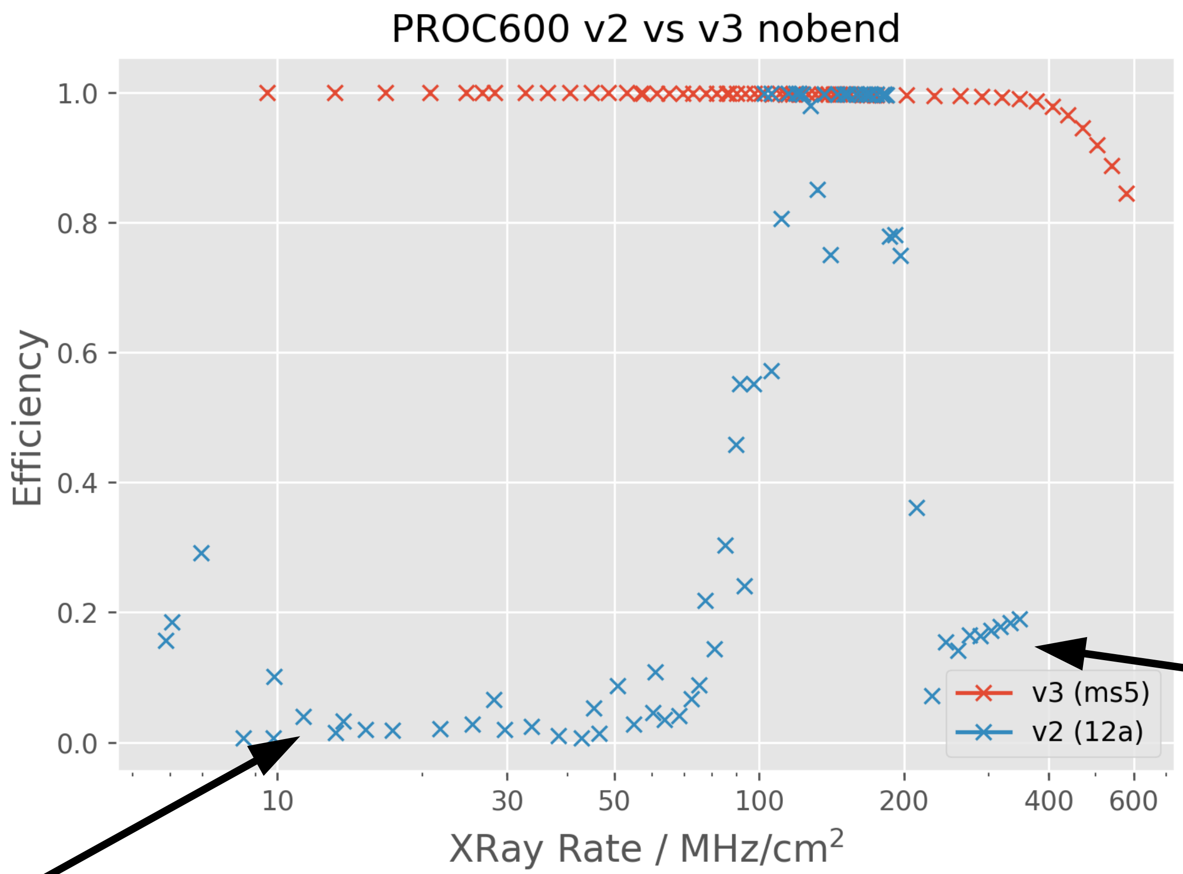


Hans-Christian & Beat understood the problem and resubmitted an improved (V3) version of it in February 2018.

It came back in May.
Stephan Burkhalter, ETH masters student, did most of the testing.

Hit efficiency versus rate

NO
RESETS!



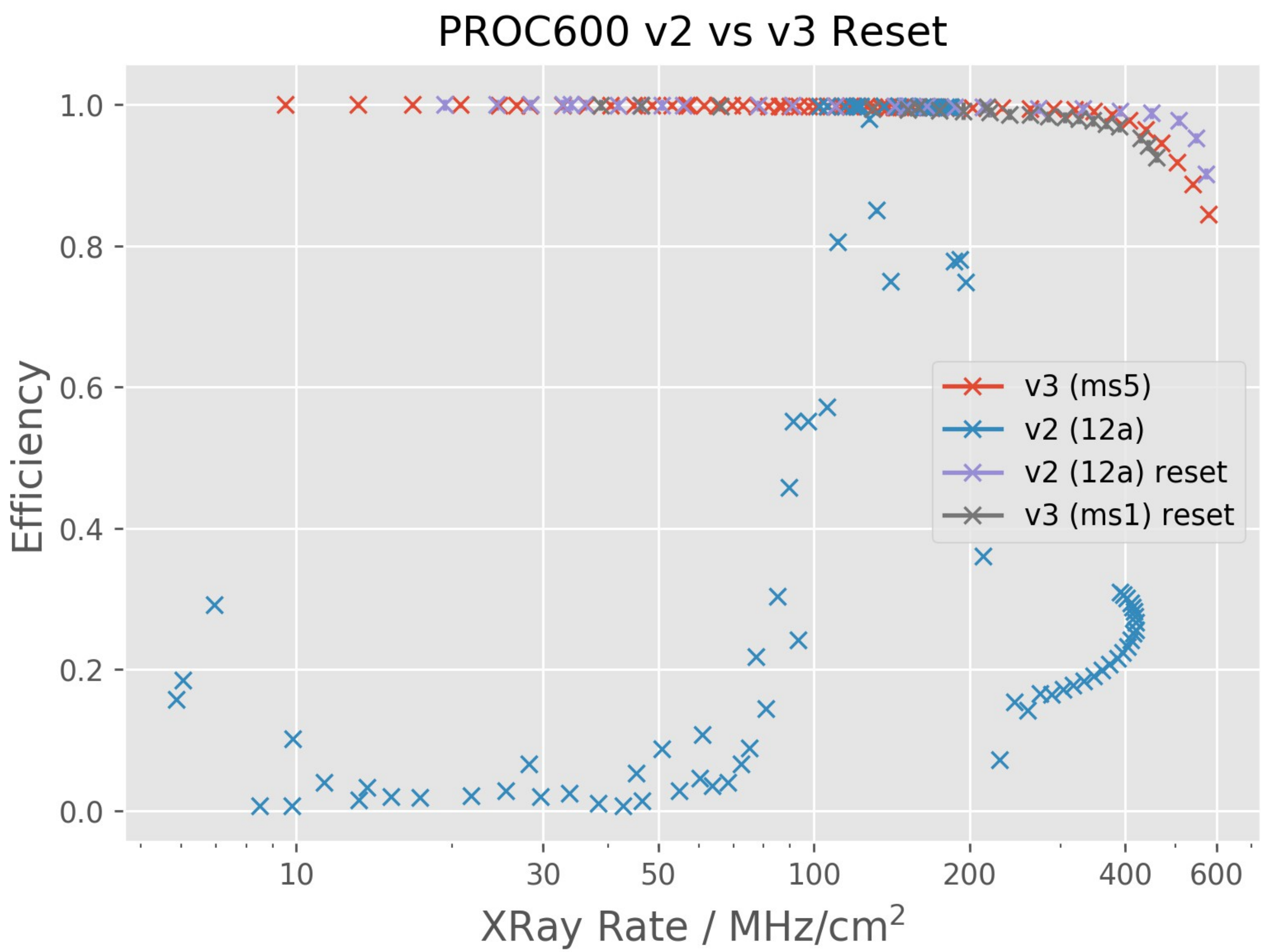
high rate
inefficiency

low rate inefficiency

V3 fully efficient until 400MHz X-ray rate (~800MHz pion rate)

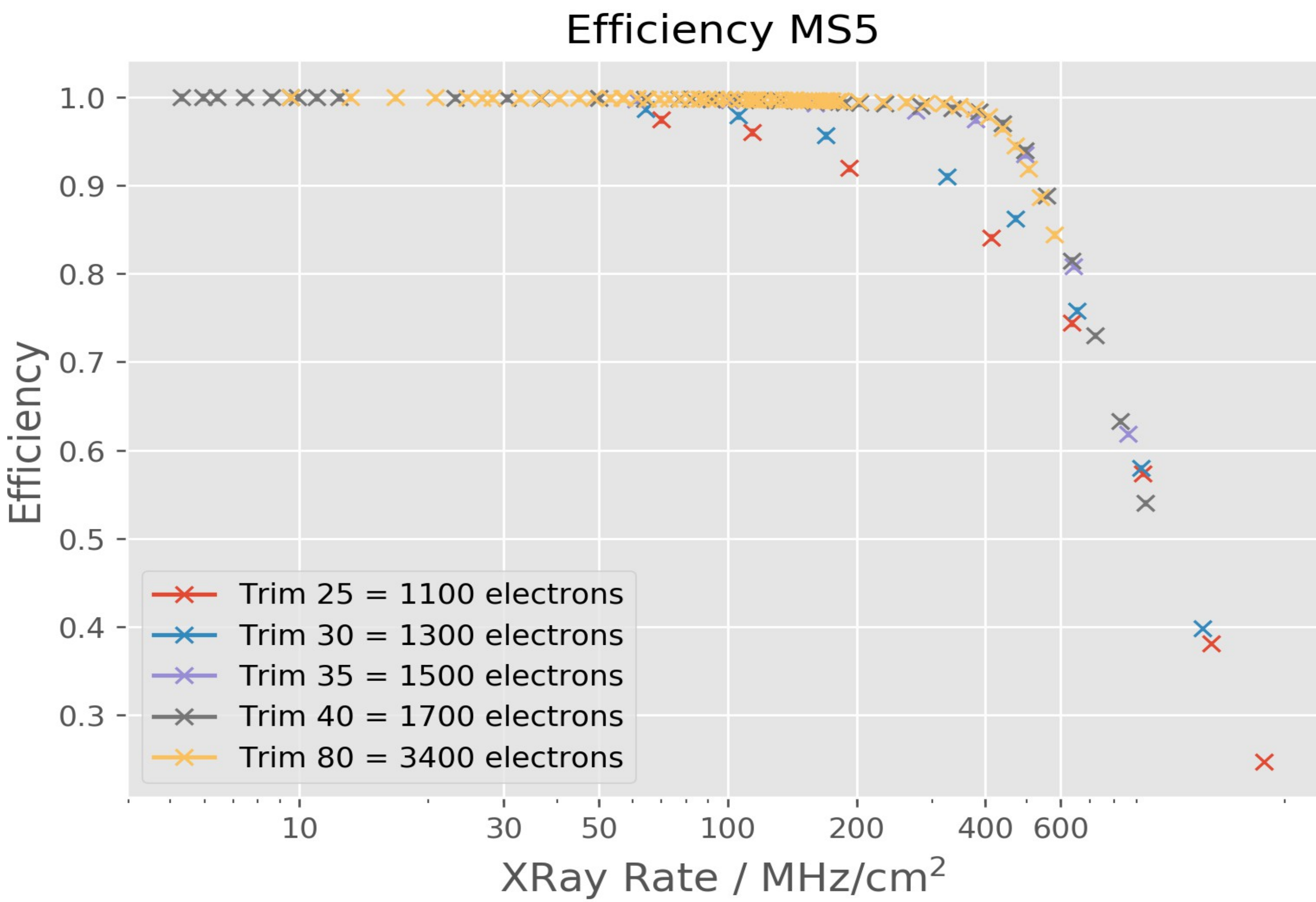
How could we every take data with V2?

With a reset before each trigger



In CMS we run with a 50 Hz reset rate.

Efficiency at different thresholds



Can be operated at full efficiency until 400MHz at 1500 electron threshold.
Should be good enough for CMS operation!

Plans for 2019-2020

Hans-Christian wants to make a few more improvements and resubmit the PROC.
V4 should come back sometime in March 2019.

We are buying new sensors and HDIs.
150 new layer-1 modules will be build in 2019 (we need ~100).

The new Layer-1 will be tested ad assembled at PSI at the beginning of 2020 and than transported to CMS/CERN in spring.

To be installed into CMS after summer 2020.
In parallel we will repair the broken modules in layers 2-4
and replace, yet again, all DCDC converters.

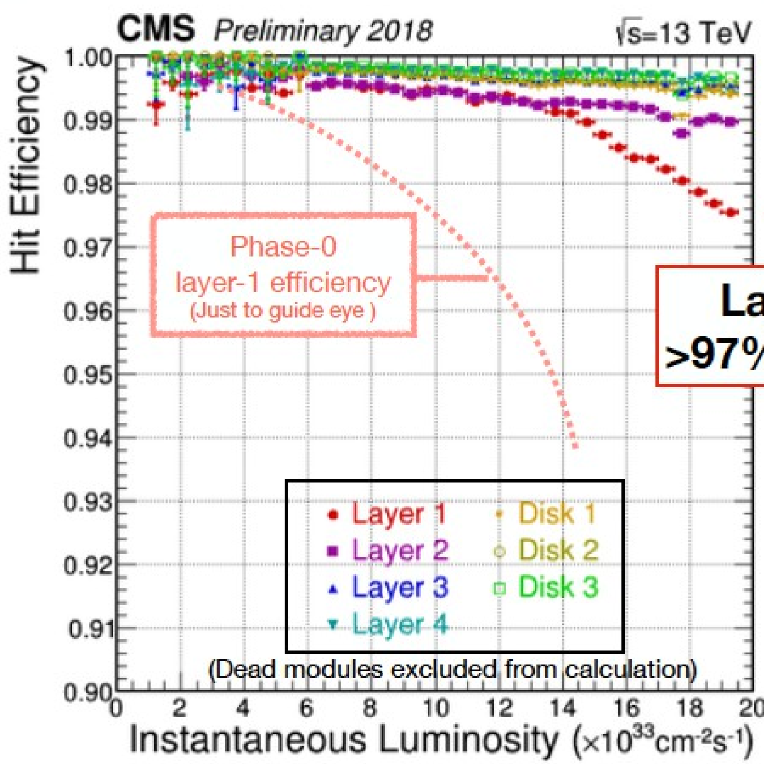
We hope to have a perfect pixel detector for Run-3 of LHC in 2021-23.

But still a lot of work for 2019-2020.

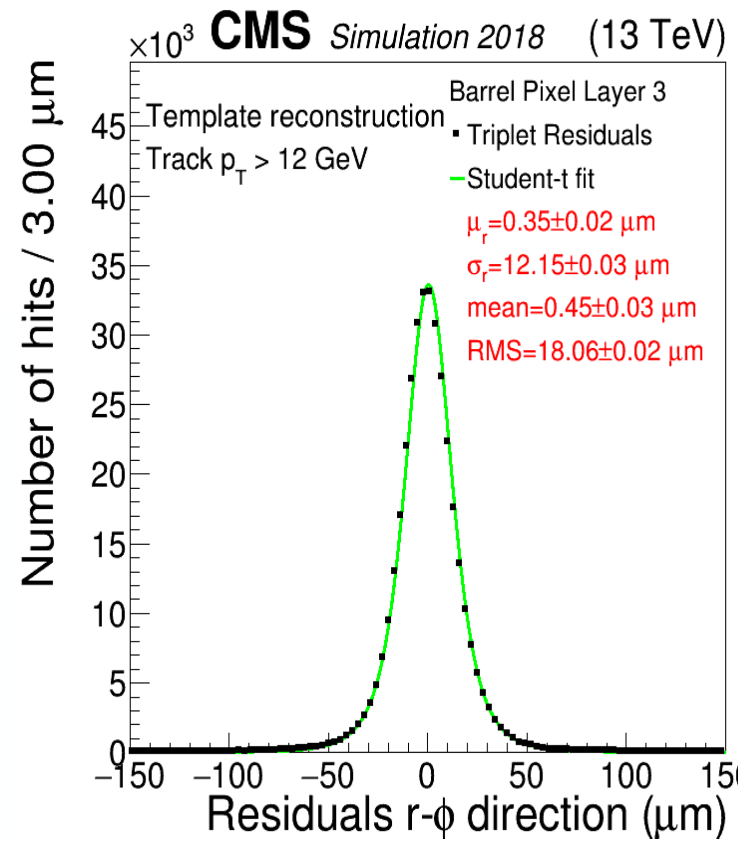
Nevertheless the detector performs very well.

The Resolution is < 12µm

Efficiency is much better than with the phase-0 detector



Layer-1 modules >97% at 2x10^{34}cm^{-2}s^{-1}



Fast readout system of phase-1 detector successfully maintains hit efficiency for instantaneous luminosity of this run-2 period.

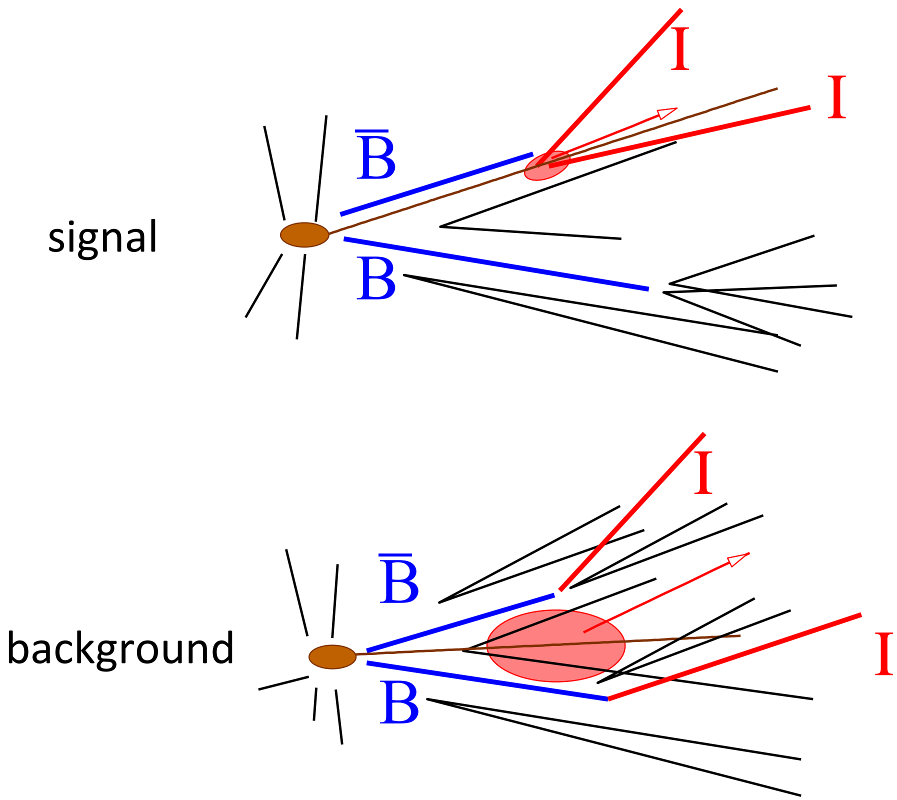
like in phase-0

The END
Thank You

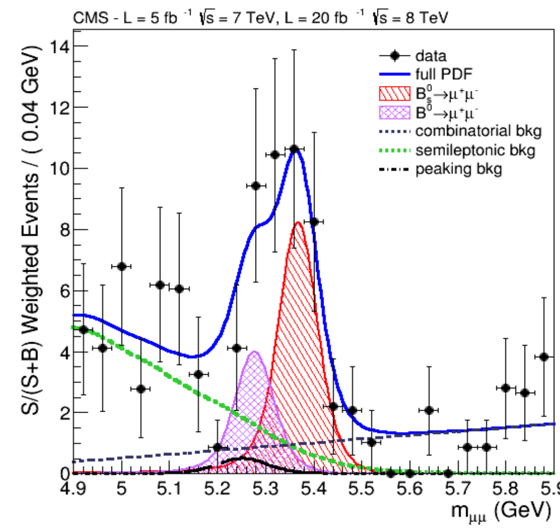
Bs➔μμ Analysis

Pixel detector essential for discrimination of signal versus background.

This decay is strongly suppressed in the Standard Model

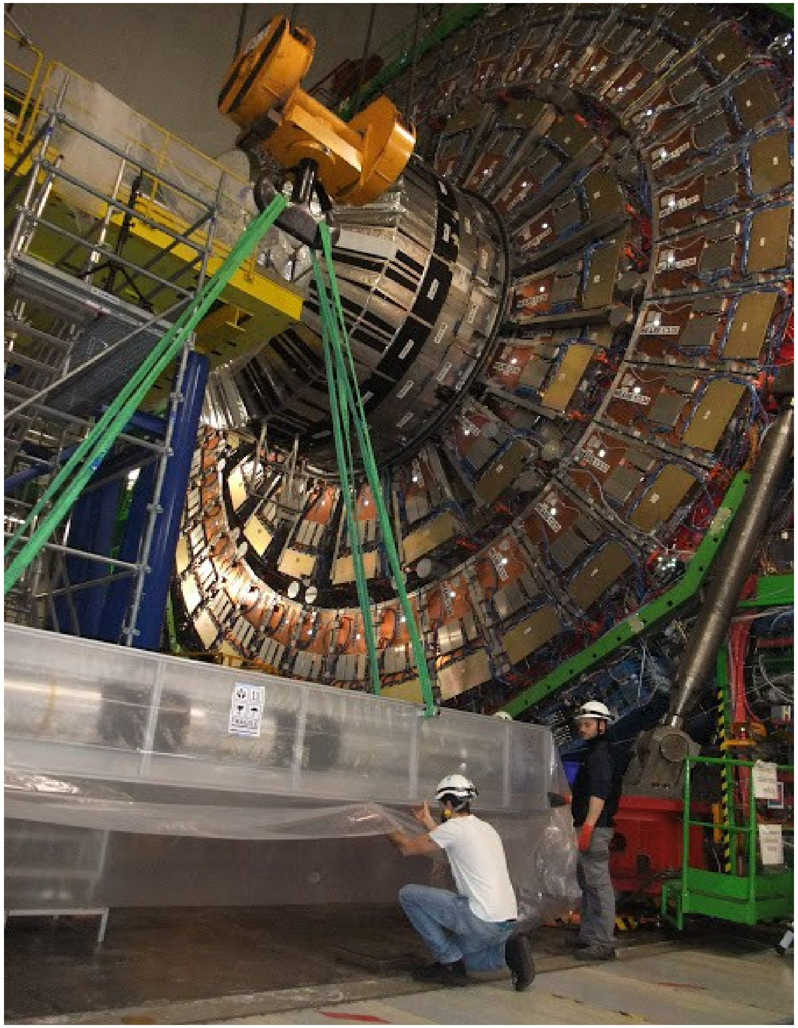


Results

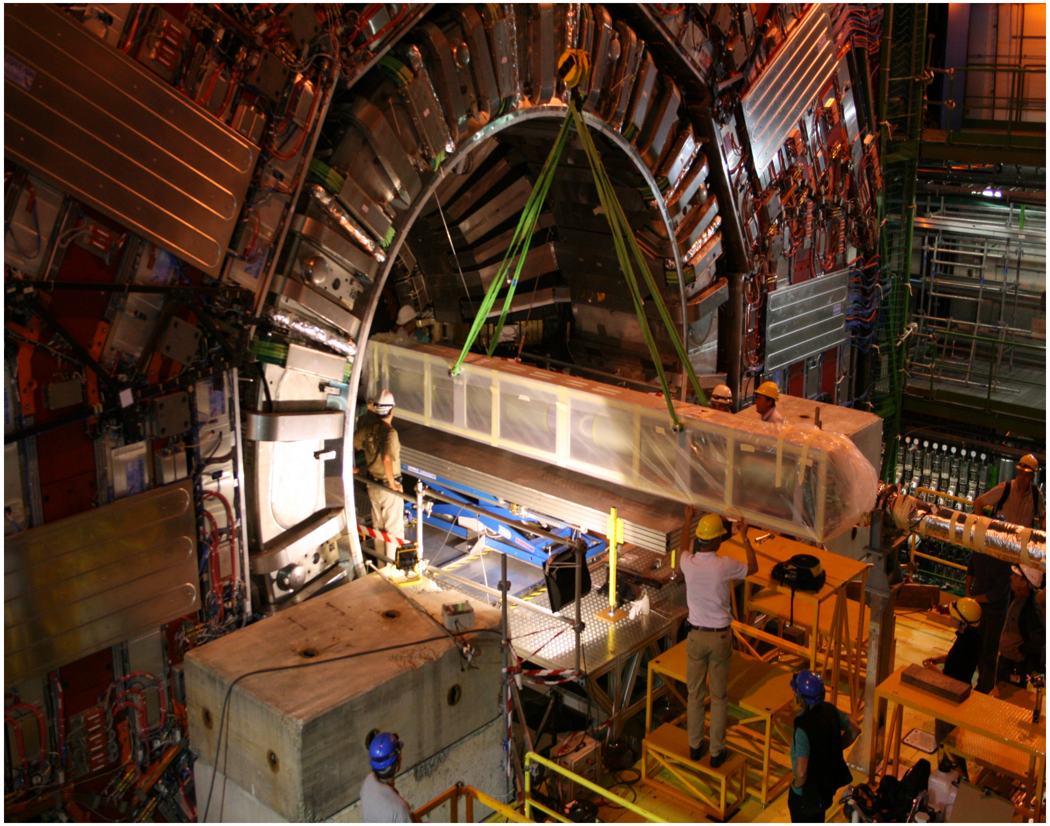


BF(B0➔μμ) < 1.1 × 10-10 (at 95%)
(Phys. Rev. Lett. 111 (2013) 101803)
Consistent with the SM predictions.

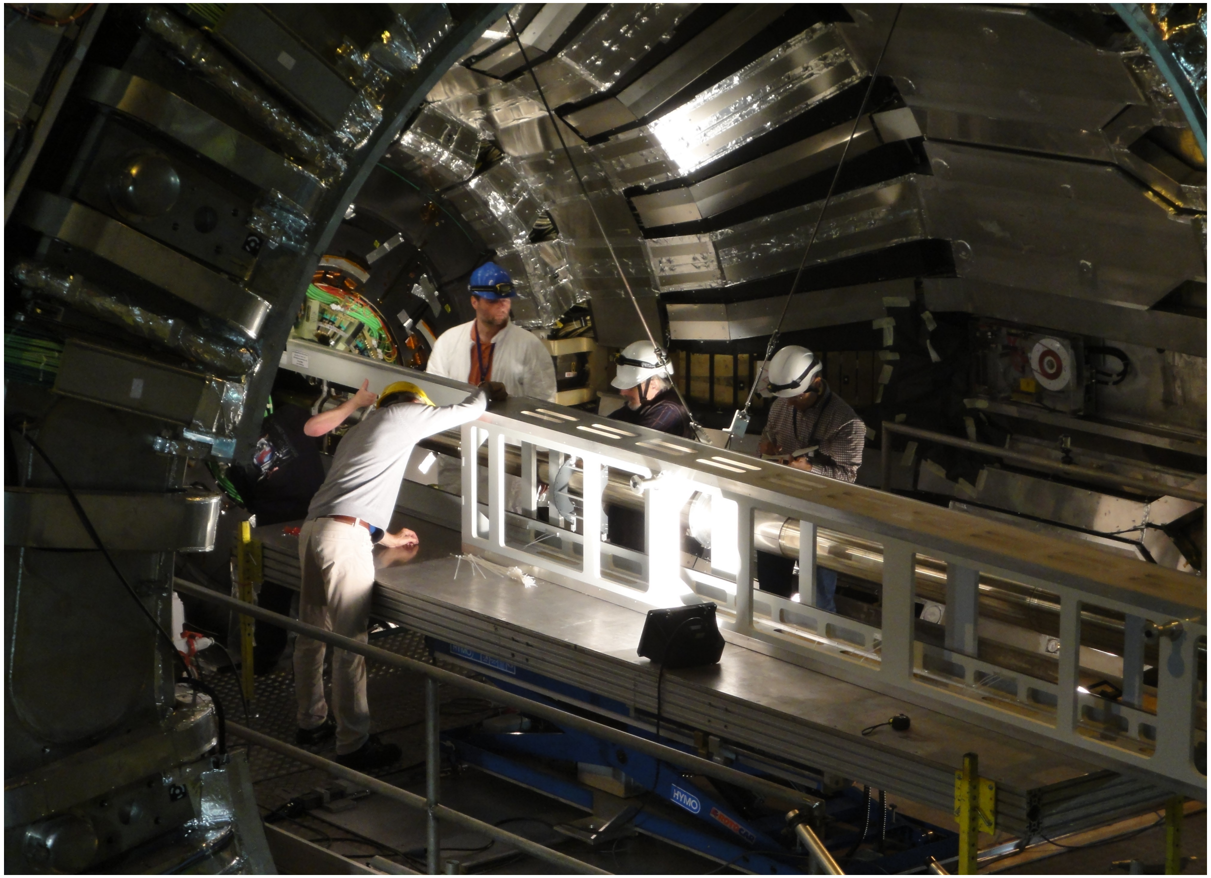
<u>Analysis lead by the PSI group</u>.
Performed using the CMS/CH T3 computing center located at PSI.



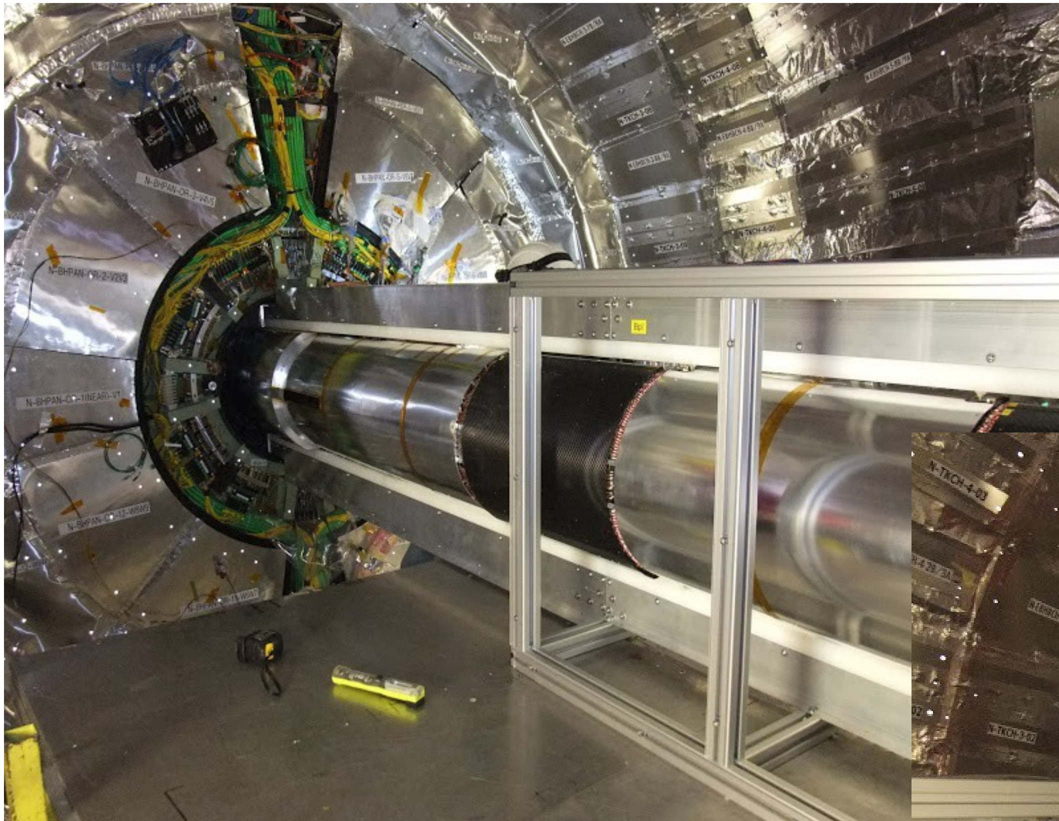
Preparations to install



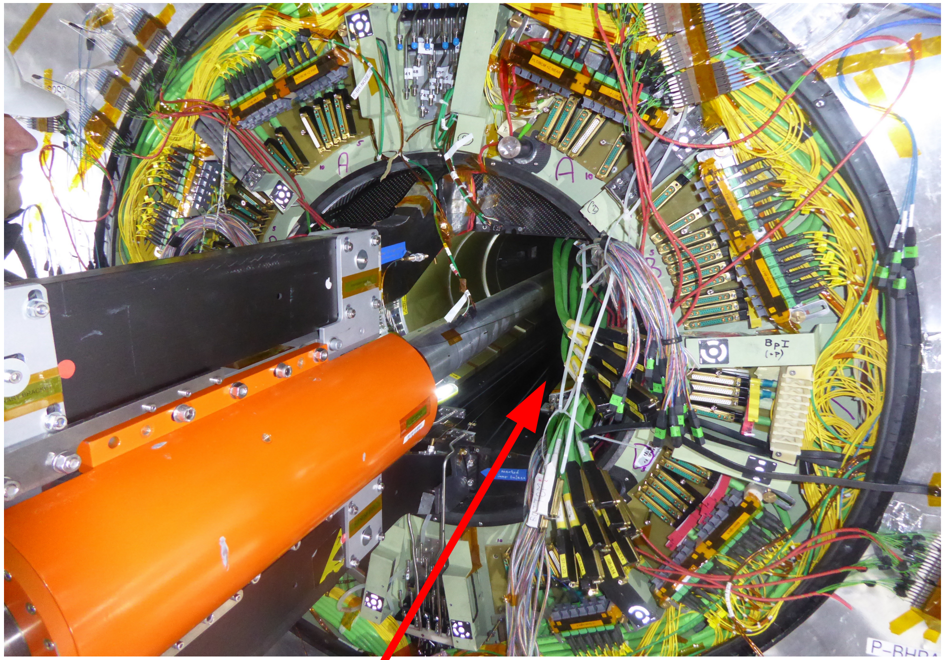
Installation of the pixel detector



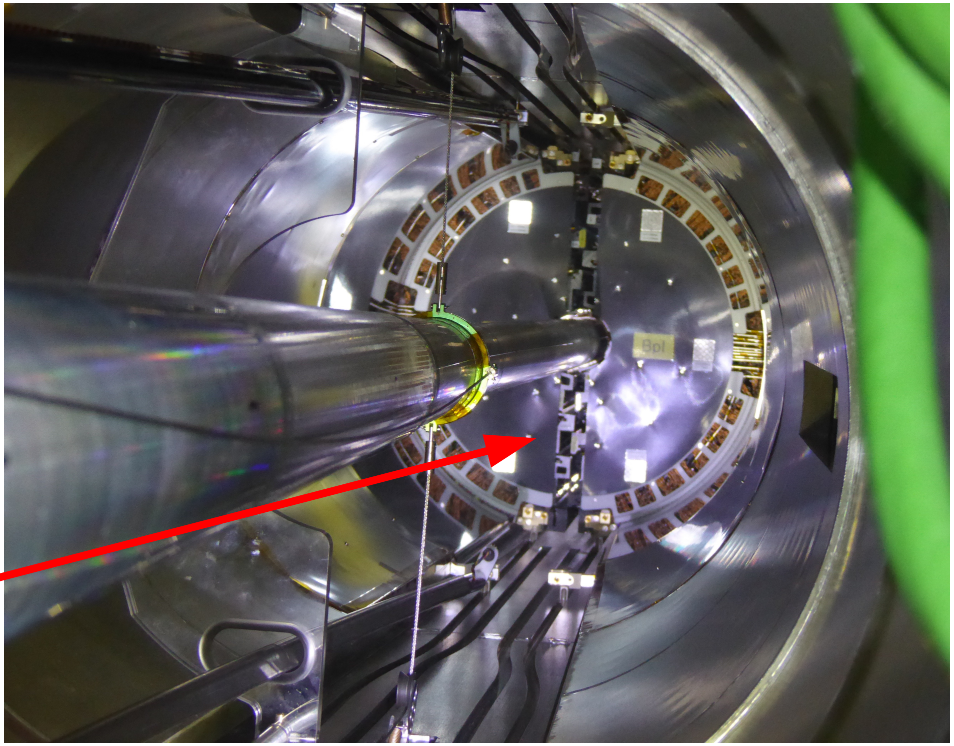
Installation of the pixel detector



BPix re-insertion



BPix has been re-inserted on 12/2
Cooling, cables & fibers attached on 13/2
Testing ongoing at +17deg.

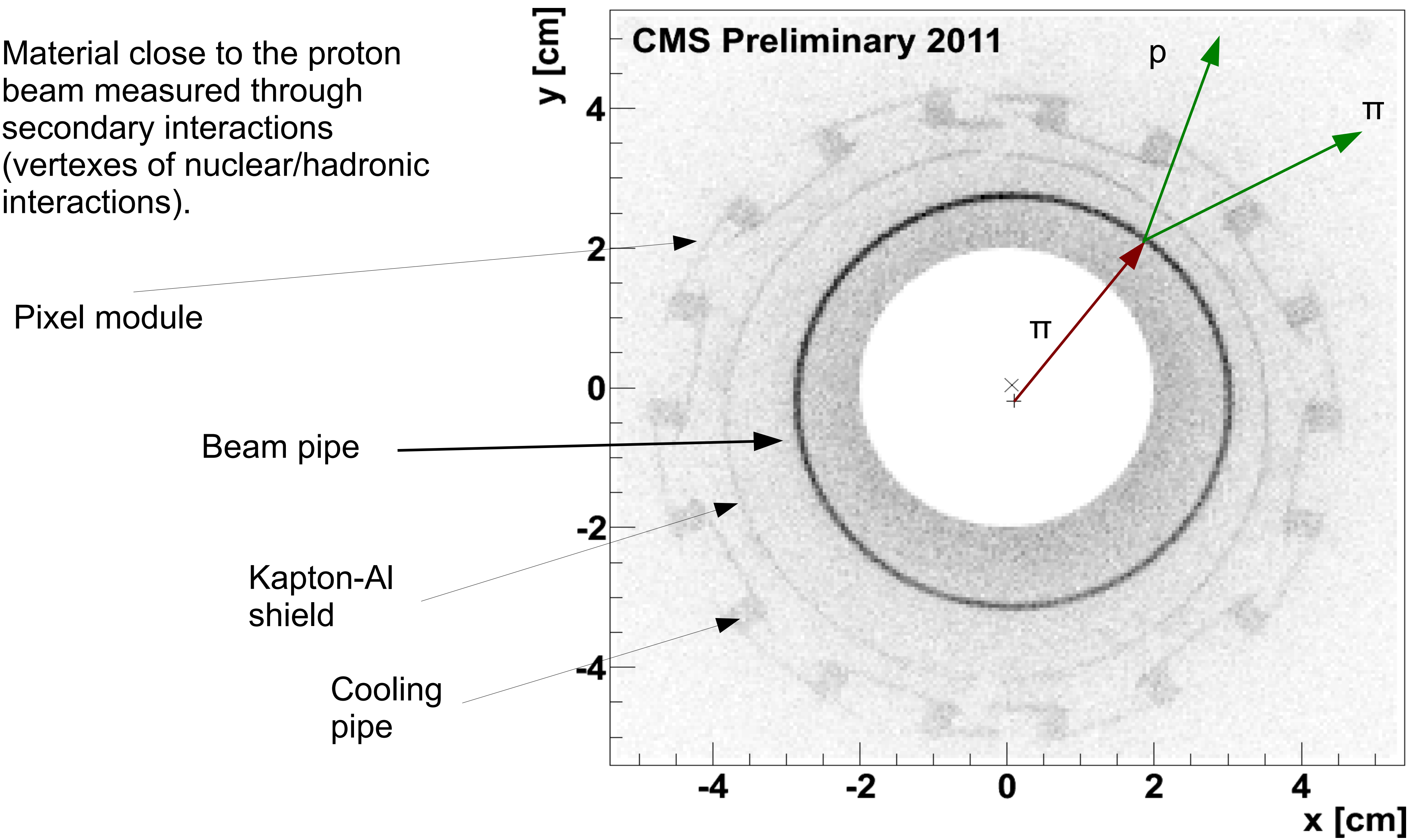


After insertion, tubes, cables
& fibers are not yet connected.

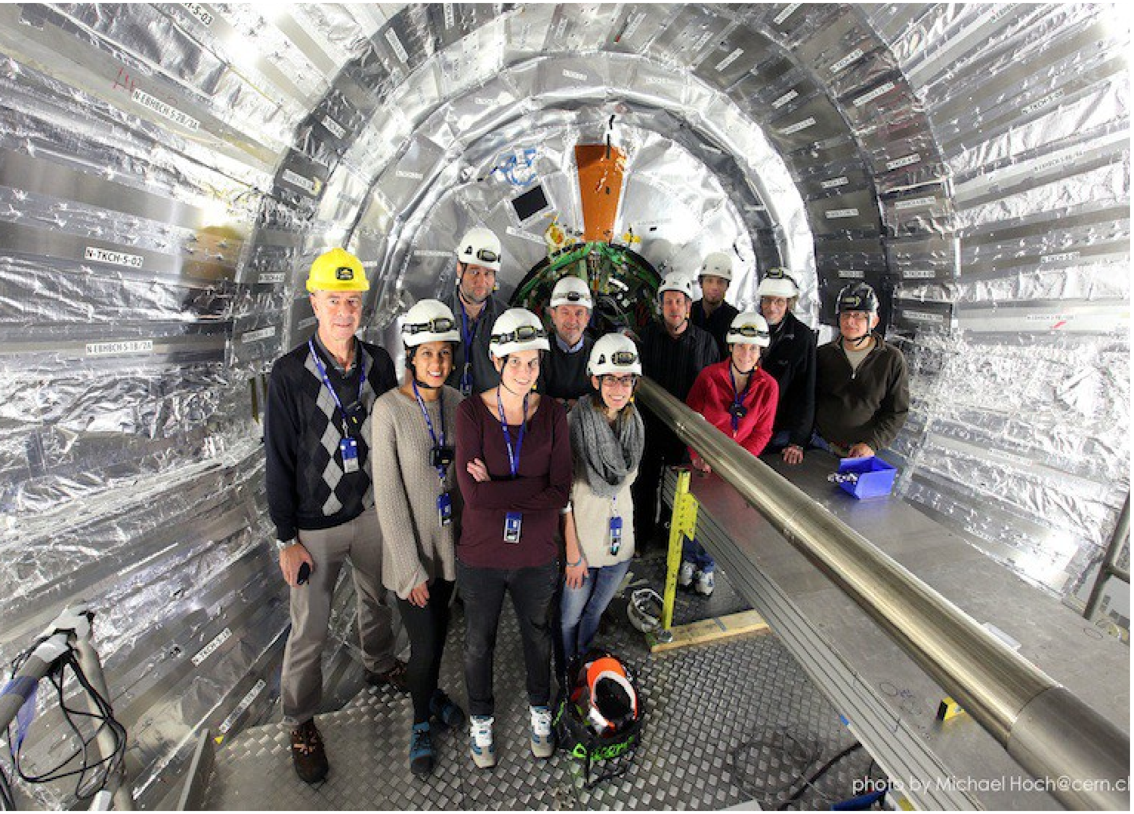
Two BPix half-shells
during the “closing” procedure
using 2m long “screwdrivers”.

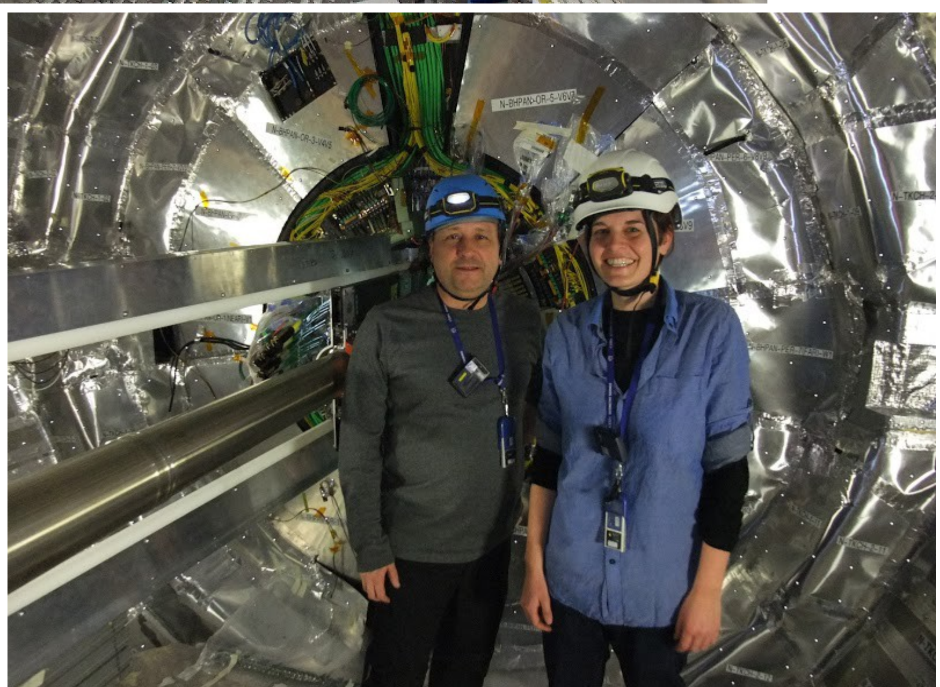
Detector Performance

Material close to the proton beam measured through secondary interactions (vertexes of nuclear/hadronic interactions).



Some happy moments!





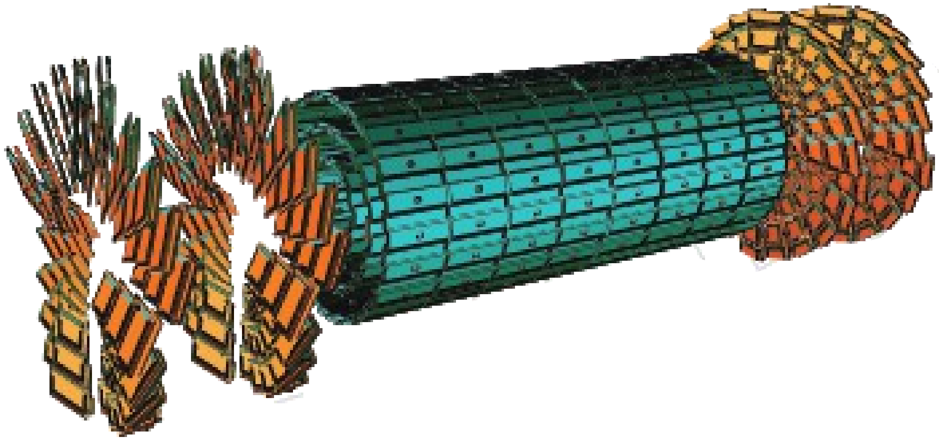
2008

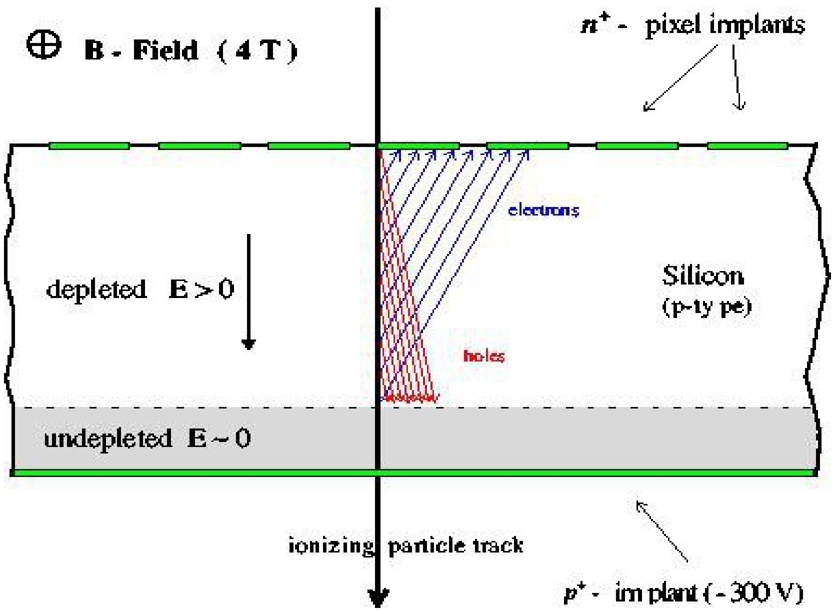
2017

CMS Pixel Detector

The only detector with **analog readout,** and almost square pixels.
Smaller than Atlas but still fully hermetic.

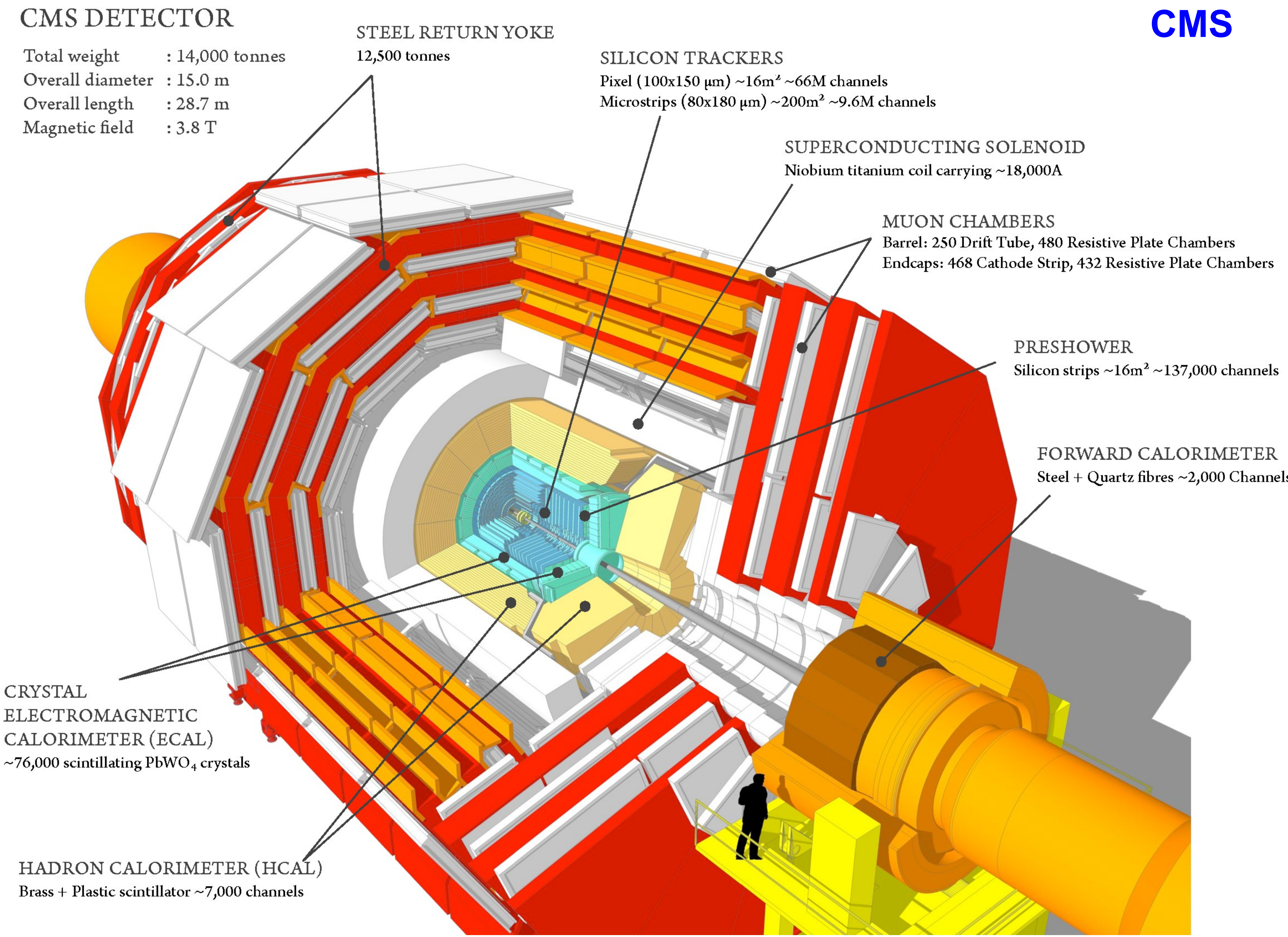
Build to allow quick extraction and insertion.
It needs about **1 week** to take it out and put back in (Atlas needs a few months).
There is a catch, CMS needs 3 weeks to open the detector to allow pixel access.
C6F14 cooling, presently running at 7degC.





Make use of the large charge drift in Magnetic field (Lorenz angle) to enhance the charge sharing and therefore the position resolution.

Therefore CMS can use <u>almost square pixels 100 * 150 μm^2</u>


CMS DETECTOR
Total weight : 14,000 tonnes
Overall diameter : 15.0 m
Overall length : 28.7 m
Magnetic field : 3.8 T
STEEL RETURN YOKE
12,500 tonnes
SILICON TRACKERS
Pixel (100x150 μm) ~16m² ~66M channels
Microstrips (80x180 μm) ~200m² ~9.6M channels
SUPERCONDUCTING SOLENOID
Niobium titanium coil carrying ~18,000A
MUON CHAMBERS
Barrel: 250 Drift Tube, 480 Resistive Plate Chambers
Endcaps: 468 Cathode Strip, 432 Resistive Plate Chambers
PRESHOWER
Silicon strips ~16m² ~137,000 channels
FORWARD CALORIMETER
Steel + Quartz fibres ~2,000 Channels
CRYSTAL ELECTROMAGNETIC CALORIMETER (ECAL)
~76,000 scintillating $PbWO_4$ crystals
HADRON CALORIMETER (HCAL)
Brass + Plastic scintillator ~7,000 channels
CMS