The Mu3e Data Acquisition System

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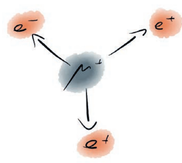
Abstract

The Mu3e Experiment at PSI is designed to search for the lepton-flavour violating decay of a positive muon to two positrons and an electron with an ultimate sensitivity of one in 10^{16} muon decays. The detector is based on ultra-thin high-voltage monolithic active pixel sensors combined with scintillating fibres and tiles for precise timing measurement. Already in the first phase of data taking with up to 10^8 muon stops/s, the detector will produce about 60 Gbit/s of raw data. We present the Mu3e data acquisition system, which transports these data out of the detector, time-sorts them and searches for interesting signatures by performing a full track and vertex reconstruction using graphics processing units (GPUs).

Mu3e Experiment

- Search for Lepton Flavour Violation in the decay $\mu \to eee$
- Standard Model BF < 10^{-54}: Observation clear sign of new physics
- Current limit: BF < 10^{-12}; SINDRUM, 1988
- Mu3e Phase I: Aimining for $O(10^{-15})$ sensitivity at the exsiting πE5 beamline: 10^8 μ/s
- Mu3e Phase II: Aimining for $O(10^{-16})$ sensitivity at a new high-intensity muon beamline (HiMB): >10^9 μ/s

Signal

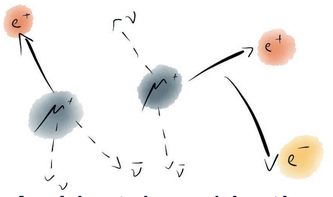


Two positrons, one electron from a common vertex
$\Sigma P_e = (m_\mu, 0)$

Need excellent momentum, vertex and timing resolution

Background

SM process
$\mu \to eeevv$
Missing momentum carried by the neutrinos



Accidental combinations of Michel decays with Bhabha scattering or γ conversion

1T magnetic field
Helium atmosphere for cooling and minimal multiple scattering

Long tube design: detect particles recurling in the field to improve momentum resolution

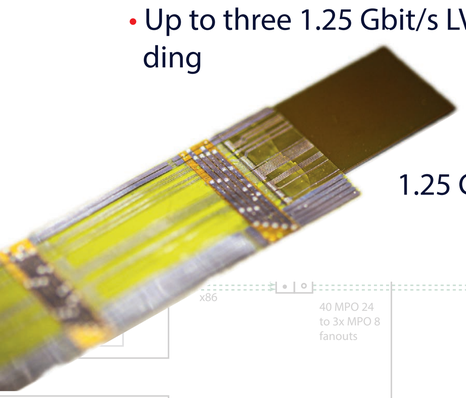
PSI muon beam, up to 10^8 μ-stops/s

Hollow double cone
Mylar stopping target

Pixel detector

High-Voltage Monolithic Active Pixel Sensors (HV-MAPS)

- Commercial high-voltage CMOS technology
- ~ 85 V reverse bias: fast charge collection via drift: Time resolution below 6 ns σ
- Can be thinned to 50 μm: Minimize multiple scattering
- Per-pixel comparator and hit buffer: Zero-suppression
- Column-drain readout controlled by state machine
- Up to three 1.25 Gbit/s LVDS links with 8b/10b encoding



Pixel prototype mounted on aluminium-Kapton flexprint
1.25 Gbit/s readout and powering demonstrated

Fibre detector

250 μm scintillating fibres coupled to SiPM arrays

- MuTRiG readout ASIC
- High-resolution TDC
- Time and charge measurement
- SiPM biasing
- Zero-suppressed digital readout via 1.25 Gbit/s 8b/10b encoded link

< 500 ps timing resolution demonstrated

Tile detector

$0.5 \times 0.5 \times 0.5$ cm³ scintillating tiles coupled to SiPMs

- MuTRiG readout ASIC

< 70 ps timing resolution demonstrated

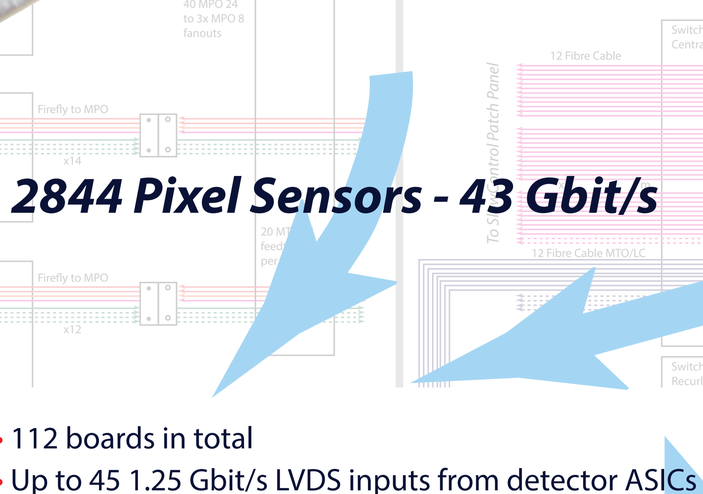
2844 Pixel Sensors - 43 Gbit/s

3072 Fibre Readout Channels 26 Gbit/s

5824 Tiles - 12 Gbit/s

Front-end board

- 112 boards in total
- Up to 45 1.25 Gbit/s LVDS inputs from detector ASICs
- < 10 ps jitter clock distribution to ASICs
- Confiuration and control of ASICs
- Data alignment and time sorting
- Needs to operate in magnetic field and helium

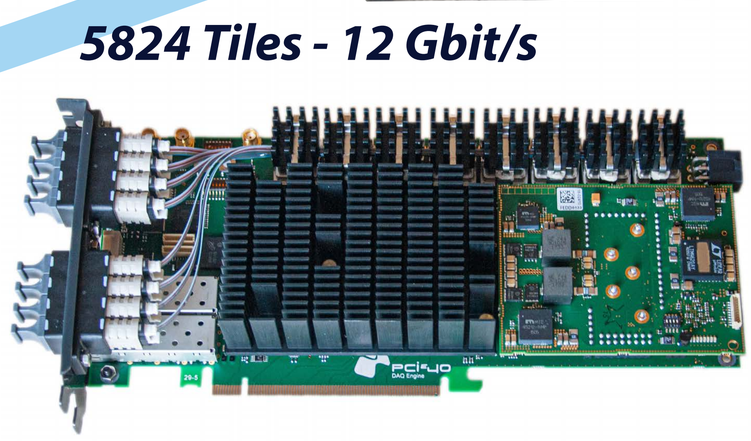


Prototype based on Altera/Intel Stratix IV FPGA
Production version with Intel Arria V FPGA, small form factor; Layout being completed

Optical Links

- All communication out of the detector optical
- 6 Gbit/s fibre links
- Use Samtec Firefly Transceivers (4 Tx/4 Rx), small form factor (detector side), Avago MiniPODs outside
- Links for data, configuration, clock and reset
- ~ 50 m to counting house

Switching Boards



- PCIe40 board developed at CPPM Marseille for LHCb and ALICE
- 48 fibre Tx/Rx
- Intel Arria 10 FPGA
- Two PCIe 3.0 8-Lane interfaces to PC
- Align data, forward to filter farm
- Detector configuration

MIDAS

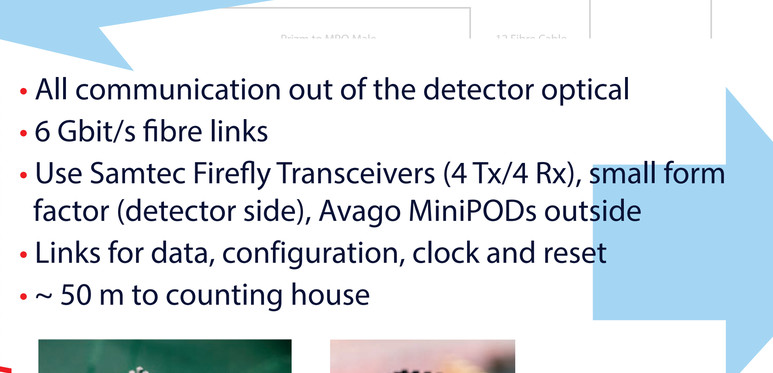
- Maximum Integrated Data Acquisition System
- PSI/TRIUMF Development
- Control of the DAQ system
- Collect up to 100 MB/s data and safe to PSI/CSCS Petabyte archive
- Web-based user interface

Filter Farm PCs

- Up to 160 GB/s input bandwidth (16 10 GBit/s optical links)
- Commercial Terasic DE5aNet board
- Intel Arria 10 FPGA
- 8 GB DDR4 buffer memory
- PCIe 3.0 8-Lane interface to PC
- Data buffering, coordinate transformations, hit combinatorics

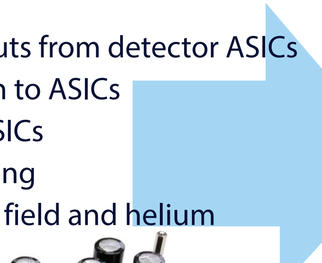
- High-performance graphics card (GPU)
- Perform track- and vertex-fit searching for $\mu \to eee$
- New track fit for multiple scattering dominated environment: 10^9 3D track-fits/s on a single GPU

Slice Tests



Clock & Reset

- Distribute 144 copies of the 125 MHz clock optically
- < 10 ps jitter
- Resets and state changes via 144 1.25 Gbit/s links
- Built by UCL
- Full system operational



www.psi.ch/mu3e