PAUL SCHERRER INSTITUT

PSI

Frank Herzog :: Electronics Engineer :: Paul Scherrer Institut

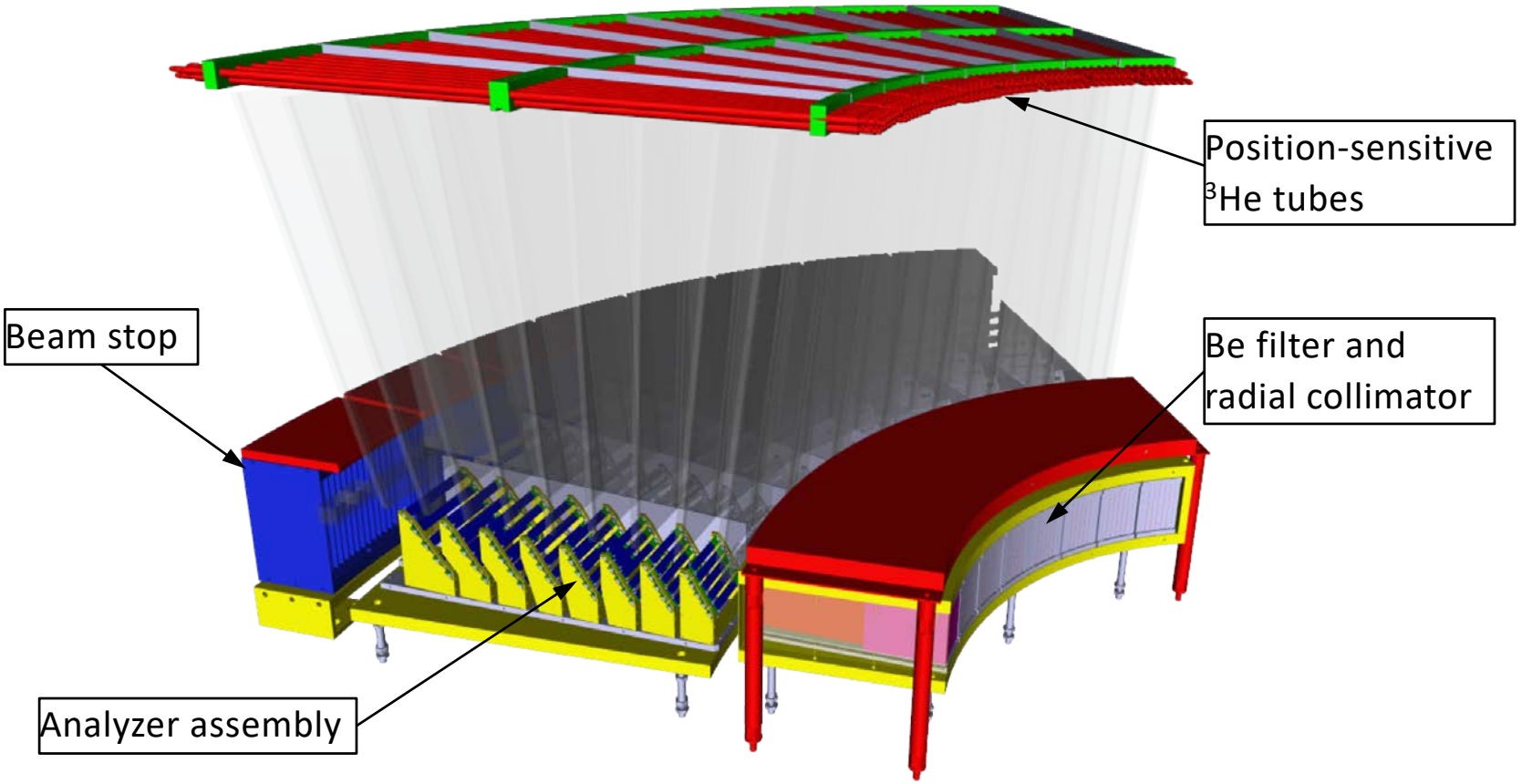
Frontend Electronics Design for the CAMEA Instrument

LTP Seminar, 23.09.2019

Content

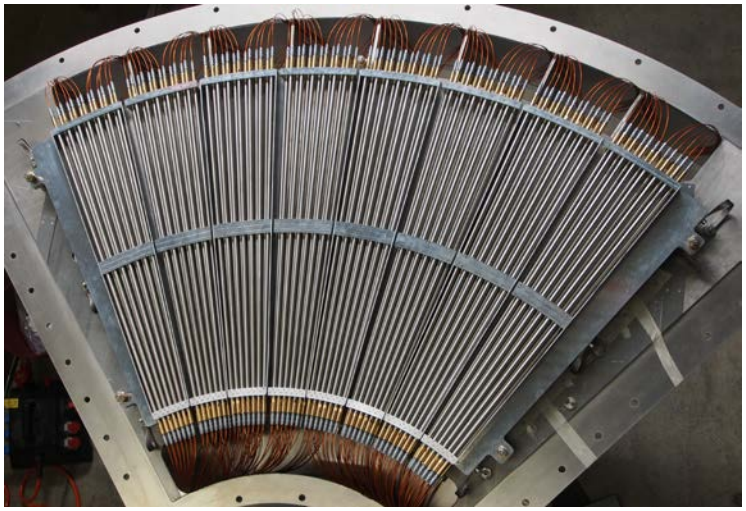
- CAMEA instrument introduction
- The CAMEA frontend electronics
- MORPHEUS tests
- Instrument commissioning

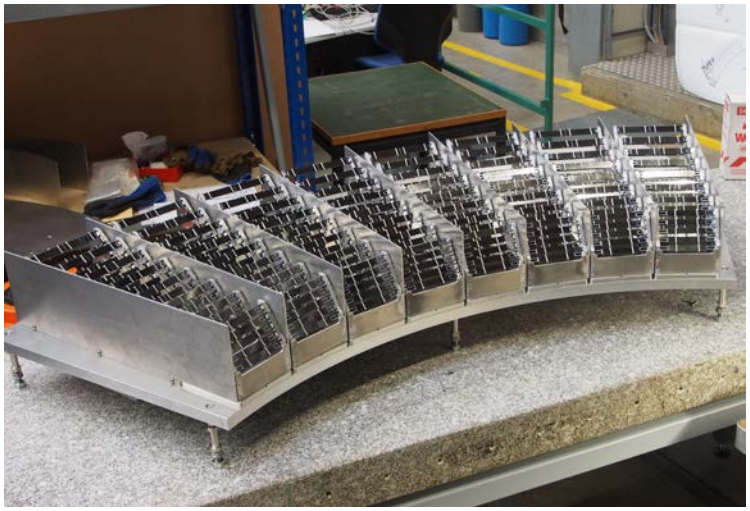
Instrument concept



- CAMEA: Continuous Angle Multiple Energy Analysis
- Groitl, F. et al. *CAMEA – A novel multiplexing analyzer for neutron spectroscopy*, Rev. Sci. Instruments 87

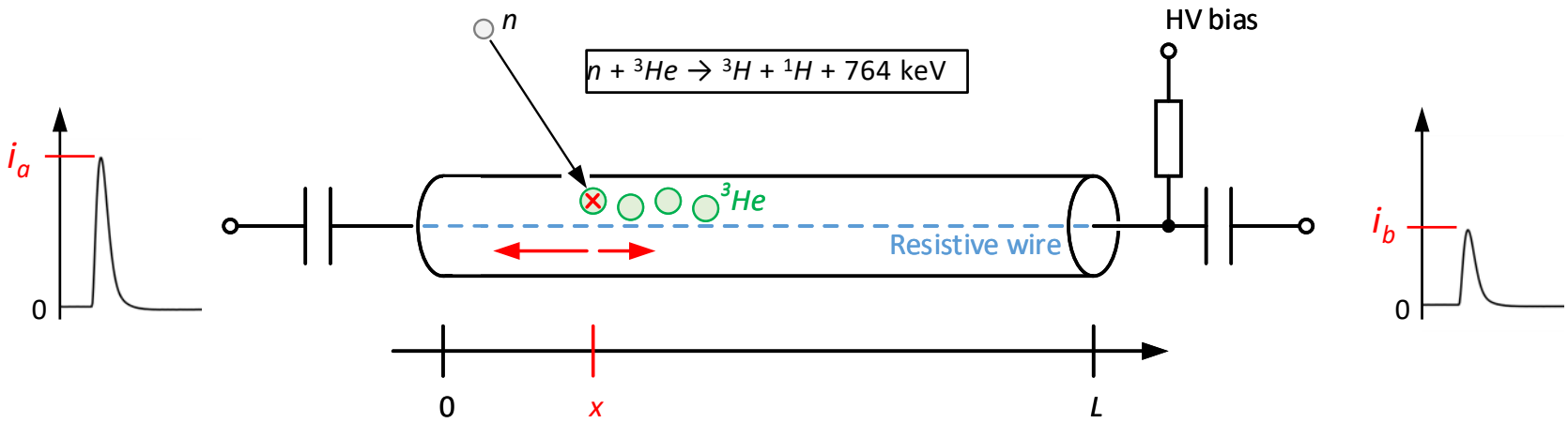
CAMEA instrument overview





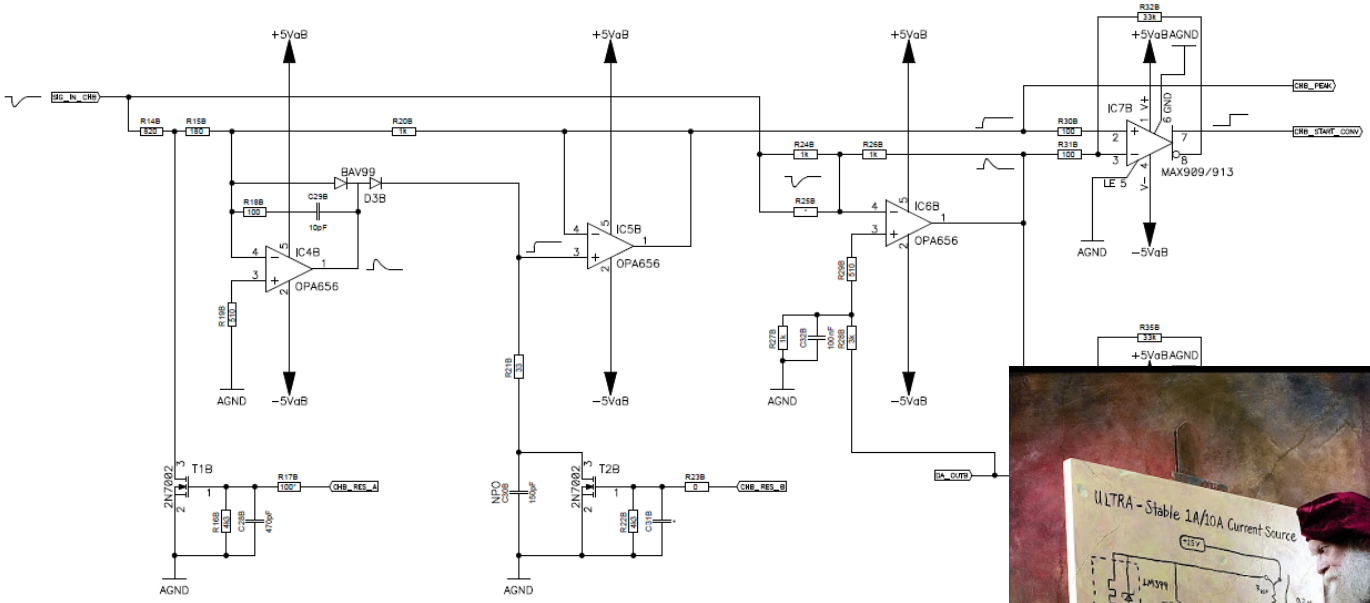
Detector readout

- 104 position sensitive (charge-division) ^{3}He neutron detector tubes
  → 208 analog acquisition channels
- Pulse event duration < 100 ns



$$x \approx \frac{i_b}{i_a + i_b}$$

Use existing PSI electronics?



- Analog track-and-hold, peak detection, etc.
- Proven performance but:
  - Many discrete components, low integration density
  - Hardwired trigger levels, filter bandwidths, etc.

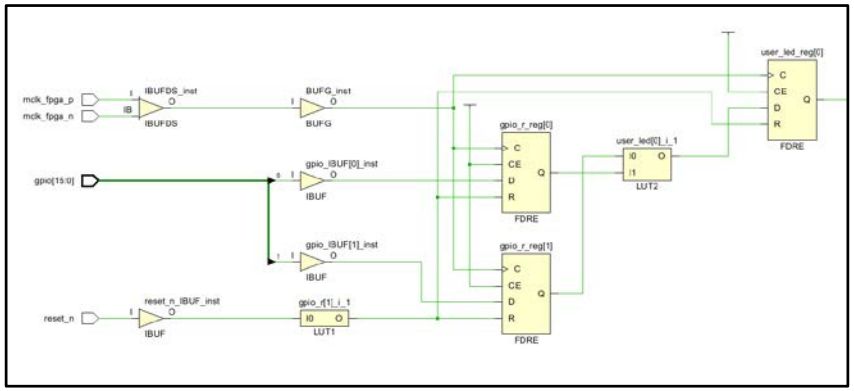
«My favourite programming language is solder»

...but then came FPGAs!

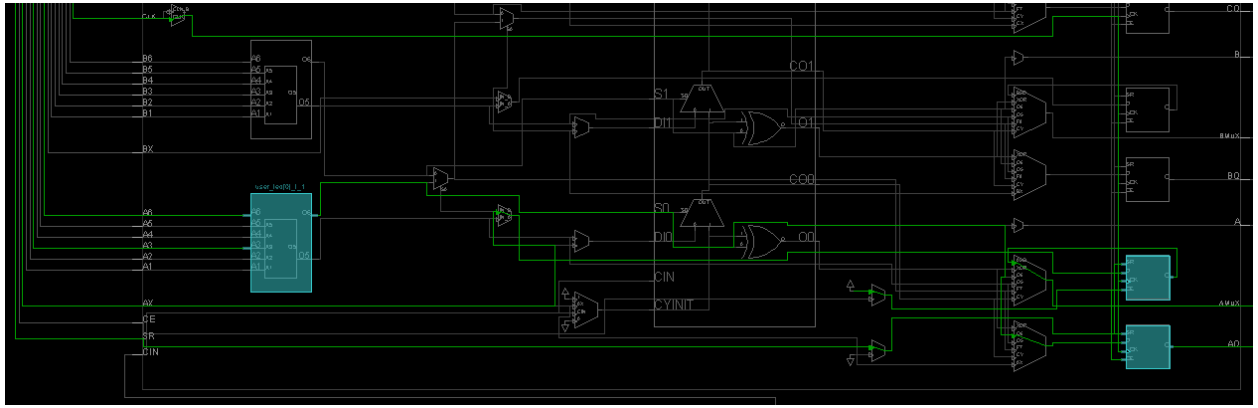
- FPGA: Field Programmable Gate Array
- VHDL: Very high speed integrated circuit Hardware Description Language

```
architecture rtl of simple_vhdl_top is

    signal mclk_fpga            : std_logic;
    signal mclk                 : std_logic;
    signal gpio_r               : std_logic_vector(15 downto 0);

begin

    process (mclk, reset_n) is
    begin
        if (rising_edge(mclk)) then
            if (reset_n = '0') then
                gpio_r          <= (others => '0');
                user_led        <= (others => '0');
            else
                gpio_r          <= gpio;
                user_led(0)     <= gpio_r(1) and gpio_r(0);
            end if;
        end if;
    end process;
```

Synthesis

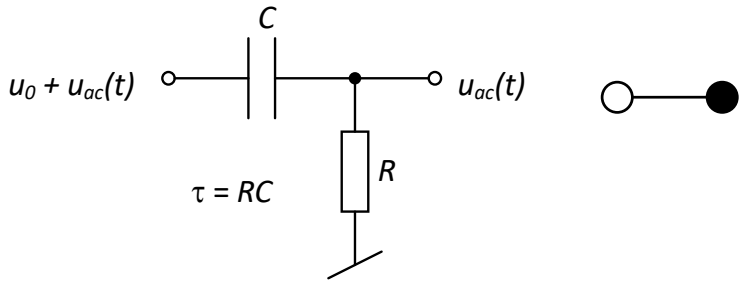


Place & Route



Configure

Digital Signal Processing (DSP) example



Offset-free output

Input

Internal state (offset)

$$y_{AC}(n) = u(n) - x(n)$$

$$x(n+1) = \frac{1}{M} \cdot \sum_{k=-\infty}^{n} y_{AC}(k)$$

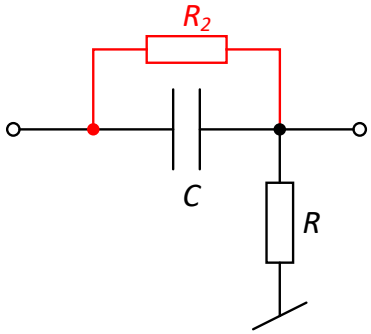
'Time constant'

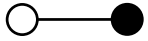
Accumulator

- Will probably need thousands of transistors in FPGA, but transistors are extremely small (28 nm gate width) → tiny footprint
- Programmable time constant M
- Provides additional offset information

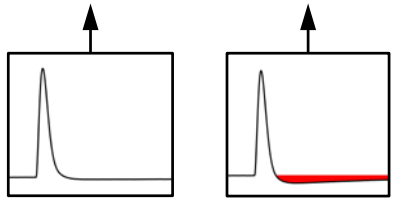
More examples...

Pole-zero cancellation

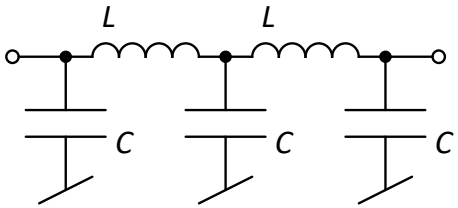


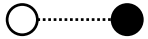


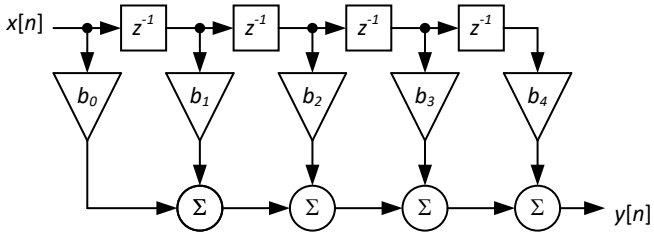
$$y'_{AC}(n) = y_{AC}(n) + \frac{1}{M_2} \cdot \sum_{k=-\infty}^{n} y_{AC}(k)$$



Filtering



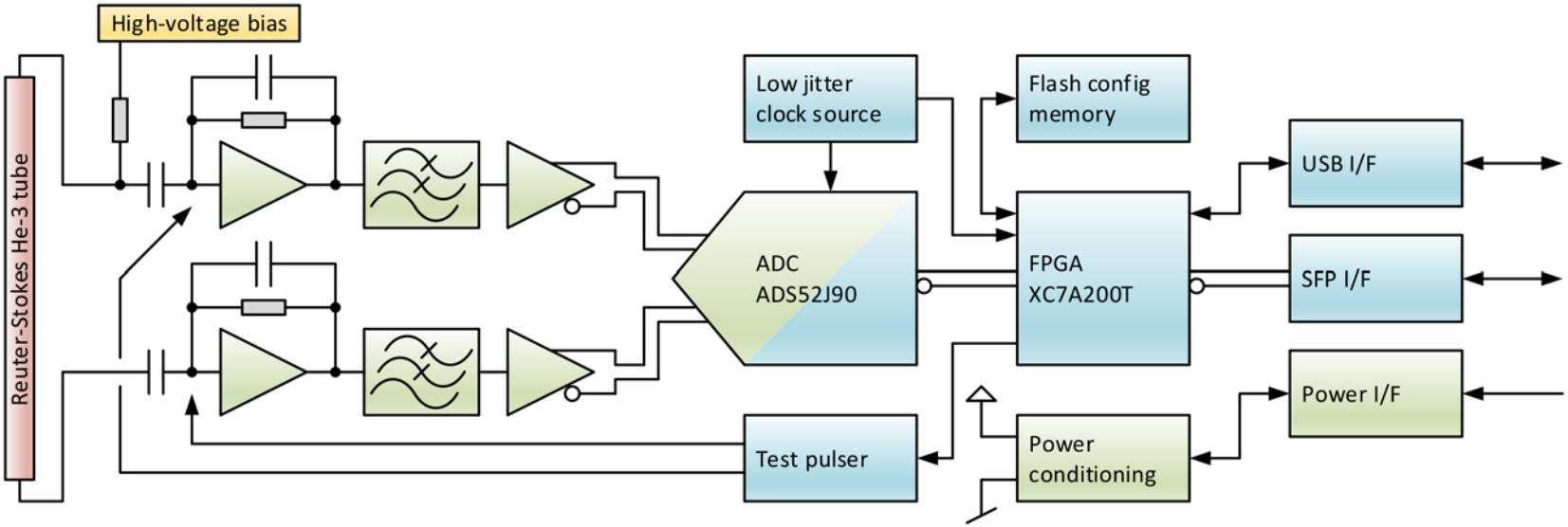




Division

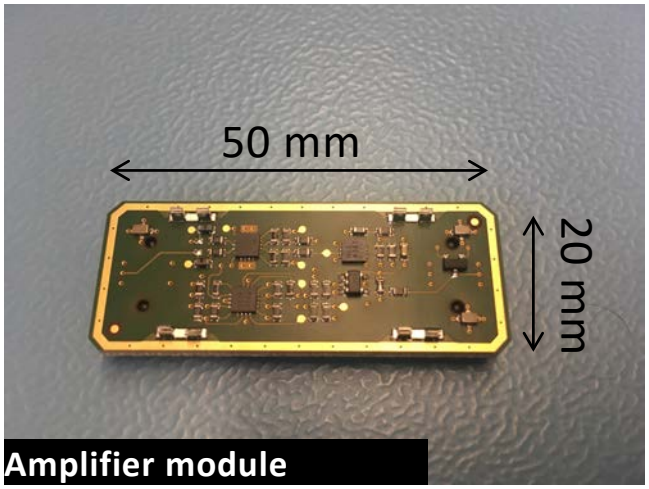
```
Q = 0;
while N ≥ D
   N = N-D;
   Q = Q+1;
end
```

CAMEA frontend electronics concept

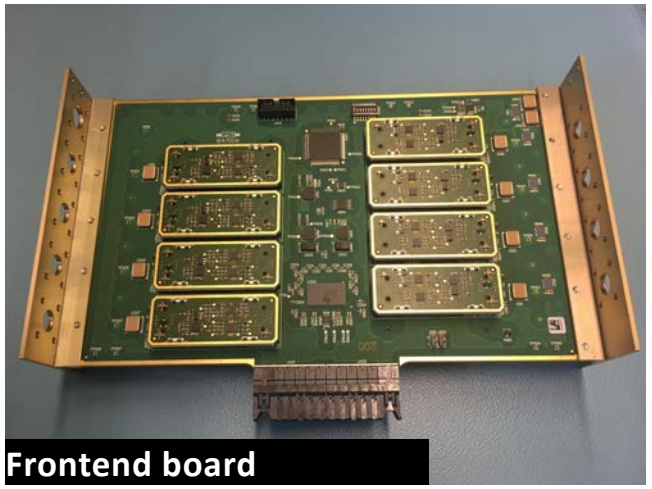


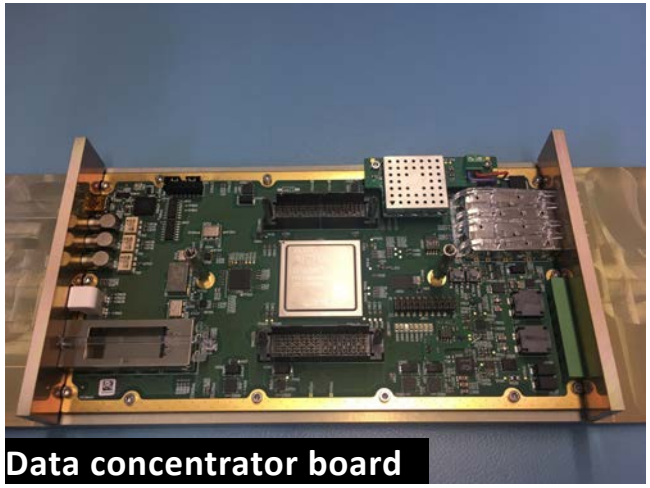
- Amplification
- Sampling
- Signal conditioning
- Pulse detection
- Pulse position calculation

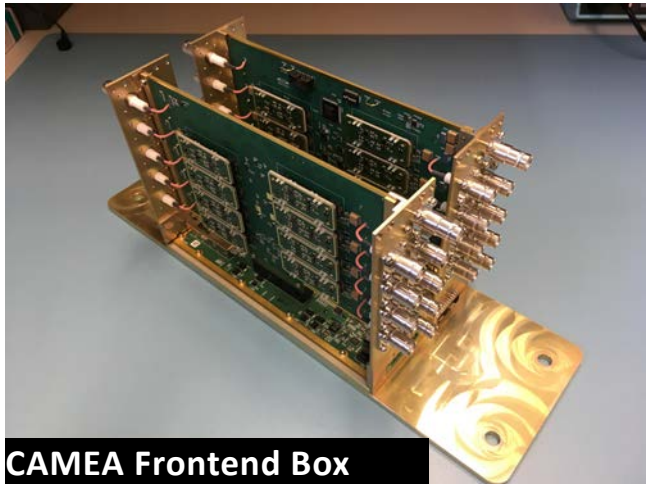
Frontend electronics hardware



Amplifier module


Frontend board

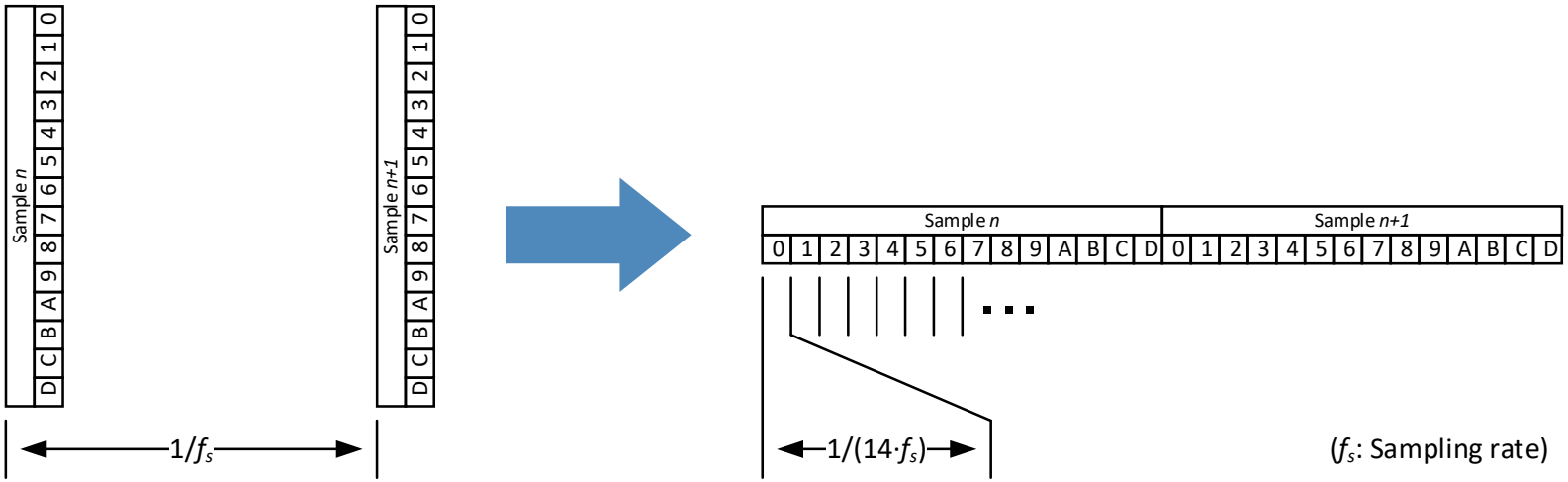

Data concentrator board


CAMEA Frontend Box

Integration density?

- 32 acquisition channels per box
- 32 ADCs
- 14 bit resolution per ADC
- 448 tracks
- 125 µm track width and clearance
- **→ 11 cm data bus width**

Serialization

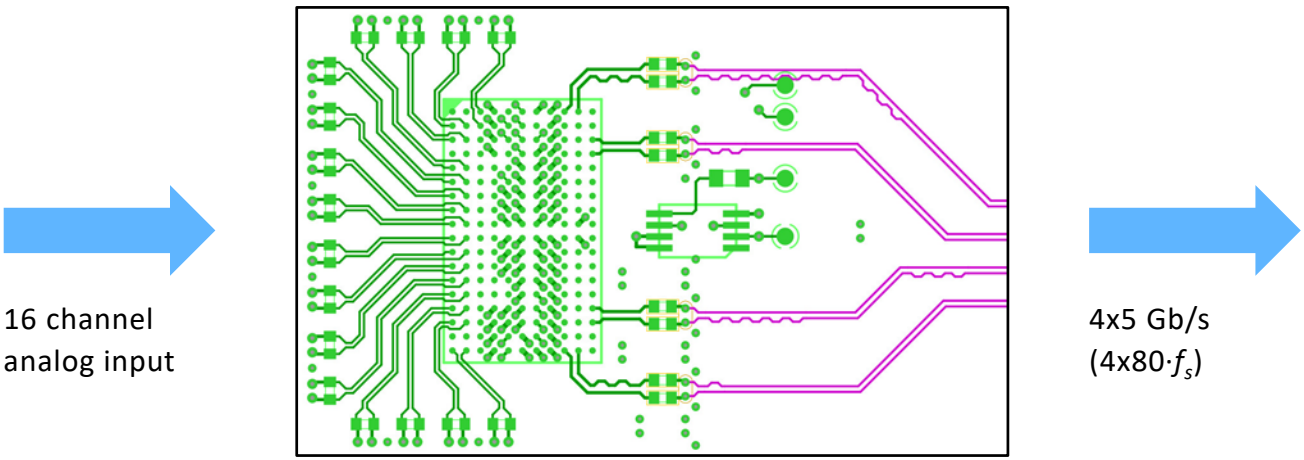


- 32 differential data lines
- 32 differential clock lines
- 128 tracks
- **Better, but still…**

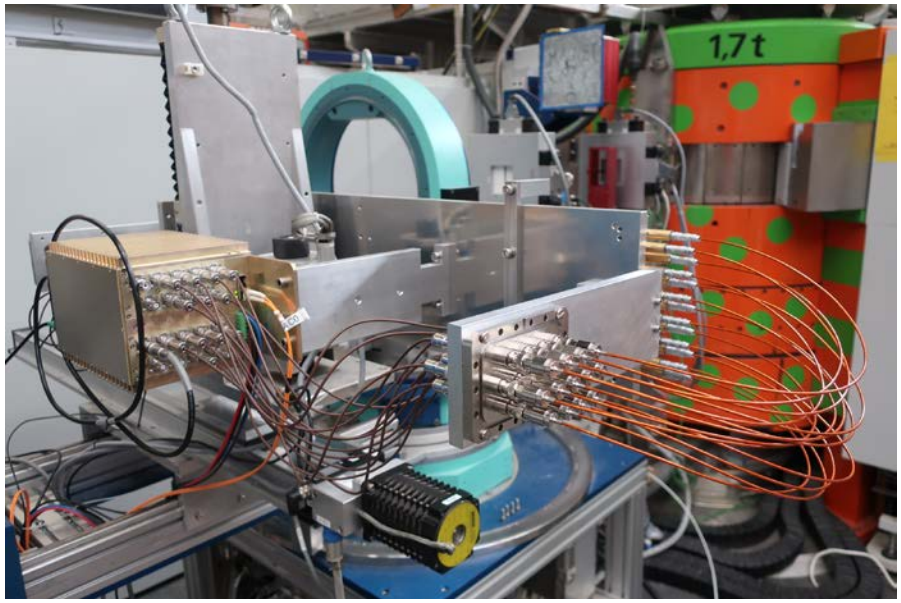
8b/10b coding

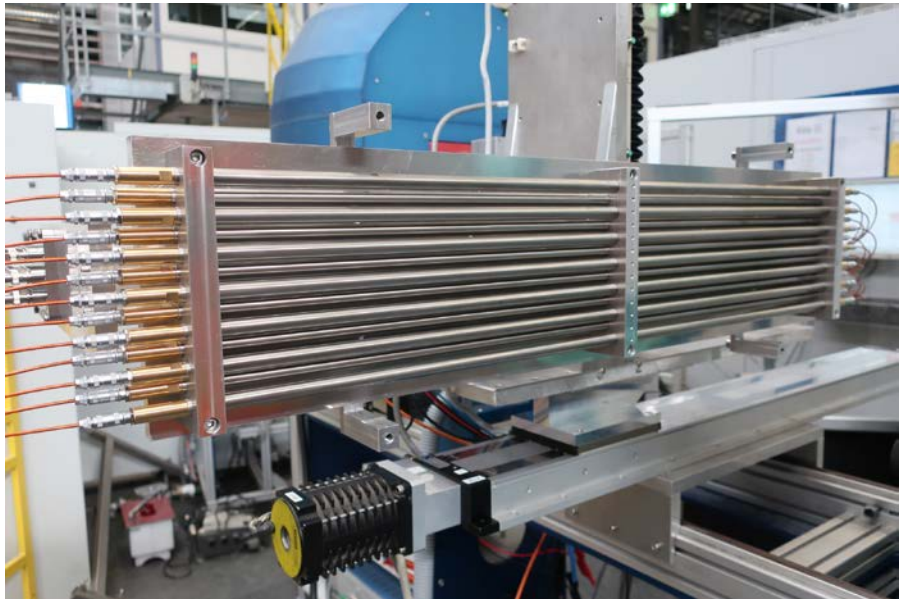
8 bit data	10 bit data (RD-)	10 bit data (RD+)
00000000	1001110100	0110001011
00000001	0111010100	1000101011
00000010	1011010100	0100101011
00000011	1100011011	1100010100
…	…	…

- Avoid long consecutive sequences of 0's or 1's
  → Clock embedded in data
- *Running disparity (RD)* is limited to -1 or 1
  → DC-free transmission
- **32 channels, 2 chips, 16 tracks**

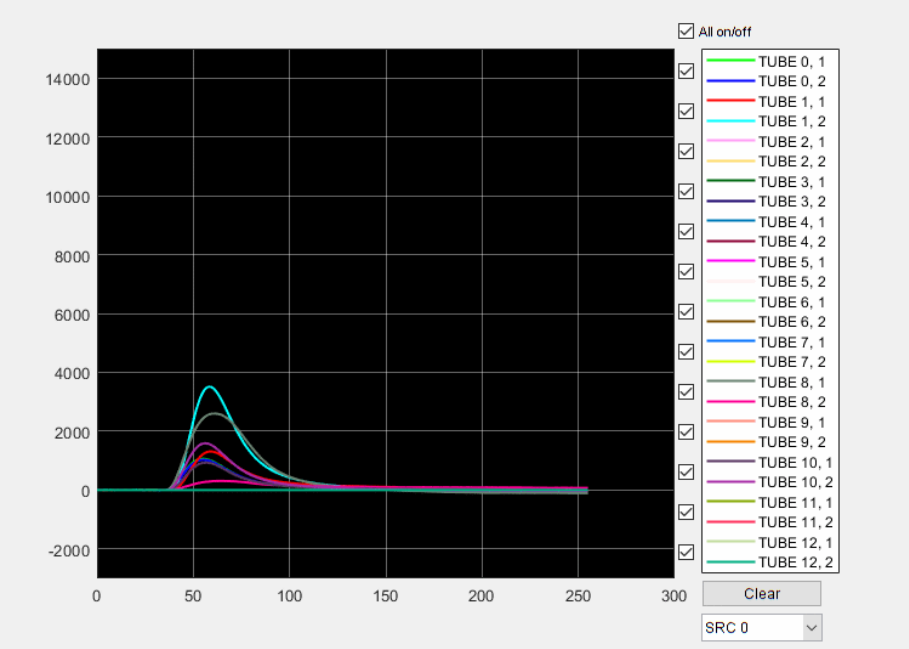


CAMEA frontend @ MORPHEUS



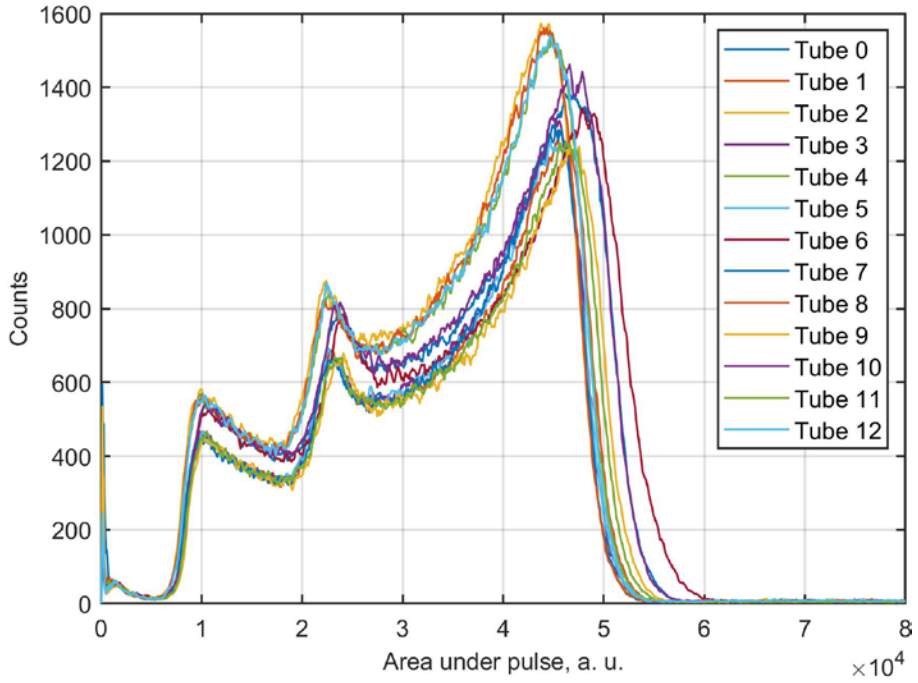


Raw waveform downlink



- 'Oscilloscope mode' to confirm:
  - Signal integrity
  - Trigger logic
  - Pulse position calculation

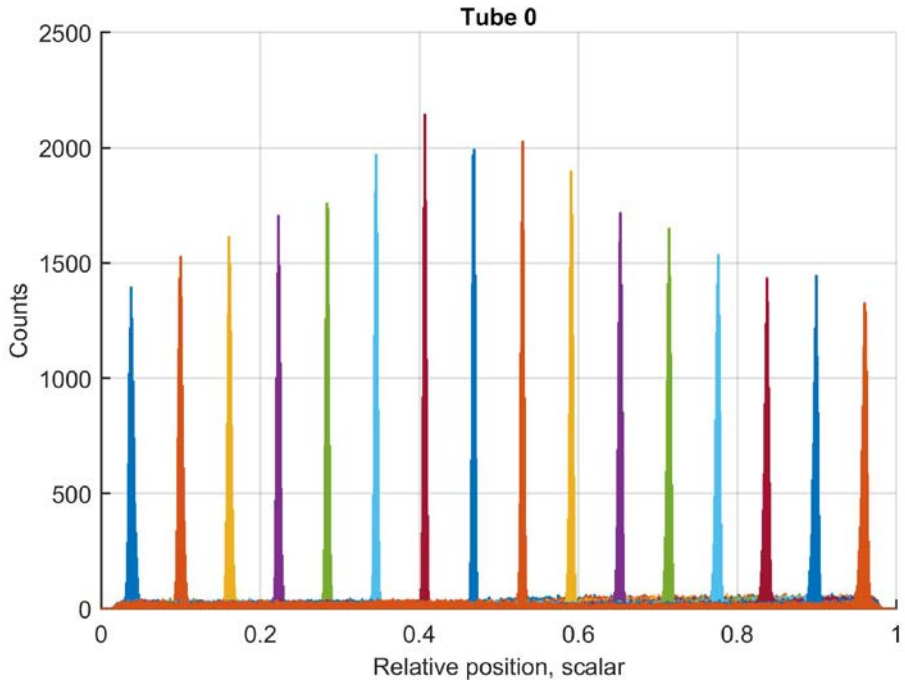
Pulse Height Spectrum (PHS)



- High voltage bias: 1500 V
- Spot size: 4x4 mm^2
- Measured at position 412 mm (i.e., approx. tube center)

Logfile D_00019

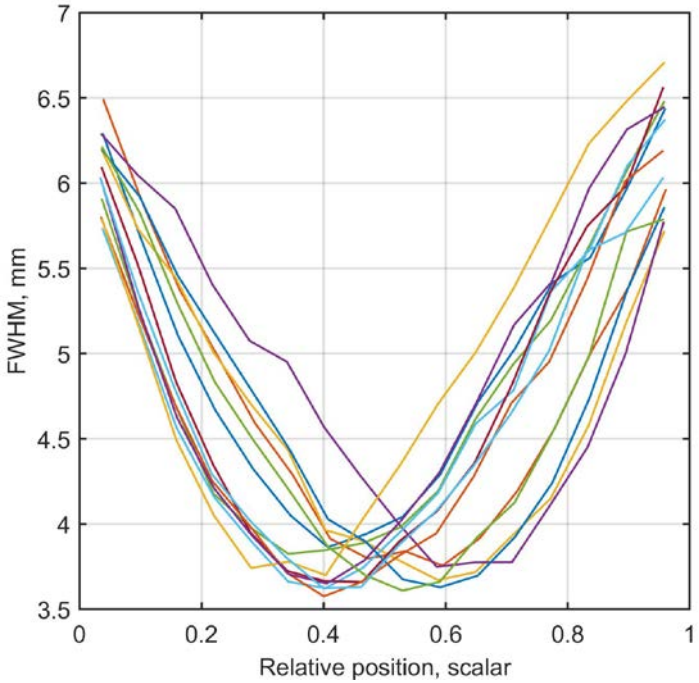
Pulse position histogram

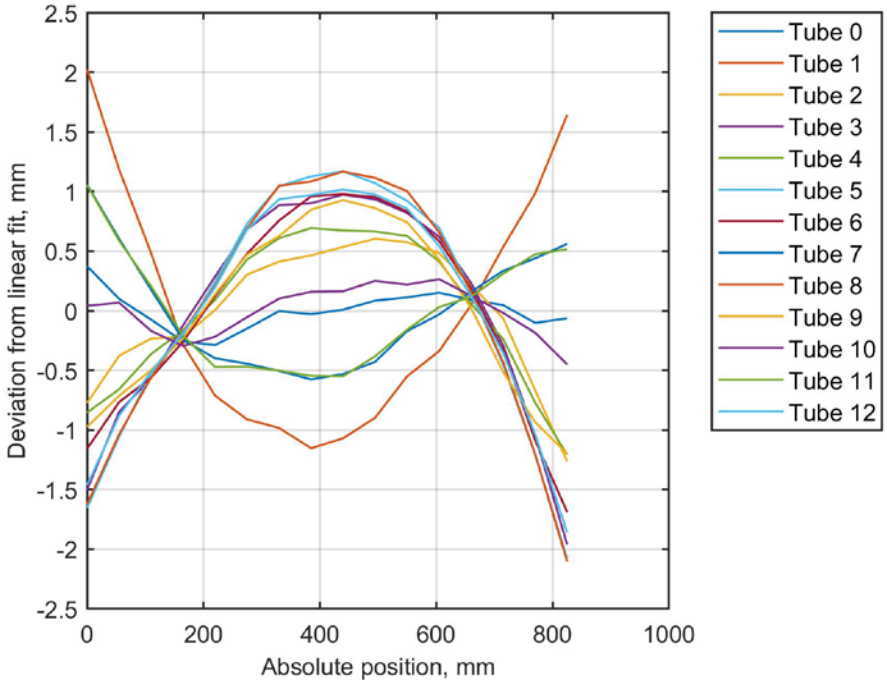


- High voltage bias: 1700 V
- Spot size: 1x3 mm^2
- Measured at positions [0:55:825] mm
- Similar results for tubes 1 to 12

Logfile D_00012

Full Width Half Max (FWHM) & linearity

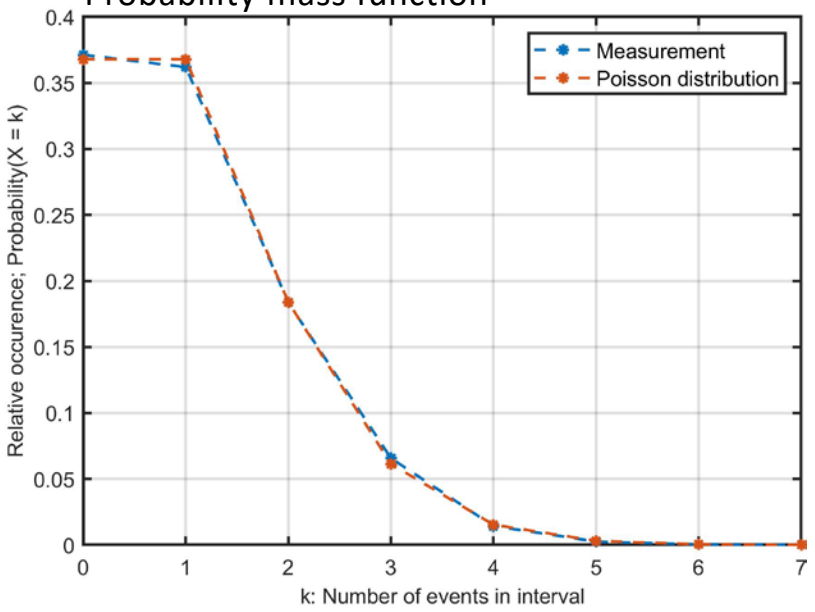




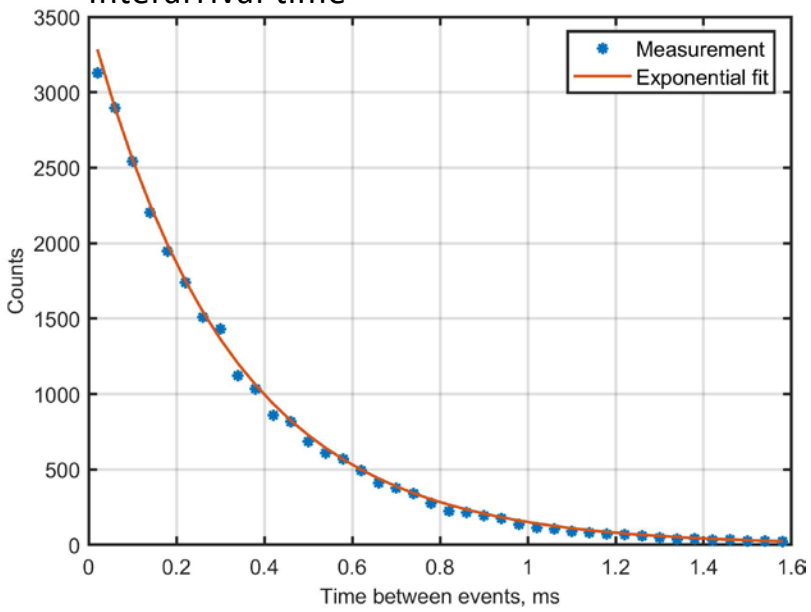
Logfile D_00012

Neutron event timestamps

Probability mass function



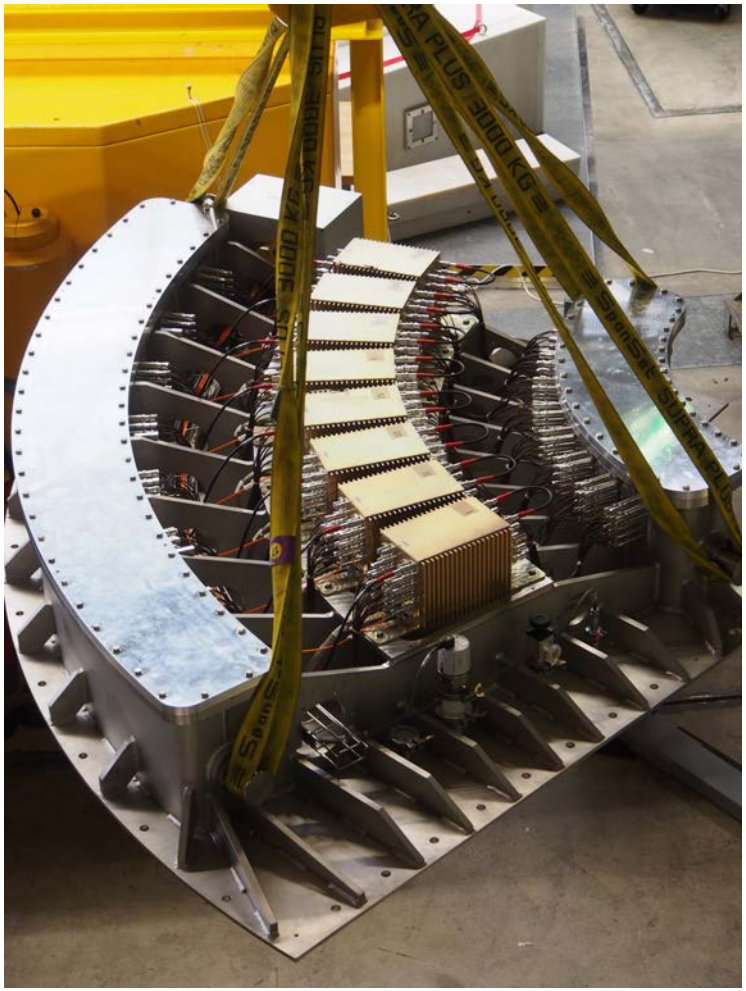
Interarrival time

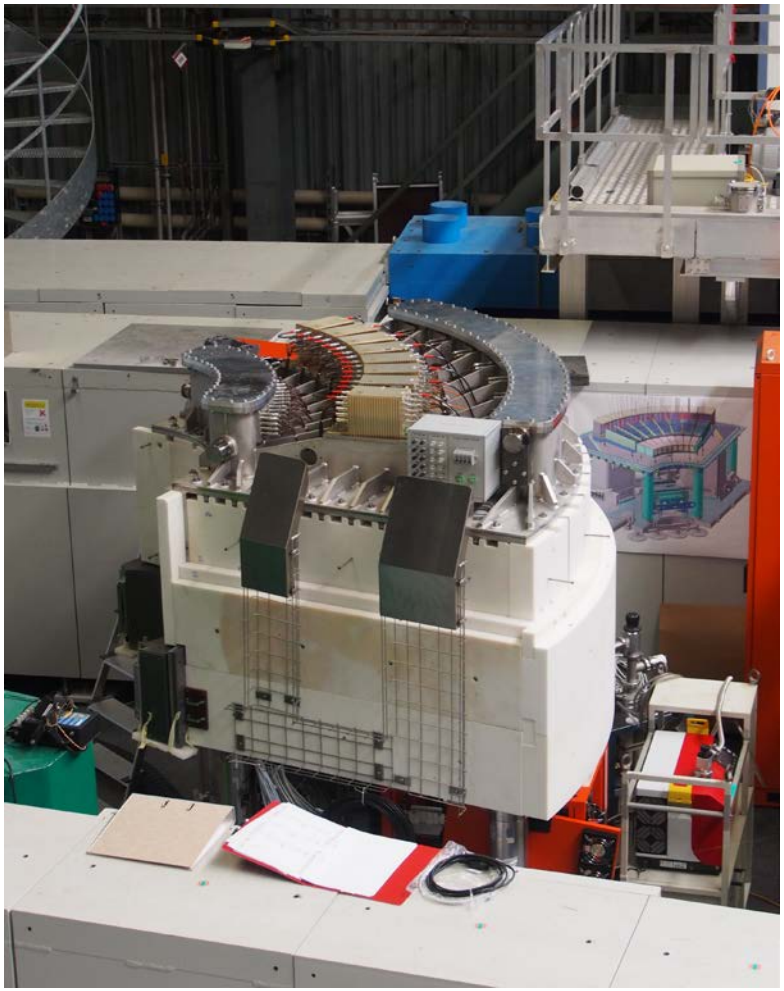


- Assumption: Neutron detection is a Poisson Process.

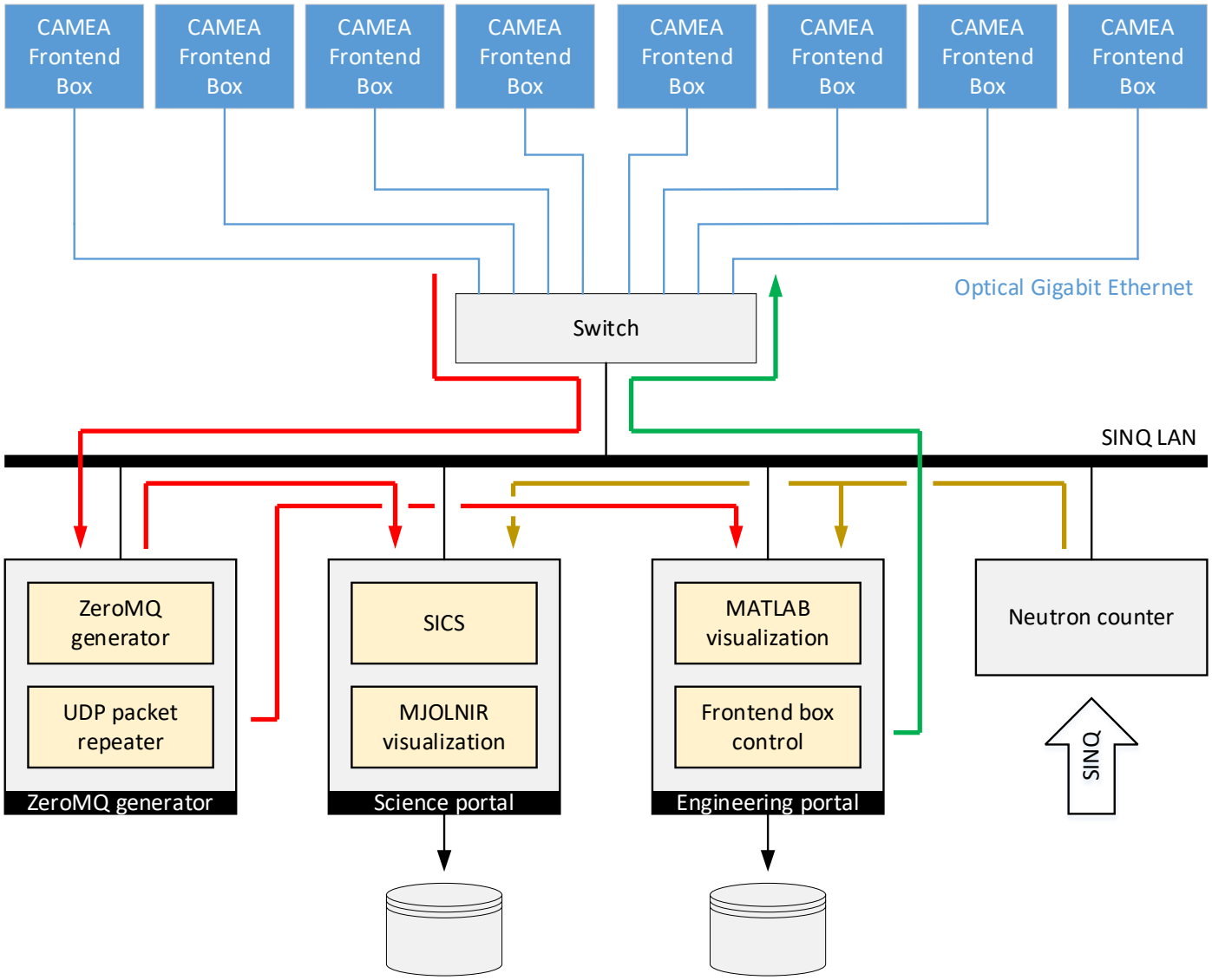
Logfile D_00021, 1755

Instrument integration

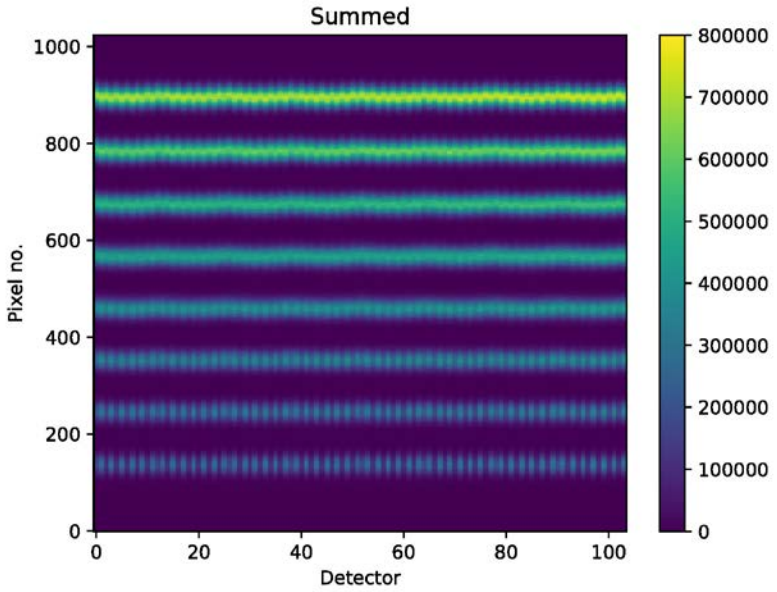




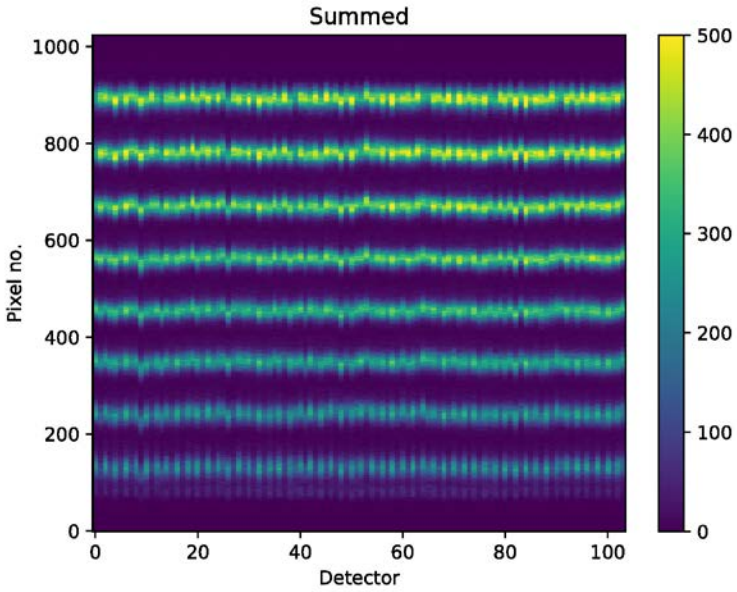
Data handling



‘First light’

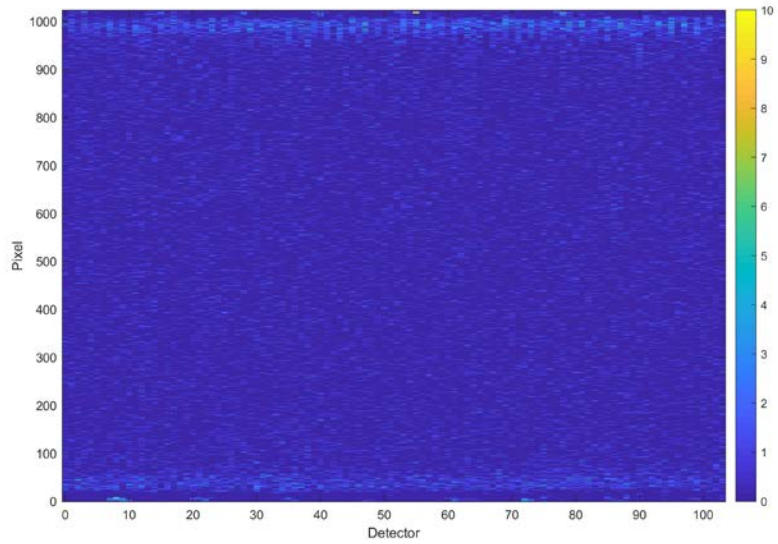


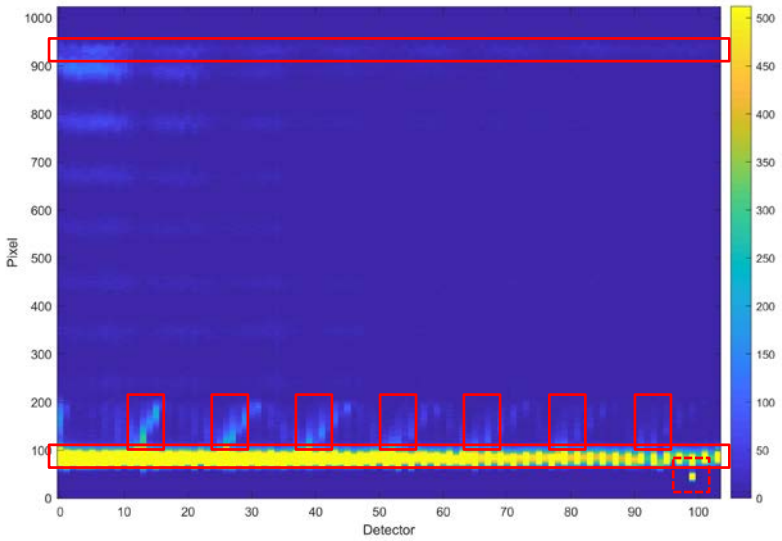
McStas simulation



Vanadium normalization scan

Background & spurious signals

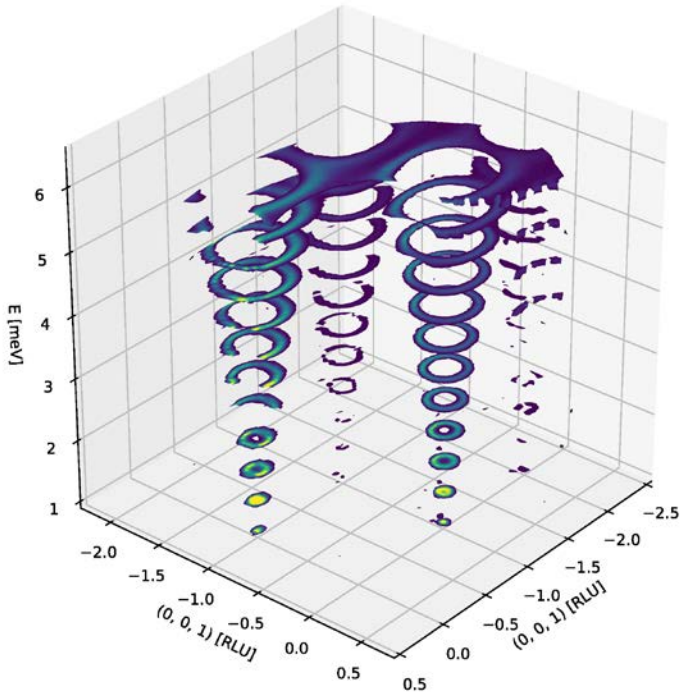


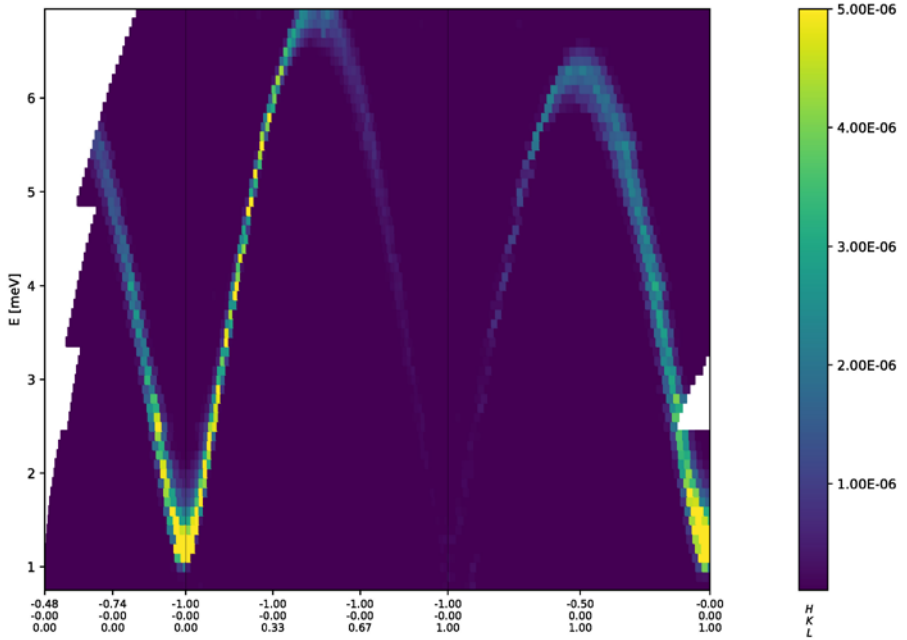


- Measurement time 5 h
- Background < 0.5 counts/min/detector

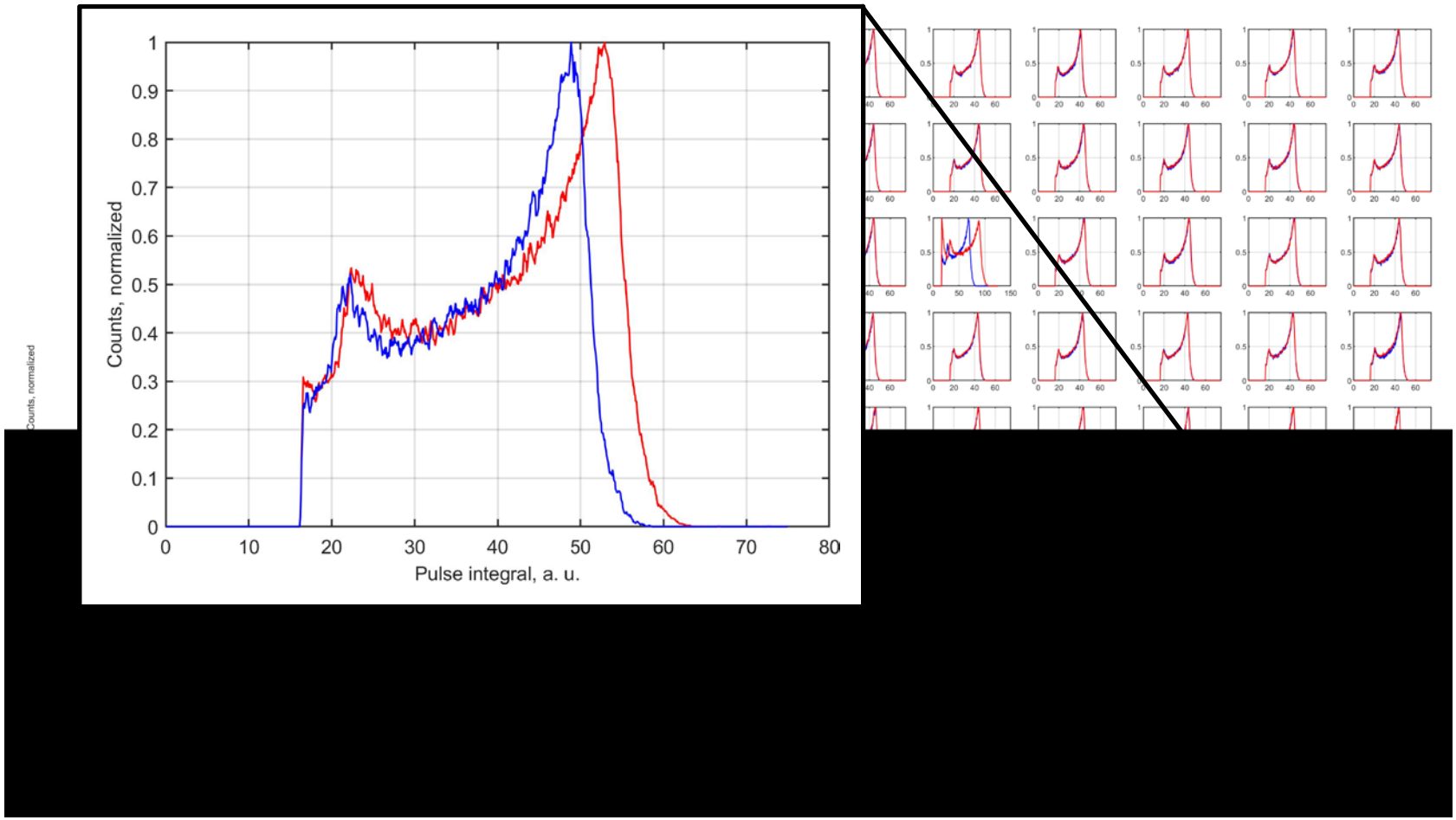
Logfiles D_00102, E_00231

Spin waves in MnF2





Detector diagnostics



Logfiles E_00119, E_00394

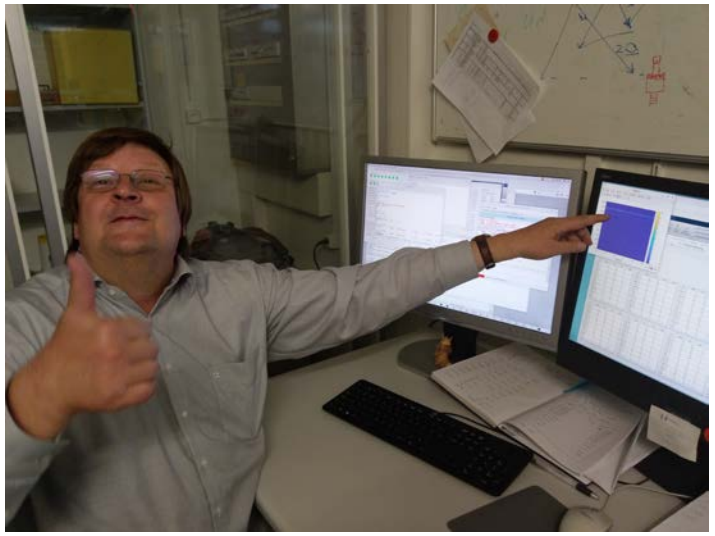
07.11.2018

13.12.2019

Conclusion

- We developed a new detector readout system, using many concepts of modern digital circuit design
- Compared to previous systems, the CAMEA electronics provides:
  - A higher integration density
  - Many system parameters are programmable
  - Extended functionality (waveform download, continuous PHS acquisition, etc.)
- Commissioning of the CAMEA instrument on a tight schedule
- Two months of (nearly) uninterrupted instrument uptime

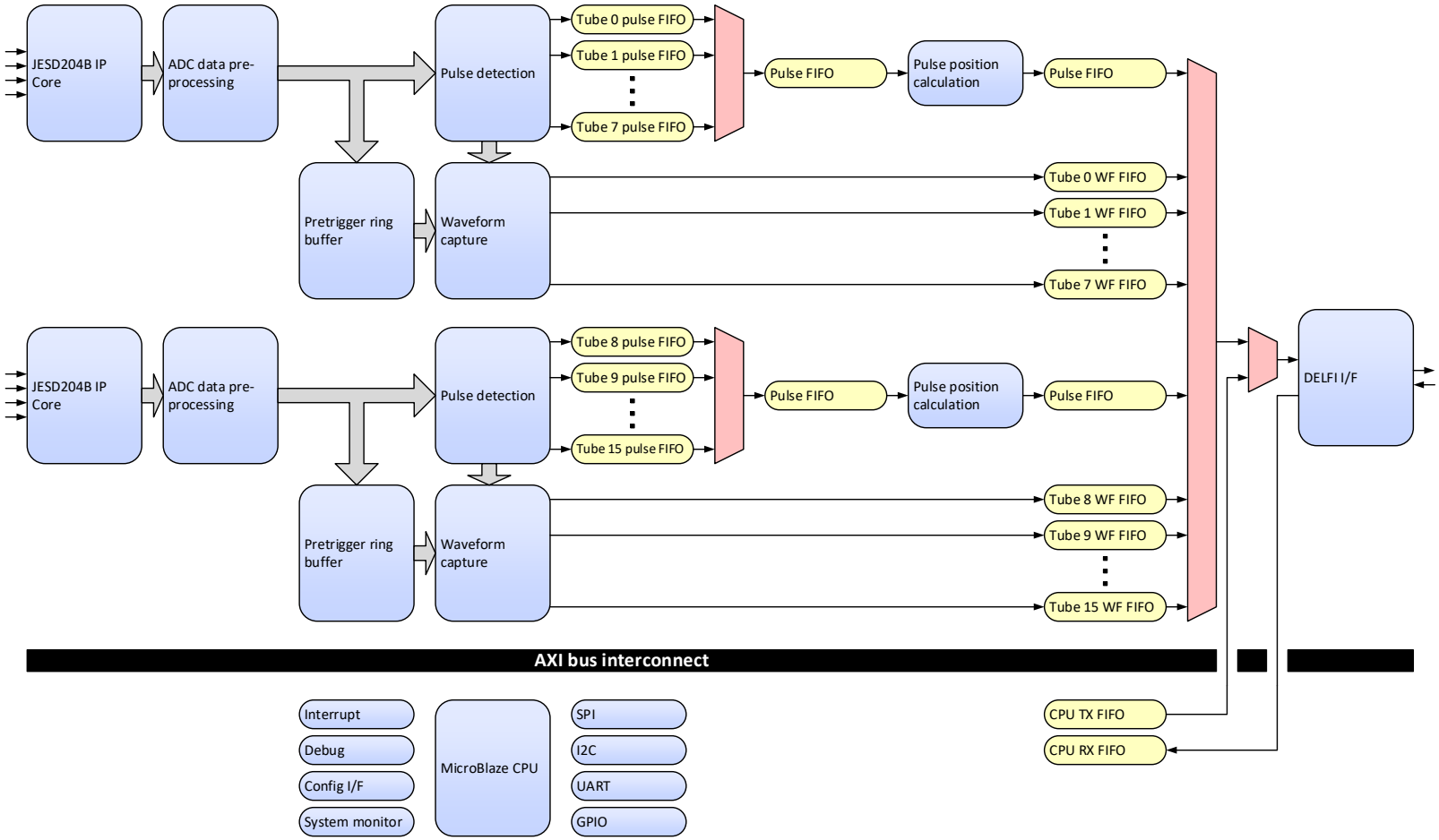
Happy scientist!



My thanks go to

- Urs Greuter
- Gerd Theidel
- The CAMEA team:
- Dieter Graf
- Jakob Lass
- Raphael Müller
- Christof Niedermayer
- Roman Bürge
- Christian Kägi
- Manuel Lehmann
- Marcel Schild
- …

Firmware


JESD204B IP Core
ADC data pre-processing
Pulse detection
Tube 0 pulse FIFO
Tube 1 pulse FIFO
Tube 7 pulse FIFO
Pulse FIFO
Pulse position calculation
Pulse FIFO
Pretrigger ring buffer
Waveform capture
Tube 0 WF FIFO
Tube 1 WF FIFO
Tube 7 WF FIFO
JESD204B IP Core
ADC data pre-processing
Pulse detection
Tube 8 pulse FIFO
Tube 9 pulse FIFO
Tube 15 pulse FIFO
Pulse FIFO
Pulse position calculation
Pulse FIFO
Pretrigger ring buffer
Waveform capture
Tube 8 WF FIFO
Tube 9 WF FIFO
Tube 15 WF FIFO
DELFI I/F
AXI bus interconnect
Interrupt
Debug
Config I/F
System monitor
MicroBlaze CPU
SPI
I2C
UART
GPIO
CPU TX FIFO
CPU RX FIFO

Commanding interface