

PAUL SCHERRER INSTITUT



Frank Herzog :: Electronics Engineer :: Paul Scherrer Institut

# Frontend Electronics Design for the CAMEA Instrument

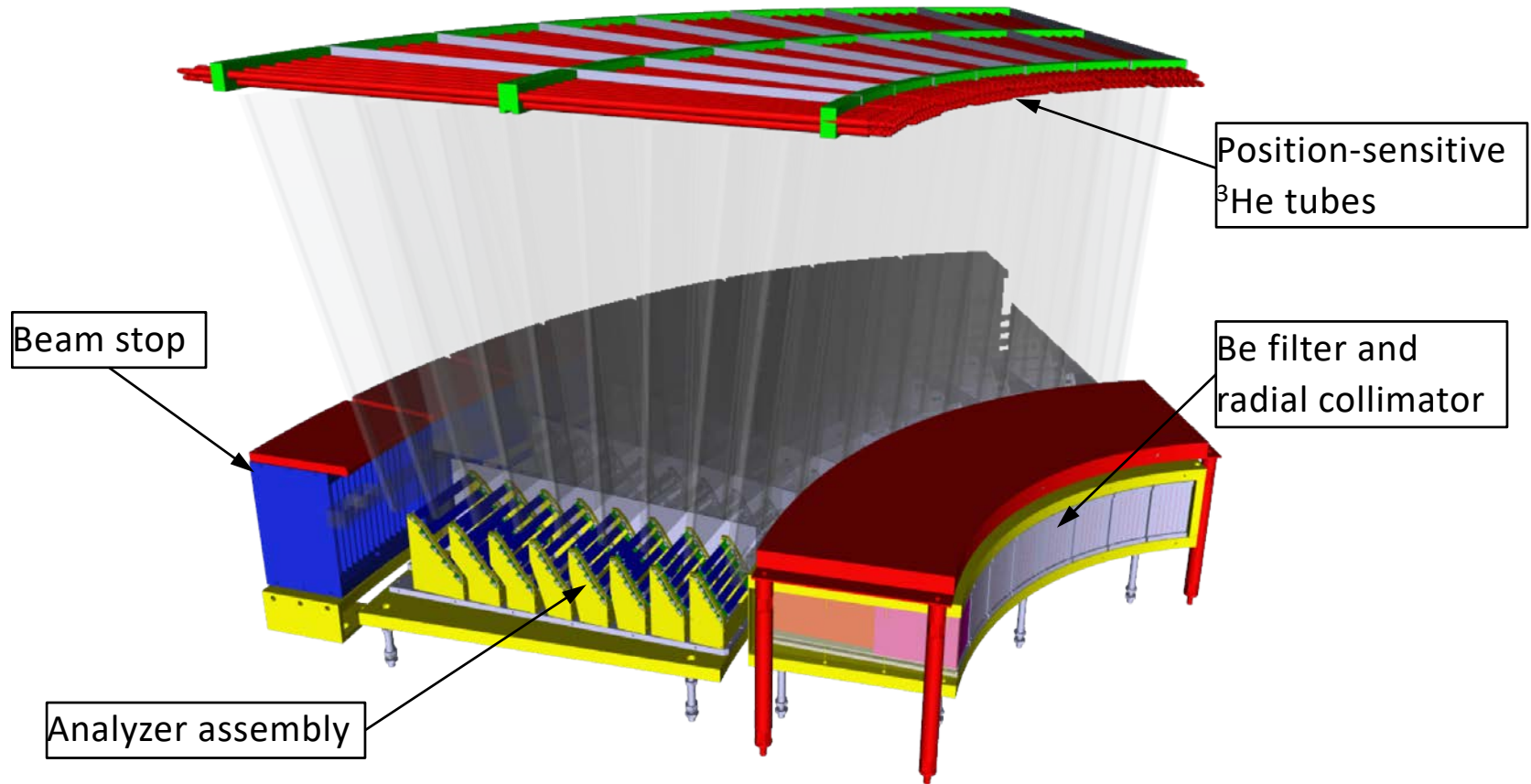
LTP Seminar, 23.09.2019



# Content

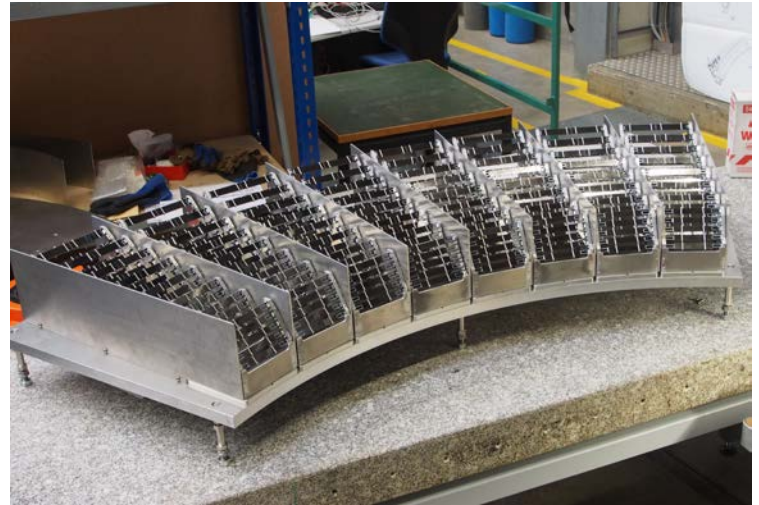
- CAMEA instrument introduction
- The CAMEA frontend electronics
- MORPHEUS tests
- Instrument commissioning

# Instrument concept



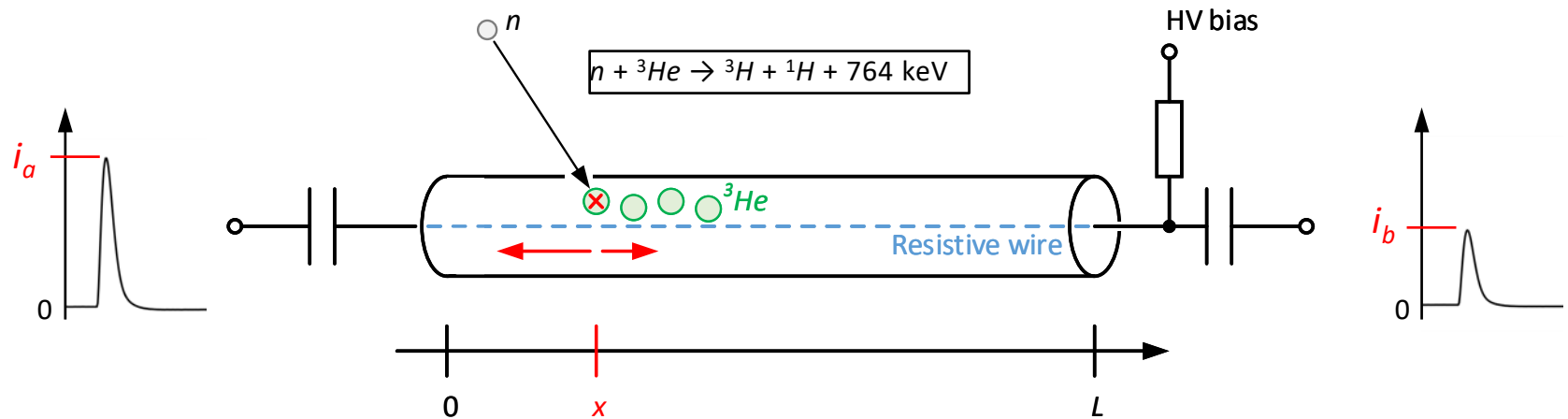
- CAMEA: Continuous Angle Multiple Energy Analysis
- Groitl, F. et al. *CAMEA – A novel multiplexing analyzer for neutron spectroscopy*, Rev. Sci. Instruments 87

# CAMEA instrument overview



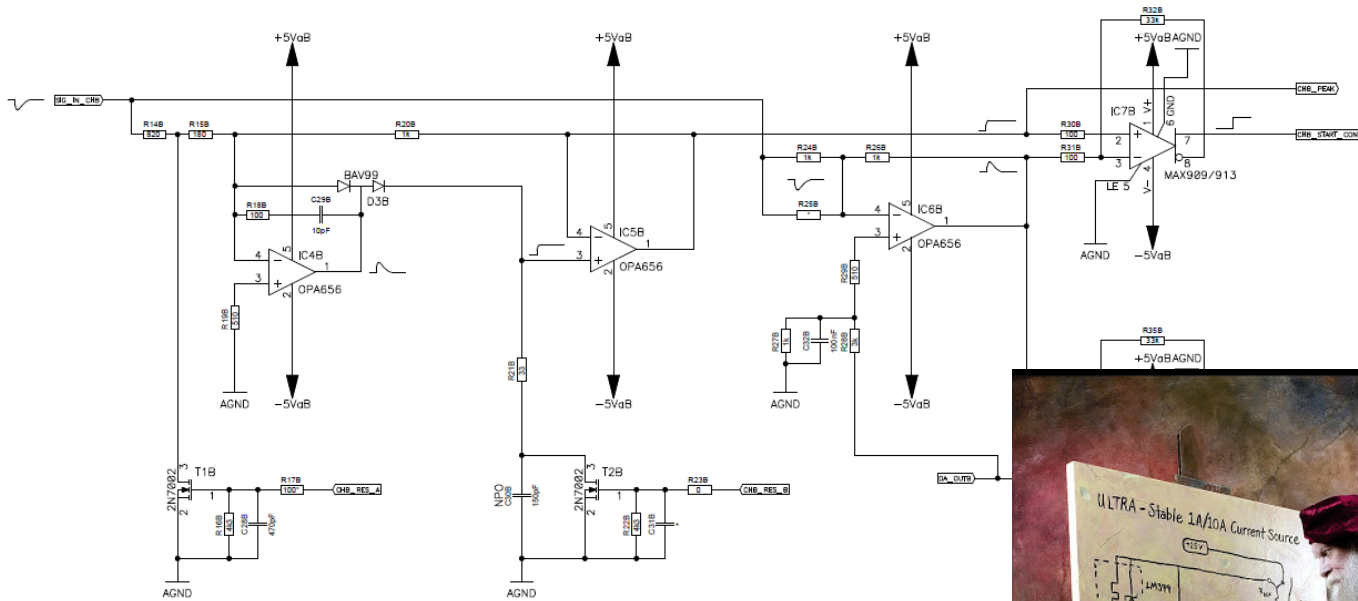
# Detector readout

- 104 position sensitive (charge-division)  $^3\text{He}$  neutron detector tubes  
→ 208 analog acquisition channels
- Pulse event duration < 100 ns



$$x \approx \frac{i_b}{i_a + i_b}$$

# Use existing PSI electronics?



- Analog track-and-hold, peak detection, etc.
- Proven performance but:
  - Many discrete components, low integration density
  - Hardwired trigger levels, filter bandwidths, etc.

**«My favourite programming language is solder»**

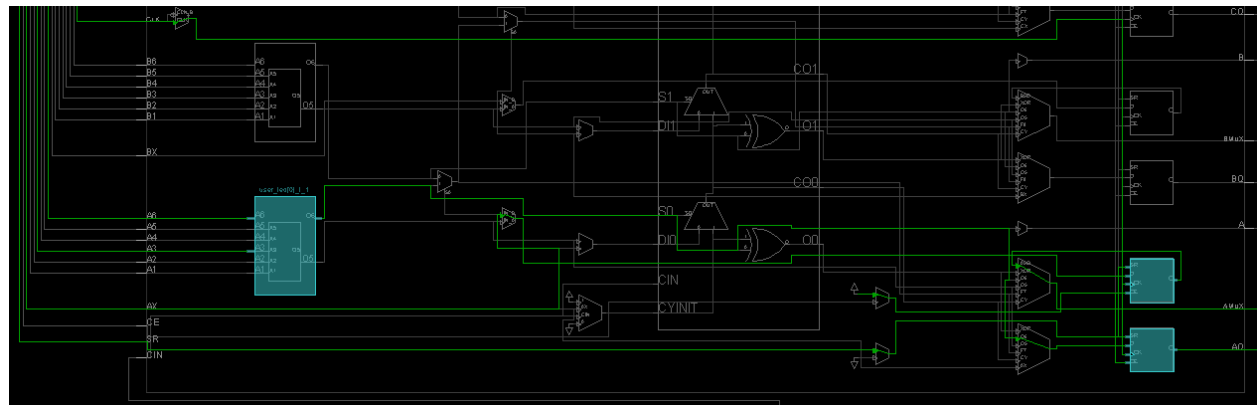
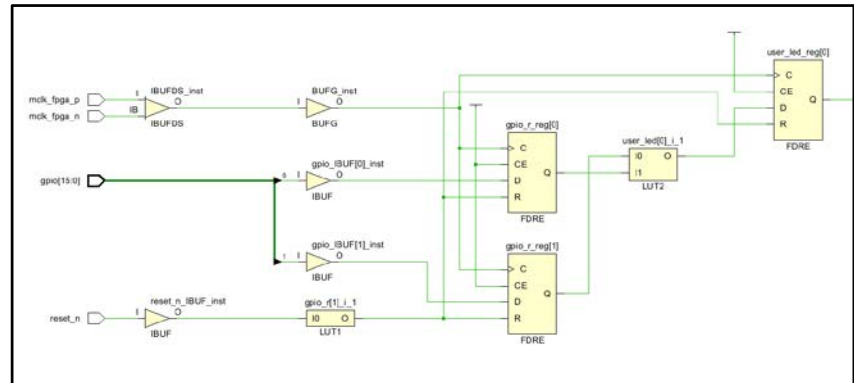


# ...but then came FPGAs!

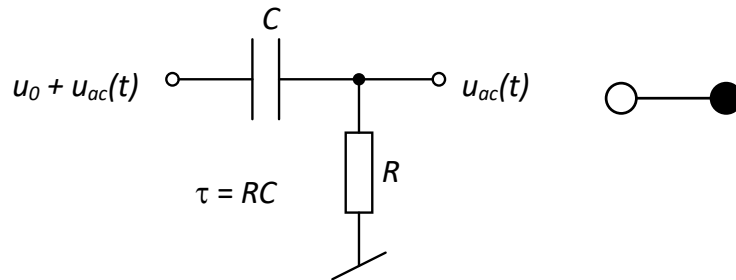
- FPGA: Field Programmable Gate Array
- VHDL: Very high speed integrated circuit Hardware Description Language

```
architecture rtl of simple_vhdl_top is
    signal mclk_fpga      : std_logic;
    signal mclk           : std_logic;
    signal gpio_r         : std_logic_vector(15 downto 0);
begin

    process (mclk, reset_n) is
    begin
        if (rising_edge(mclk)) then
            if (reset_n = '0') then
                gpio_r      <= (others => '0');
                user_led    <= (others => '0');
            else
                gpio_r      <= gpio;
                user_led(0) <= gpio_r(1) and gpio_r(0);
            end if;
        end if;
    end process;
end architecture;
```



# Digital Signal Processing (DSP) example



Offset-free output

Input

Internal state (offset)

$$y_{AC}(n) = u(n) - x(n)$$

$$x(n+1) = \frac{1}{M} \cdot \sum_{k=-\infty}^n y_{AC}(k)$$

'Time constant'

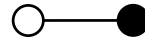
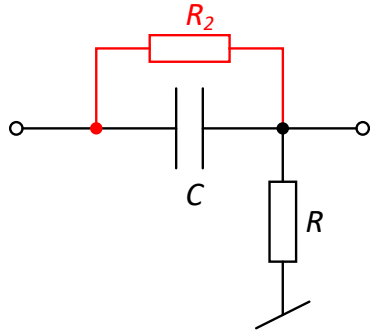
Accumulator

- Will probably need thousands of transistors in FPGA, but transistors are extremely small (28 nm gate width) → tiny footprint
- Programmable time constant M
- Provides additional offset information

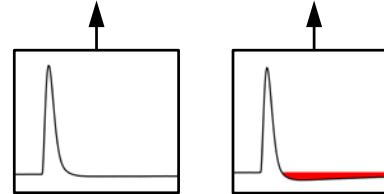


# More examples...

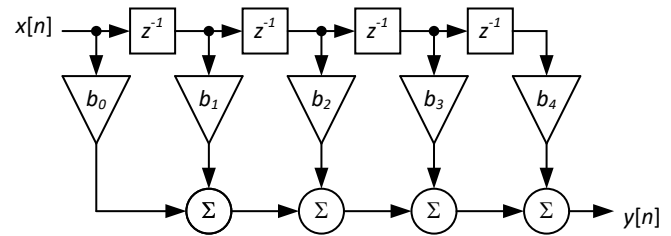
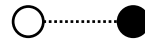
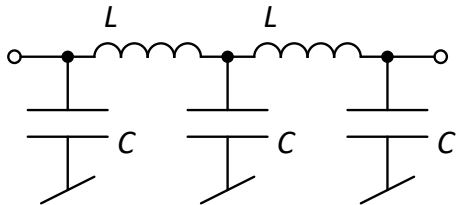
## Pole-zero cancellation



$$y'_{AC}(n) = y_{AC}(n) + \frac{1}{M_2} \cdot \sum_{k=-\infty}^n y_{AC}(k)$$



## Filtering



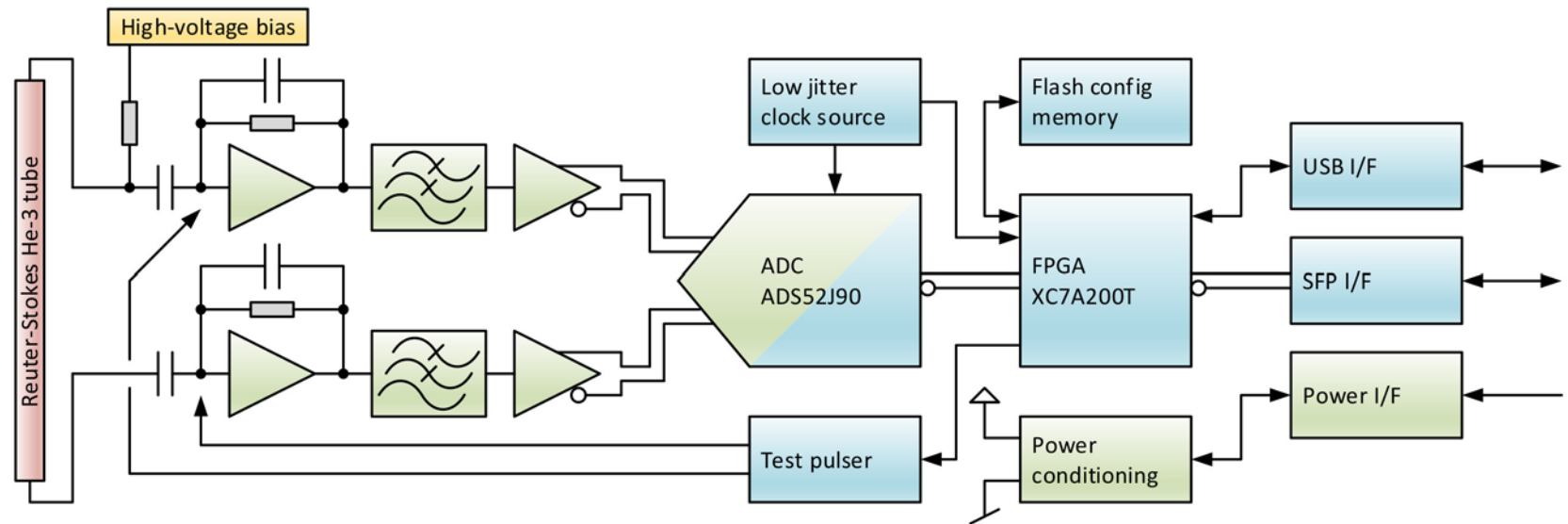
## Division



```

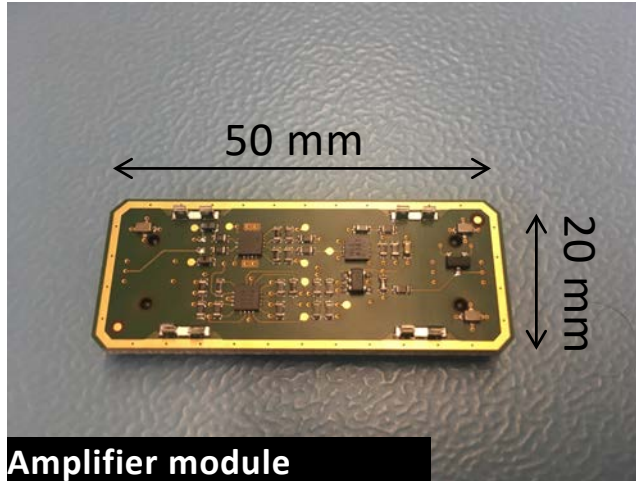
Q = 0;
while N ≥ D
    N = N-D;
    Q = Q+1;
end
    
```

# CAMEA frontend electronics concept

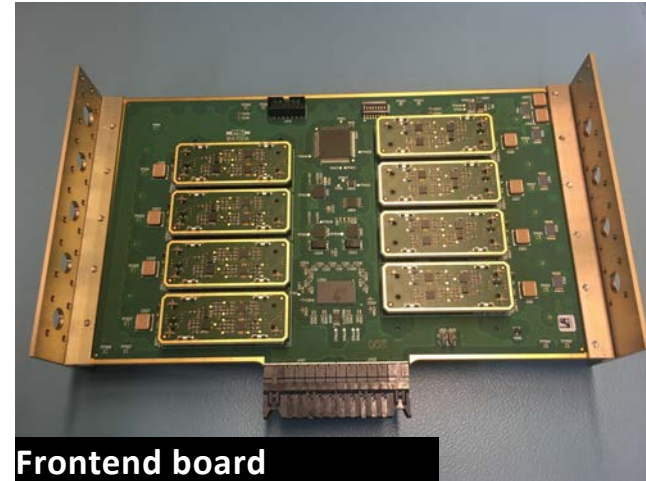


- Amplification
- Sampling
- Signal conditioning
- Pulse detection
- Pulse position calculation

# Frontend electronics hardware



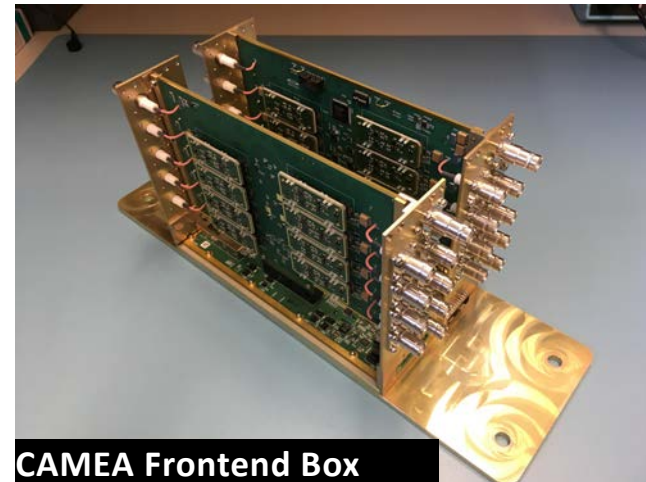
**Amplifier module**



**Frontend board**



**Data concentrator board**



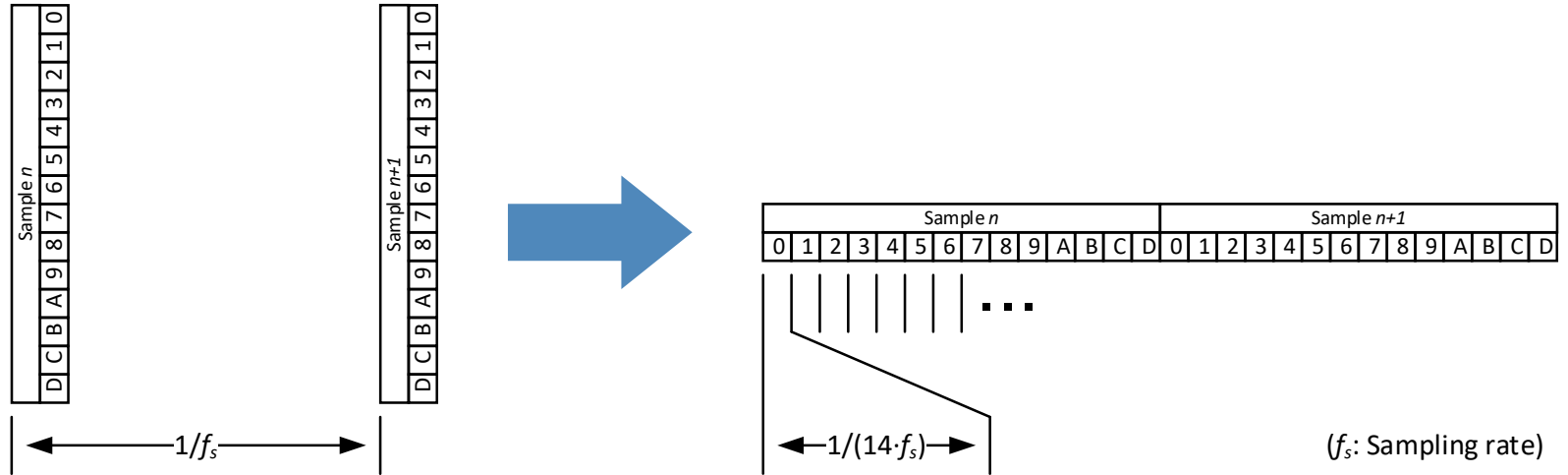
**CAMEA Frontend Box**

# Integration density?

- 32 acquisition channels per box
- 32 ADCs
- 14 bit resolution per ADC
- 448 tracks
- 125  $\mu\text{m}$  track width and clearance
- → **11 cm data bus width**



# Serialization

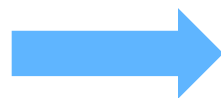


- 32 differential data lines
- 32 differential clock lines
- 128 tracks
- **Better, but still...**

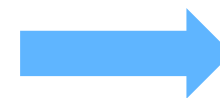
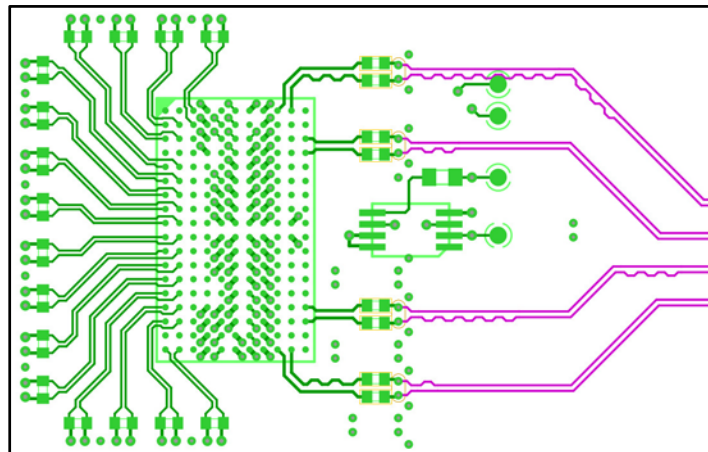
# 8b/10b coding

8 bit data	10 bit data (RD-)	10 bit data (RD+)
00000000	1001110100	0110001011
00000001	0111010100	1000101011
00000010	1011010100	0100101011
00000011	1100011011	1100010100
...	...	...

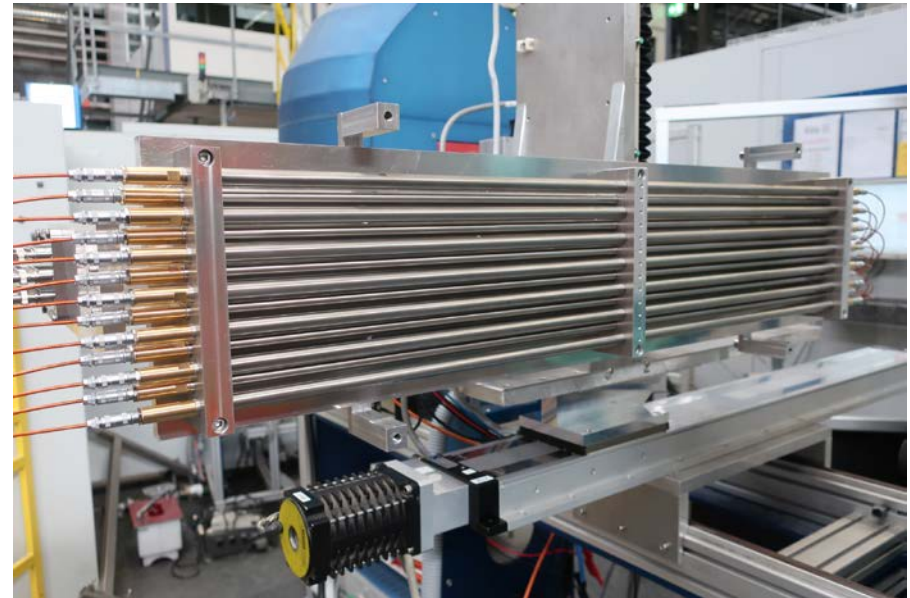
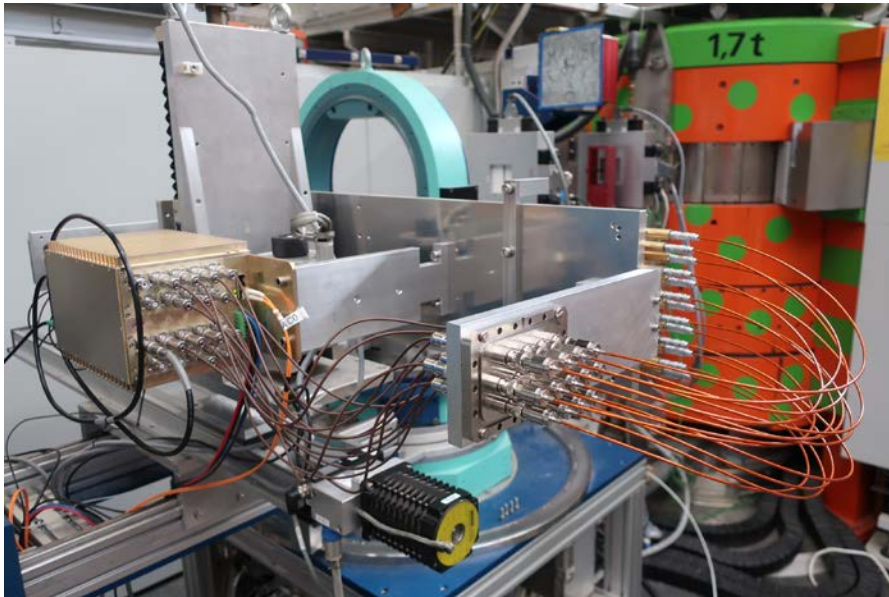
- Avoid long consecutive sequences of 0's or 1's  
→ Clock embedded in data
- *Running disparity (RD)* is limited to -1 or 1  
→ DC-free transmission
- **32 channels, 2 chips, 16 tracks**



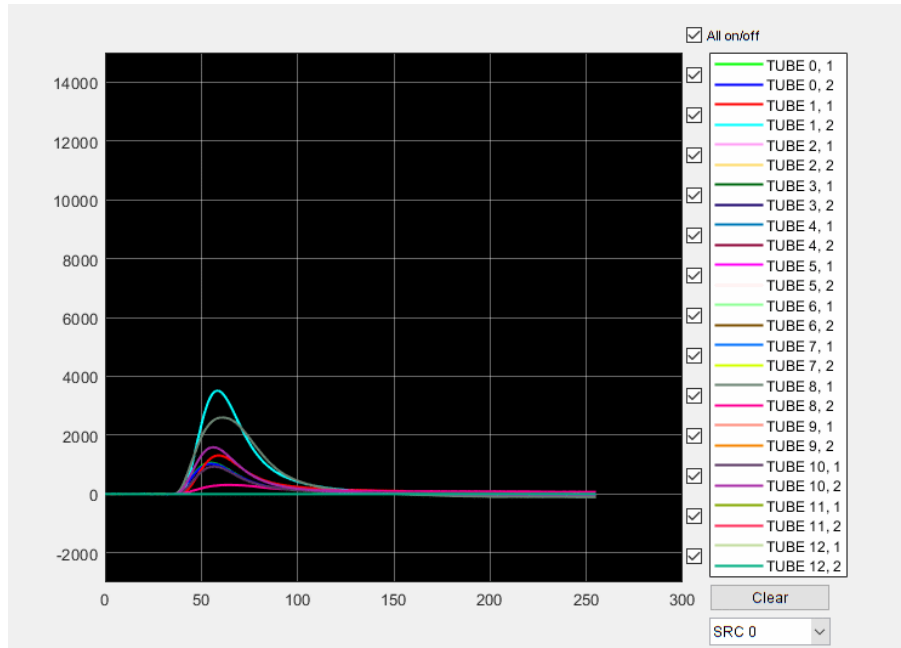
16 channel  
analog input



4x5 Gb/s  
( $4 \times 80 \cdot f_s$ )



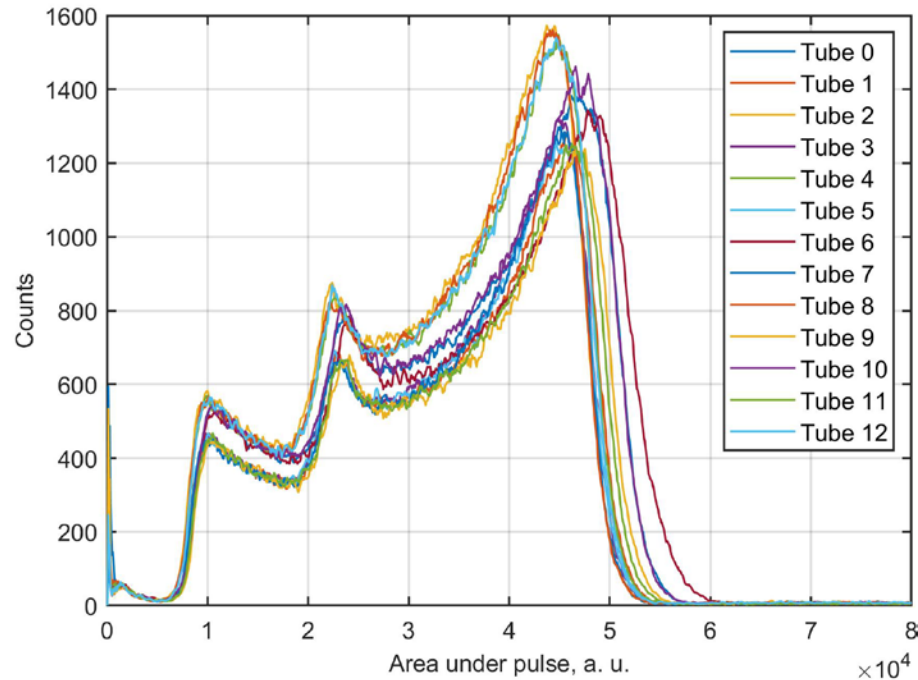
# Raw waveform downlink



- 'Oscilloscope mode' to confirm:
  - Signal integrity
  - Trigger logic
  - Pulse position calculation

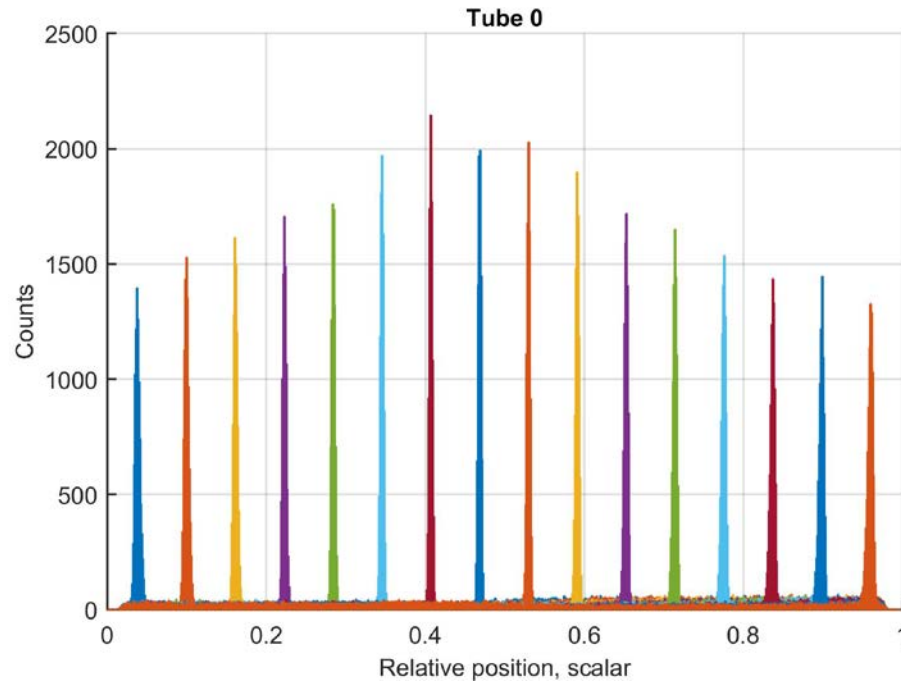


# Pulse Height Spectrum (PHS)



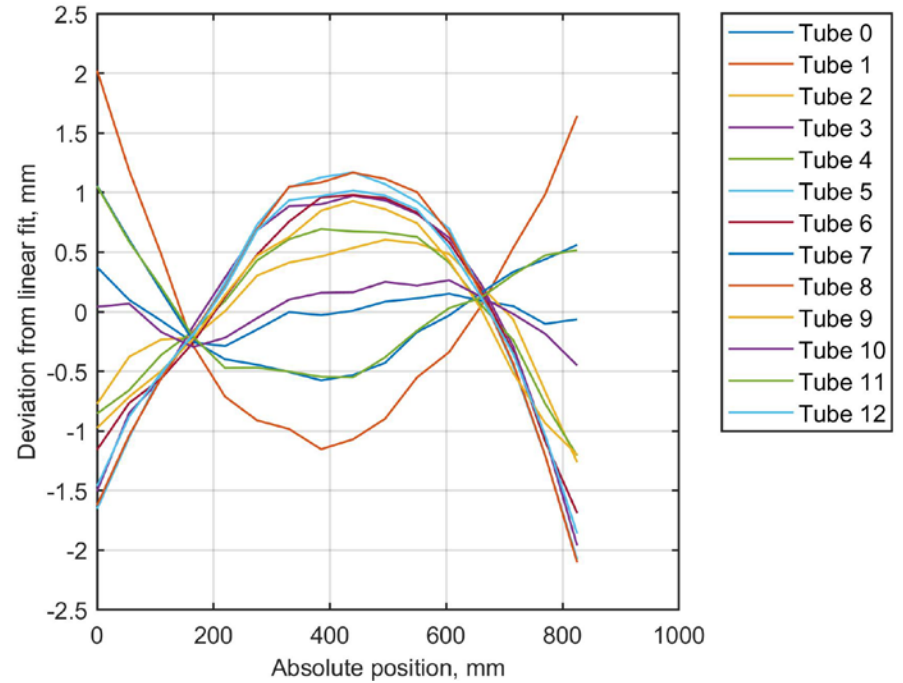
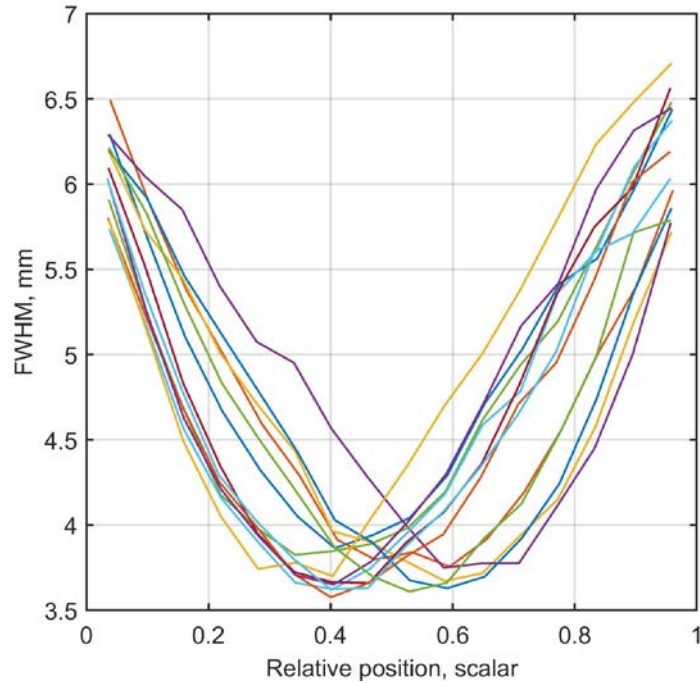
- High voltage bias: 1500 V
- Spot size: 4x4 mm<sup>2</sup>
- Measured at position 412 mm (i.e., approx. tube center)

# Pulse position histogram

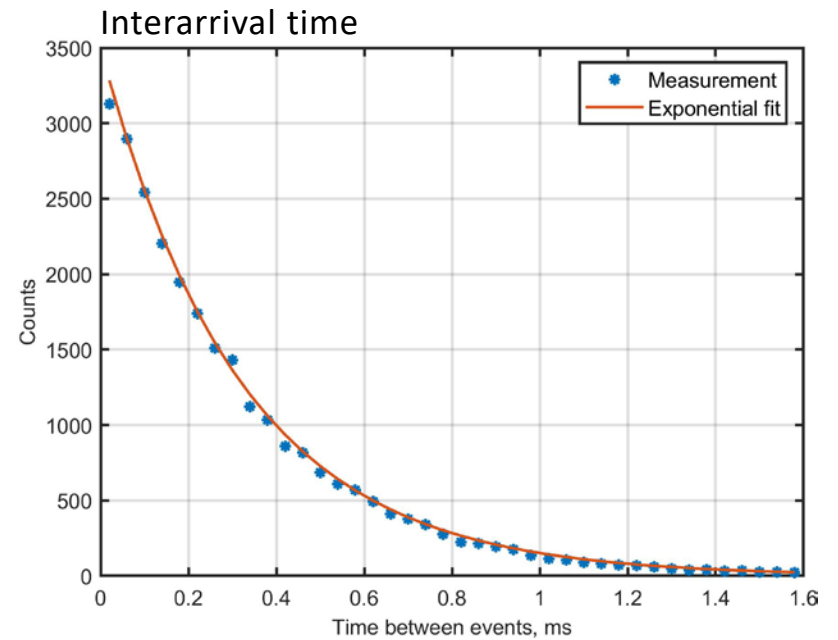
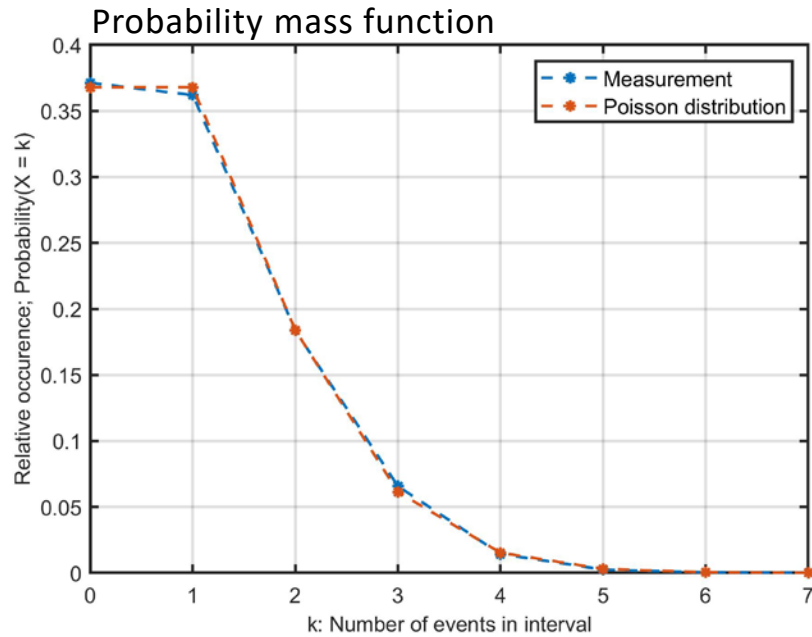


- High voltage bias: 1700 V
- Spot size: 1x3 mm<sup>2</sup>
- Measured at positions [0:55:825] mm
- Similar results for tubes 1 to 12

# Full Width Half Max (FWHM) & linearity

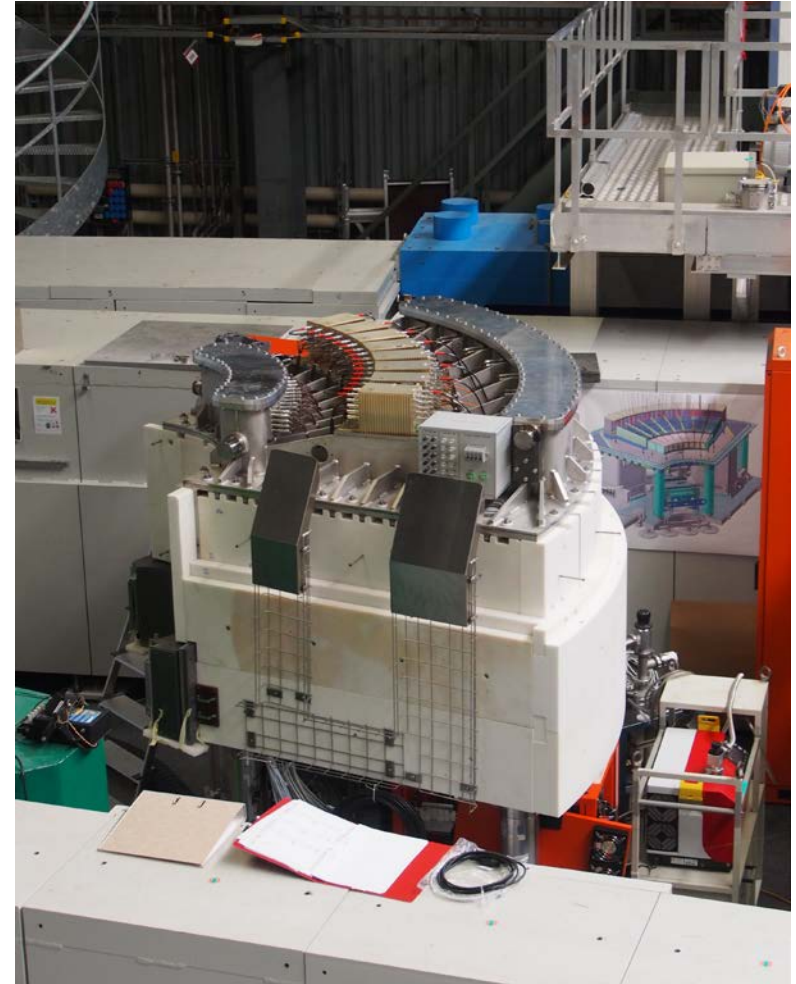
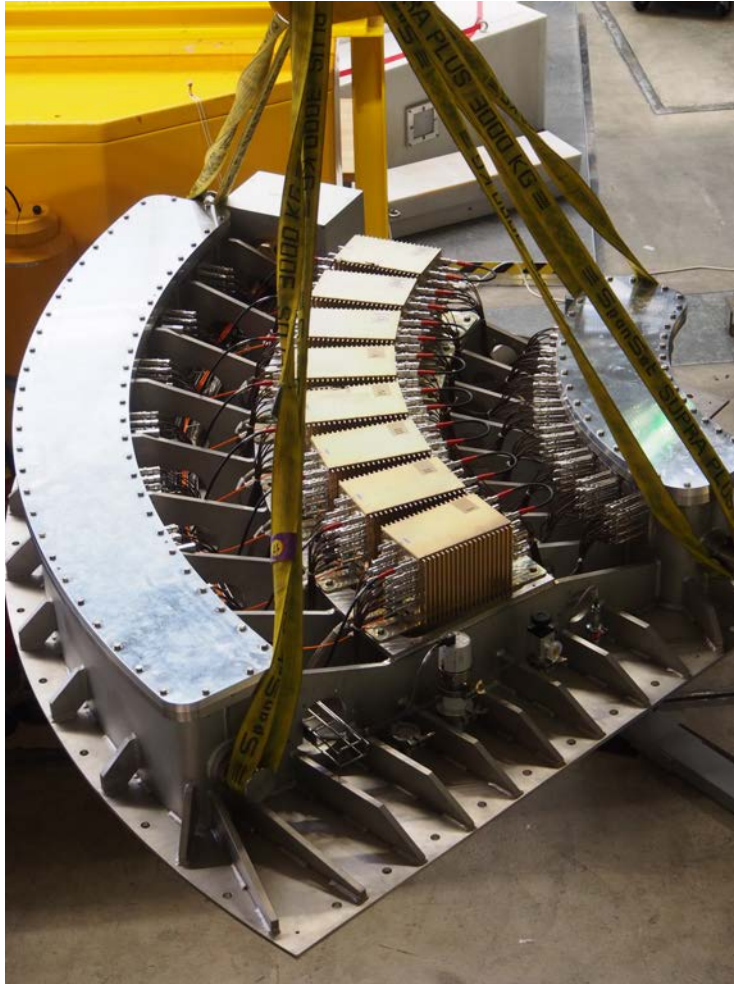


# Neutron event timestamps

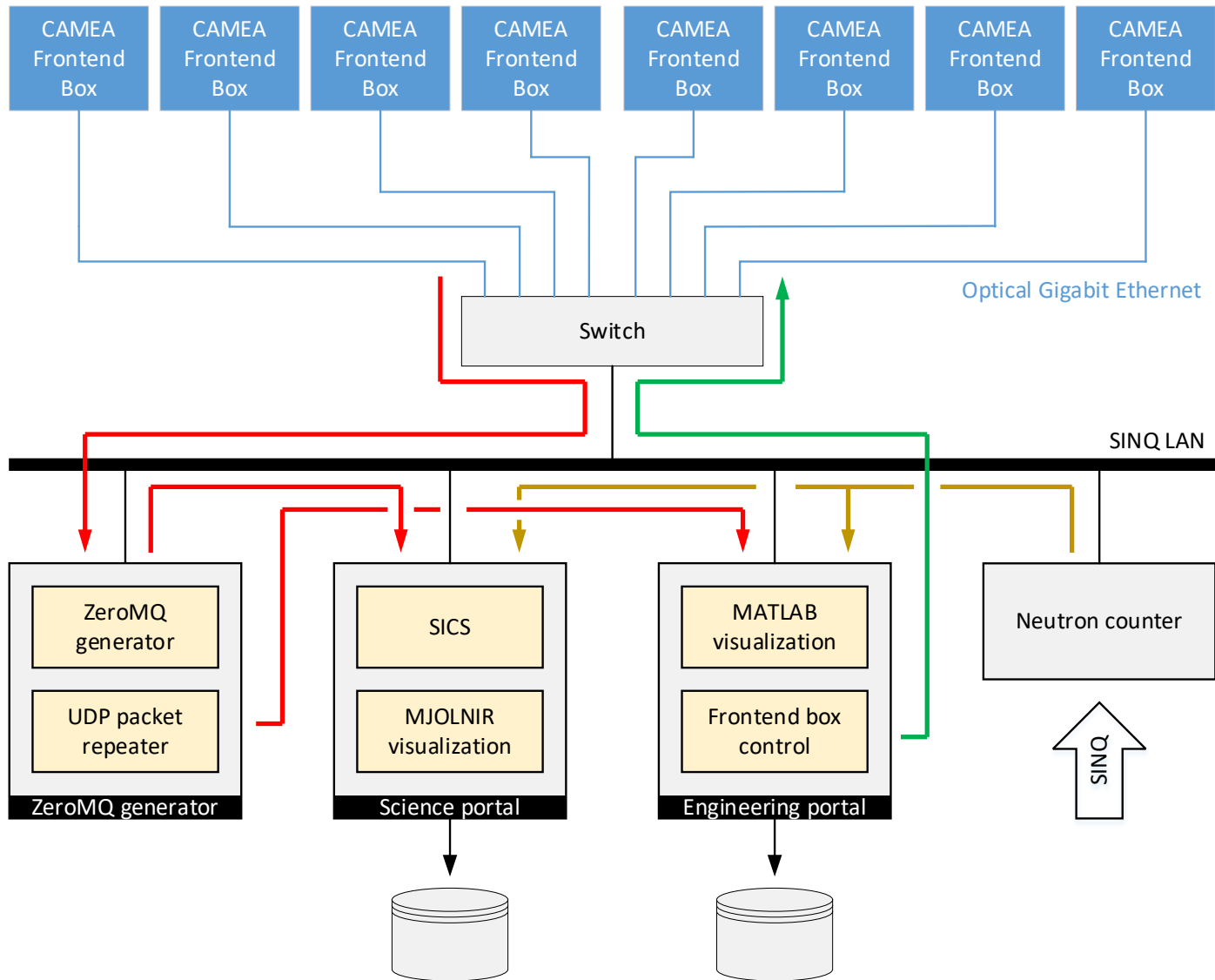


- Assumption: Neutron detection is a Poisson Process.

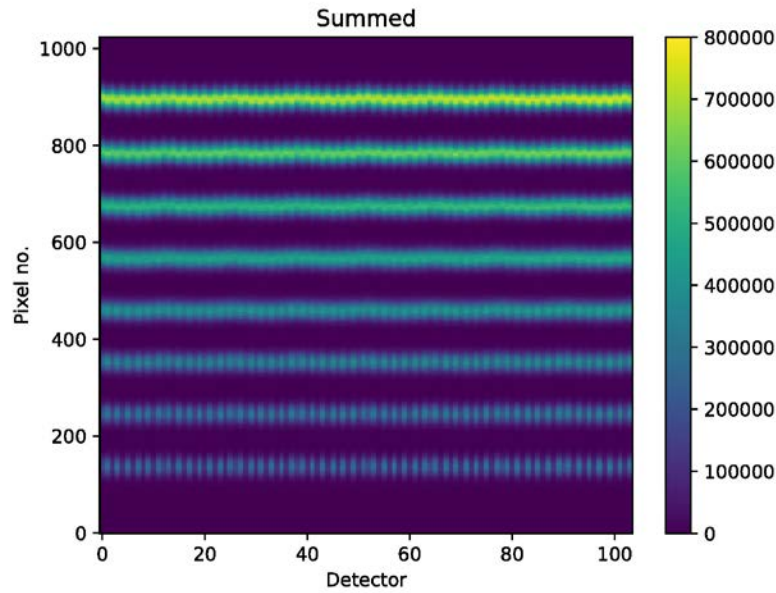
# Instrument integration



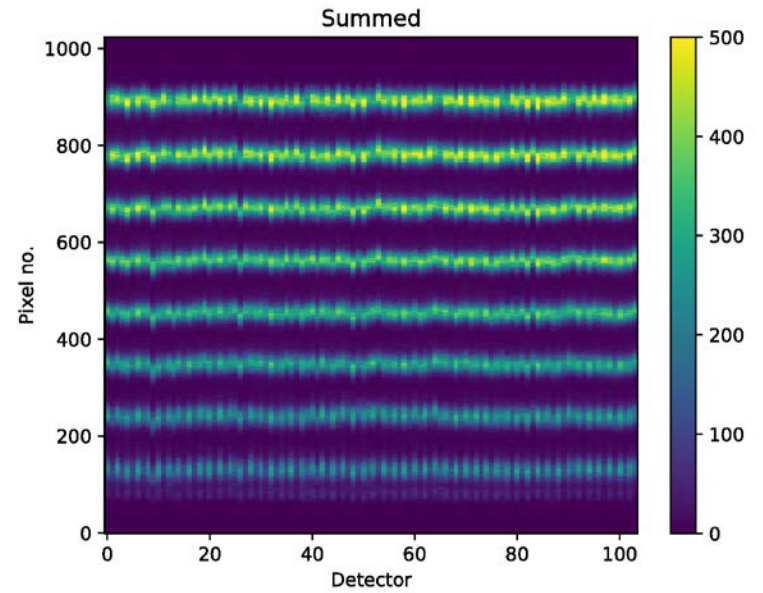
# Data handling



# 'First light'

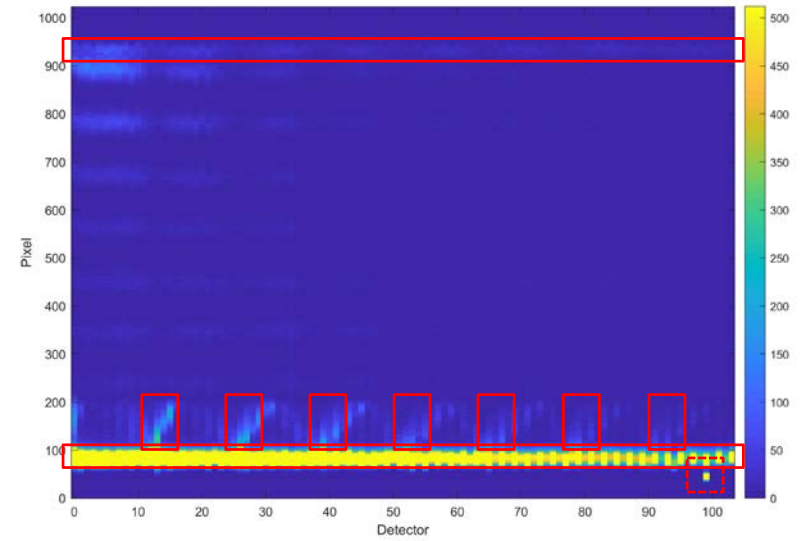
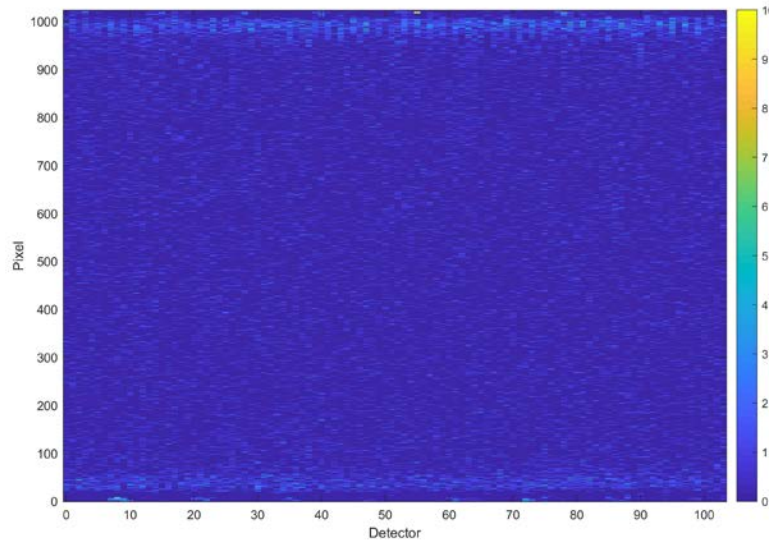


McStas simulation



Vanadium normalization scan

# Background & spurious signals



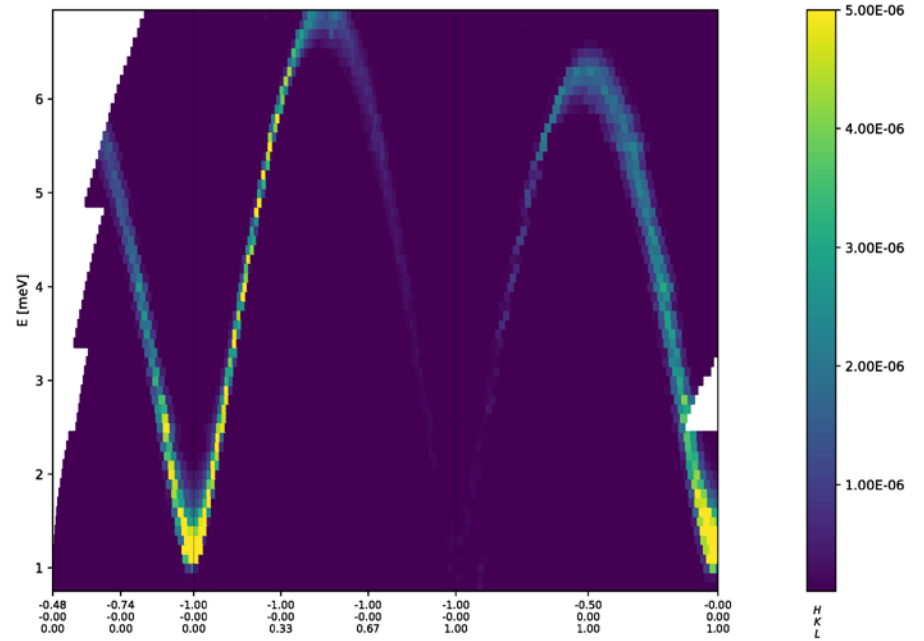
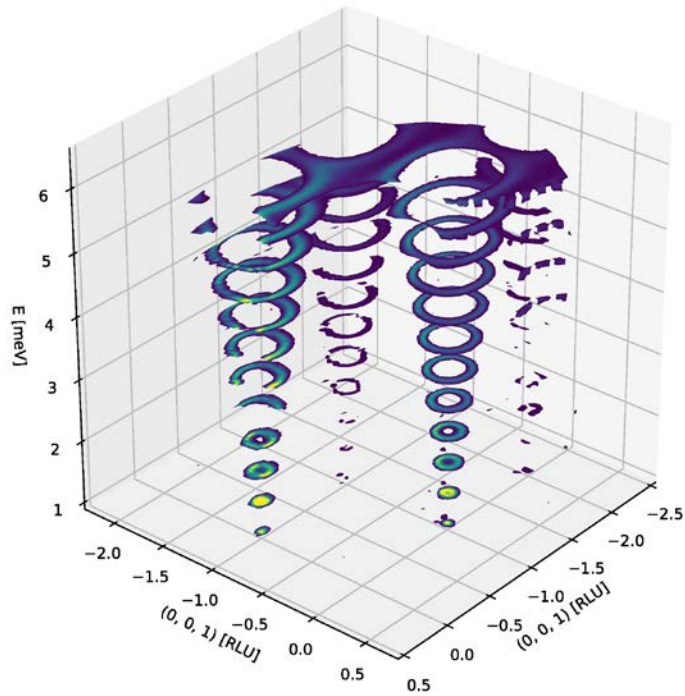
- Measurement time 5 h
- Background < 0.5 counts/min/detector

— Neutron leak  
- - - High voltage pulser

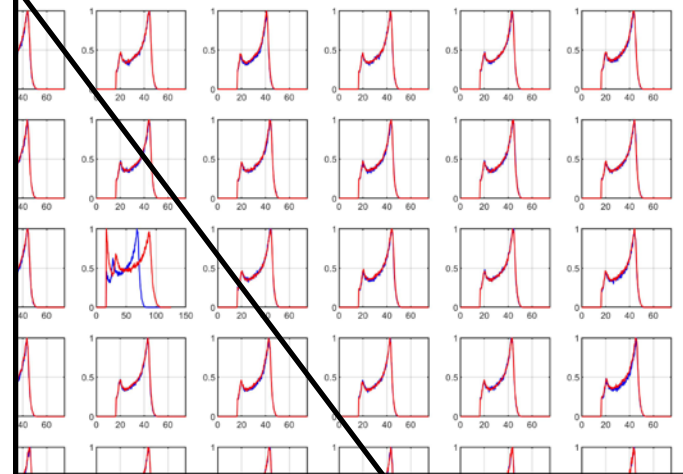
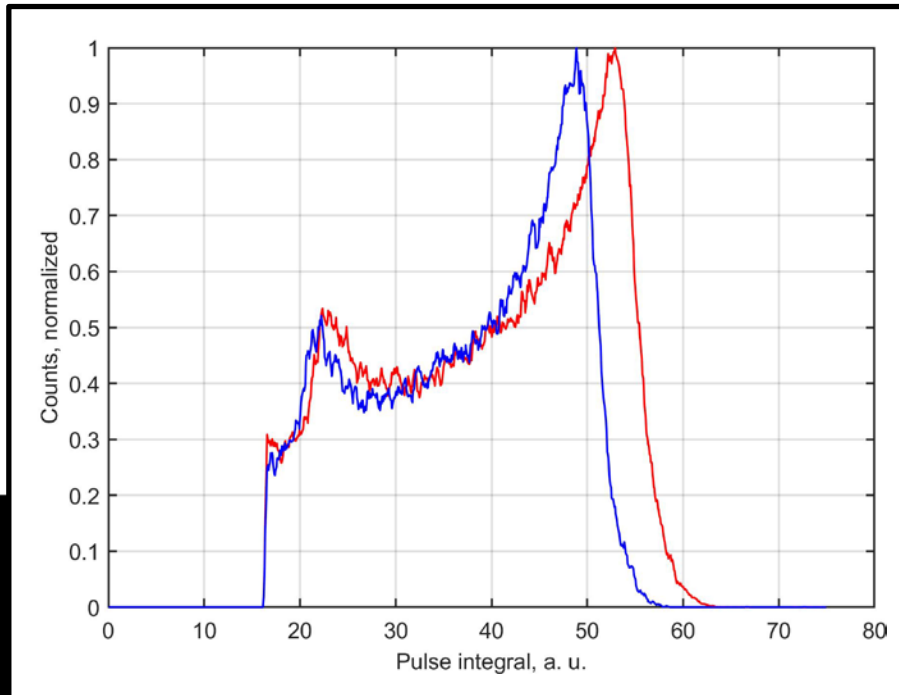
Logfiles D\_00102, E\_00231



# Spin waves in MnF<sub>2</sub>



# Detector diagnostics



Logfiles E\_00119, E\_00394

— 07.11.2018  
 — 13.12.2019

# Conclusion

- We developed a new detector readout system, using many concepts of modern digital circuit design
- Compared to previous systems, the CAMEA electronics provides:
  - A higher integration density
  - Many system parameters are programmable
  - Extended functionality (waveform download, continuous PHS acquisition, etc.)
- Commissioning of the CAMEA instrument on a tight schedule
- Two months of (nearly) uninterrupted instrument uptime

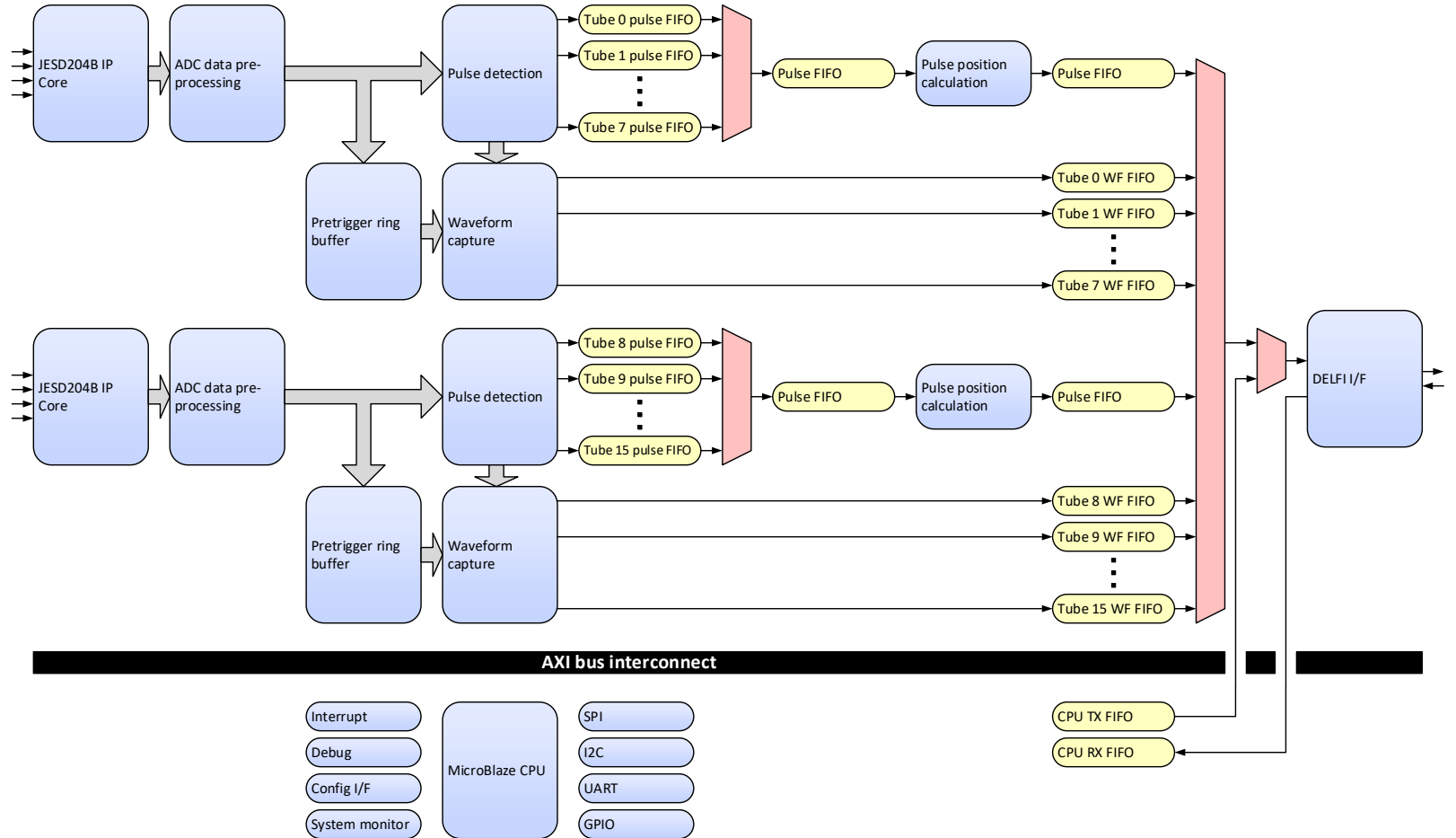
**Happy  
scientist!**



## My thanks go to

- Urs Greuter
- Gerd Theidel
- The CAMEA team:
- Dieter Graf
- Jakob Lass
- Raphael Müller
- Christof Niedermayer
- Roman Bürge
- Christian Kägi
- Manuel Lehmann
- Marcel Schild
- ...





# Commanding interface

**Common register access**

Connection state: ● ● ● ● ● ● ● ●

Commanding state: ● ● ● ● ● ● ● ●

**Pulse detection**

PULSE\_DET\_EN  
 PULSE\_POS\_EN  
 PULSE\_STATS\_EN  
 AUTO\_TRIG  
 EXT\_OVERRIDE  
 PULSE\_STATS\_RATE

**System monitor**

SYSMON\_EN  
 100000000 INTERVAL

**Test pulser**

131072 INTERVAL

**ADC conditioning**

REM\_OFFSET\_EN  
 GAIN\_EN  
 PZC\_EN

0 OFFSET  
 256 TRIG\_LVL  
 2048 GAMMA\_LVL  
 16777216 HOLDOFF  
 100000000 INTERVAL

**UDP packet generator (remote)**

UDP\_EN

48:0F:CF:53:EA:F8 MAC address  
 129.129.193.37 IP address  
 62952 Port  
 0 HOLDOFF

Disconnect  
 Read registers  
 Clear counters  
 Start log  
 DST 0

**Register access**

DST 0 DST 1 DST 2 DST 3 DST 4 DST 5 DST 6 DST 7

**WF\_ACQ\_EN**

TUBE 0  
 TUBE 1  
 TUBE 2  
 TUBE 3  
 TUBE 4  
 TUBE 5  
 TUBE 6  
 TUBE 104  
 TUBE 7  
 TUBE 8  
 TUBE 9  
 TUBE 10  
 TUBE 11  
 TUBE 12  
 TUBE 105  
 TUBE 106  
 All

**Test pulser**

TUBE 0  
 TUBE 1  
 TUBE 2  
 TUBE 3  
 TUBE 4  
 TUBE 5  
 TUBE 6  
 TUBE 104  
 TUBE 7  
 TUBE 8  
 TUBE 9  
 TUBE 10  
 TUBE 11  
 TUBE 12  
 TUBE 105  
 TUBE 106  
 All

**Amplifier enable**

TUBE 0  
 TUBE 1  
 TUBE 2  
 TUBE 3  
 TUBE 4  
 TUBE 5  
 TUBE 6  
 TUBE 104  
 TUBE 7  
 TUBE 8  
 TUBE 9  
 TUBE 10  
 TUBE 11  
 TUBE 12  
 TUBE 105  
 TUBE 106  
 All

**Offset DAC**

ADC00 -5893  
 ADC01 -5929  
 ADC02 -5958  
 ADC03 -5877  
 ADC04 -6003  
 ADC05 -5859  
 ADC06 -5912  
 ADC07 -33  
 ADC08 -36  
 ADC09 -5960  
 ADC10 -5839  
 ADC11 -5934  
 ADC12 -5906  
 ADC13 -5928  
 ADC14 -5884  
 ADC15 -5826  
 ADC16 -5825  
 ADC17 -5917  
 ADC18 -5864  
 ADC19 -5888  
 ADC20 -5831  
 ADC21 -65  
 ADC22 -5848  
 ADC23 30  
 ADC24 -38  
 ADC25 -5803  
 ADC26 963  
 ADC27 -5837  
 ADC28 -5781  
 ADC29 -5849  
 ADC30 -5819  
 ADC31 -5831

**Digital filter**

COEFF00 0  
 COEFF01 0  
 COEFF02 0  
 COEFF03 0  
 COEFF04 0  
 COEFF05 0  
 COEFF06 0  
 COEFF07 0  
 COEFF08 0  
 COEFF09 0  
 COEFF10 0  
 COEFF11 0  
 COEFF12 0  
 COEFF13 0  
 COEFF14 0  
 COEFF15 0  
 COEFF16 0

4 ADC  
 Reload  
 0 bit  
 Set dirac

**System monitor**

0x0014B40163258854 DEVICE\_DNA  
 02.00.0000 FW\_VERSION  
 02.00.0000 SW\_VERSION

**FE board id**

0x00 FE1  
 0x01 FE2

**UDP packet generator (local)**

70:B3:D5:3B:71:01 MAC address  
 129.129.193.47 IP address  
 5481 Port

ADC control Flash access

**Flash access (DST 0)**

**Panel**

Erase GLD Write GLD  
 Erase MB0 Write MB0 Write init  
 Erase MB1 Write MB1 Read init  
 Write enable

**Config state**

Golden  
 Multiboot 0  
 Multiboot 1

**Config command**

Golden  
 Multiboot 0  
 Multiboot 1  
 Reconfigure

**Read content**

Golden start  
 MB0 start  
 MB1 start  
 Init config  
 Swap bytes

Select bit file...  
 Select file

ADDR	DATA
00000000	FFFFFFFF
00000004	FFFFFFFF
00000008	FFFFFFFF
0000000C	FFFFFFFF
00000010	FFFFFFFF
00000014	FFFFFFFF
00000018	FFFFFFFF
0000001C	FFFFFFFF
00000020	B8000000
00000024	44002211
00000028	FFFFFFFF
0000002C	FFFFFFFF
00000030	665599AA
00000034	00000020
00000038	01E00330
0000003C	68020000
00000040	01800030
00000044	12000000
00000048	00000020
0000004C	01200230
00000050	00000000

**ADC control (DST 0)**

ADC 0	ADC 1	ADC 2	ADC 3	ADC 4	ADC 5	ADC 6	ADC 7	ADC 8	ADC 9	ADC 10	ADC 11	ADC 12	ADC 13	ADC 14	ADC 15	ADC 16	ADC 17	ADC 18	ADC 19	ADC 20	ADC 21	ADC 22	ADC 23	ADC 24	ADC 25	ADC 26	ADC 27	ADC 28	ADC 29	ADC 30	ADC 31
<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	<input checked="" type="radio"/> Sample <input type="radio"/> All zeros <input type="radio"/> All ones <input type="radio"/> Ramp	

ADC 15 ADC 6  
 ADC 13 ADC 2  
 ADC 11 ADC 4  
 ADC 9 ADC 6  
 ADC 14 ADC 1  
 ADC 12 ADC 3  
 ADC 8 ADC 5  
 ADC 8  
 ADC 7  
 ADC 16 ADC 31  
 ADC 18 ADC 29  
 ADC 28 ADC 27  
 ADC 22 ADC 25  
 ADC 17 ADC 30  
 ADC 19 ADC 28  
 ADC 21  
 ADC 26  
 ADC 23  
 ADC 24  
 All  
 All