Powering and Cabling of the Pixel Tracker

With an emphasis on (space) constraints.

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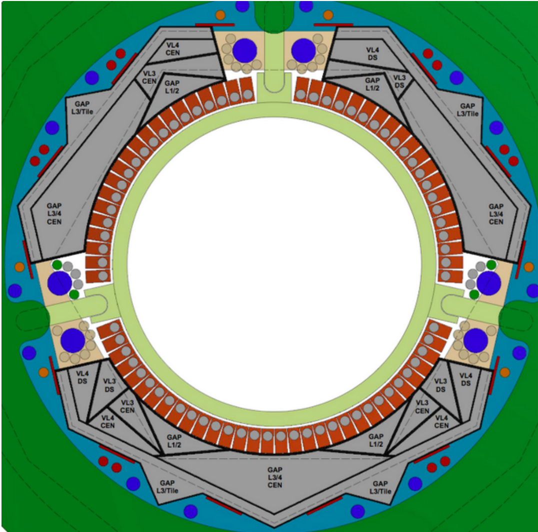
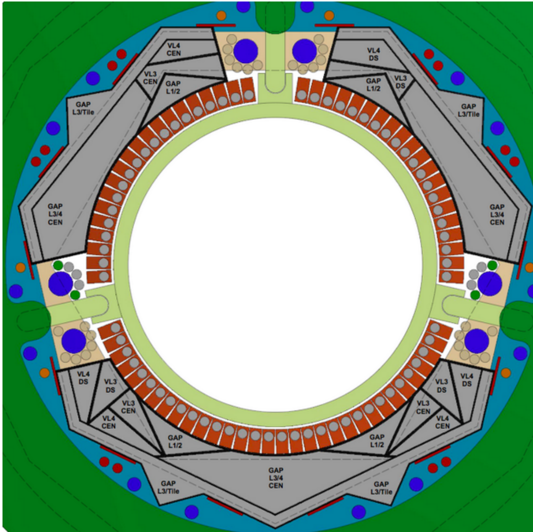
Space constraints in experiment



This is a cut view of the beampipe.

Innermost ring: beampipe. O.D. 66 mm

Space constraints in experiment



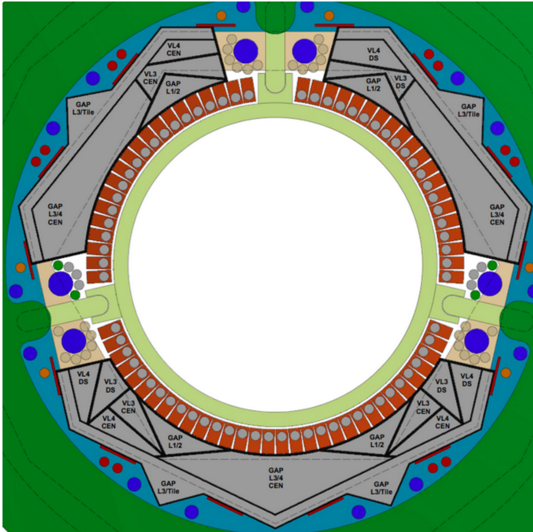
Power is brought in through copper bars, $5 \times 2.5\,\mathrm{mm}^2$.

72 bars = 36 circuits. 30 for pixels, 6 for SciFi.

This gives nearly maximum packing density.

We cannot offer more circuits, cannot go below 2.5 mm in width. Mechanical limit.

Space constraints in experiment



Data lines are bundles of 50 micro-twisted pair lines.

Placed around the 6 blue cooling lines.

brown: 26 for pixel L3/4,
green: 4 for vertex pixel,
grey: 6 for SciFi

Space constraints in experiment

This is a cut where two L3/4 barrels meet.

Space constraints in experiment

And this is essentially all the space left for cable routing.

Power and data.

HDI power distribution layer options in a nutshell

HDI layer stack in LTU technology:

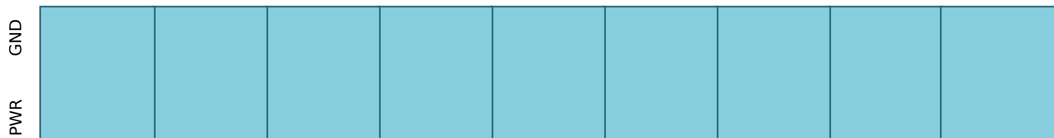
Aluminium thickness: 12 μm, two conducting layers.

HDI power distribution layer options in a nutshell

LTU aluminium technology has a few limitations:

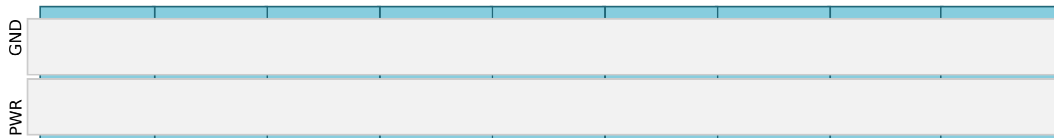
- Aluminium thickness in commercially available foil thicknesses (12 µm=1/2 mil, 25 µm=1 mil etc.)
- Smallest feature size (trace, land): 63 µm
- Available feature sizes are in fractions of 7 µm
- Vias are consuming lots of space (along trace direction $\gtrapprox$ 600 µm). Their count should be minimized.

HDI power distribution layer options in a nutshell



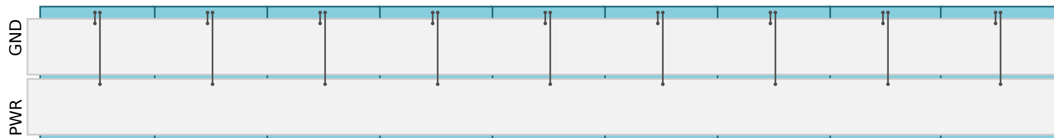
You want to power 9 chips in a ladder

HDI power distribution layer options in a nutshell



Simple approach: a power and a ground line...

HDI power distribution layer options in a nutshell

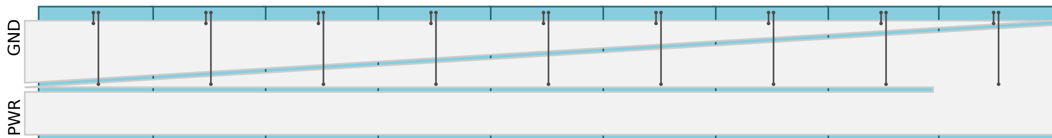


. . . and you connect them with stubs (in other layer)
Disadvantage: Every chip sees a different rail voltage.

HDI power distribution layer options in a nutshell

Bringing in one line to the end seems like an interesting option
but burns more power and voltage accross chips still not uniform

HDI power distribution layer options in a nutshell



With this you make sure that every chip sees the same voltage but still at roughly $1.5^2 = 2.3\times$ the power loss.

HDI power distribution layer options in a nutshell

Providing power to groups of chips are possible. Within a group, voltage drops are unavoidable. The groups can be leveled by different trace widths (only equal case shown here).

Within a group, chicanes can be added to equalize voltage drop, at expense of power loss.

HDI power distribution layer options in a nutshell

The specific resistance of Aluminium is

$$\rho_{\mathrm{Al}} = 2.65 \times 10^{-2} \, \frac{\Omega \, \mathrm{mm}^2}{\mathrm{m}} \tag{1}$$

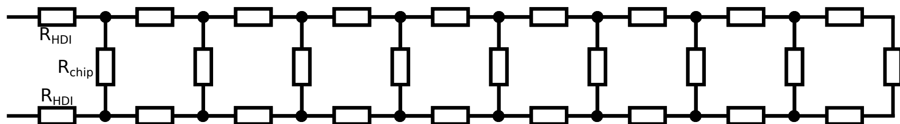
The cross-section of a 10 mm wide trace (half the ladder width) is

$$A = w \cdot h = 10 \, \mathrm{mm} \cdot 0.012 \, \mathrm{mm} = 0.12 \, \mathrm{mm}^2 \tag{2}$$

Hence for a trace between two chips ($l = 20 \, \mathrm{mm}$) we get

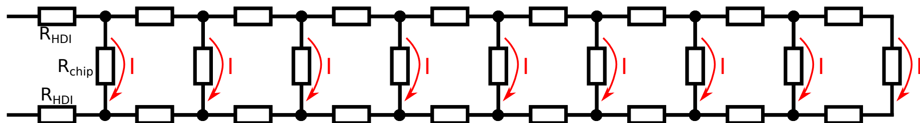
$$R = \frac{\rho_{\mathrm{Al}} \cdot l}{A} = 4.4 \, \mathrm{m}\Omega \tag{3}$$

HDI power distribution layer options in a nutshell



This is the simplified schematic. R_{HDI} is the resistance of the trace between neighbouring chips, R_{chip} means the chip load.

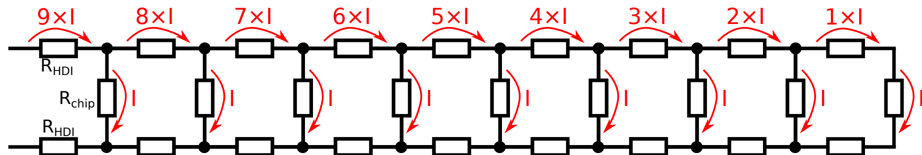
HDI power distribution layer options in a nutshell



Simplified assumption: Every chip draws the same (constant) current.

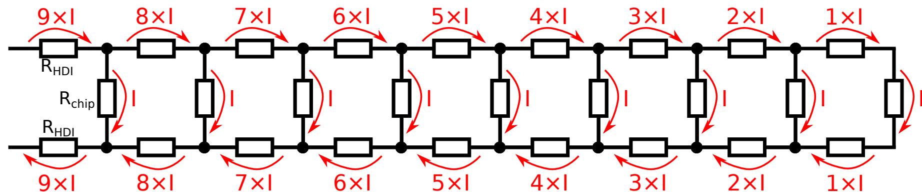
NOTE: Yes, I do know that the chip is a much more complicated load with possible feedback behaviour.

HDI power distribution layer options in a nutshell



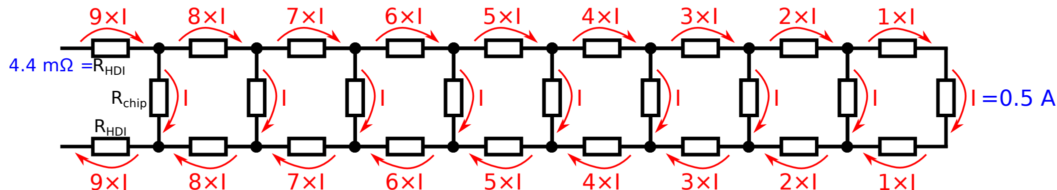
In the simple approach, the currents add on the same line.

HDI power distribution layer options in a nutshell



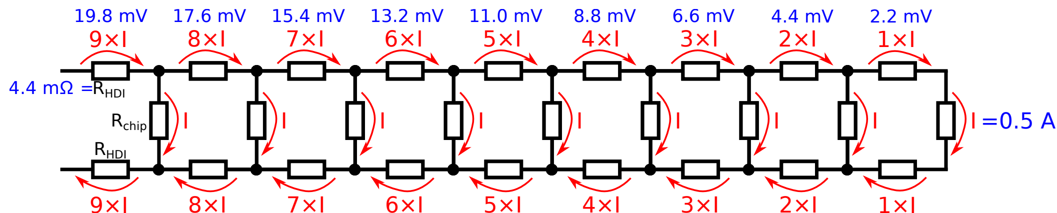
And on ground too.

HDI power distribution layer options in a nutshell



Let's do an example. The 44 mΩ is the expected R for 2 cm long trace, 10 mm wide and 12 µm thick.

HDI power distribution layer options in a nutshell



The values in blue give the voltage drops accross the 20 mm long path.

HDI power distribution layer options in a nutshell

ΔU = 99 mV

19.8 mV 17.6 mV 15.4 mV 13.2 mV 11.0 mV 8.8 mV 6.6 mV 4.4 mV 2.2 mV

9×I 8×I 7×I 6×I 5×I 4×I 3×I 2×I 1×I

4.4 mΩ = R_{HDI}

R_{chip}

R_{HDI}

I I I I I I I I I = 0.5 A

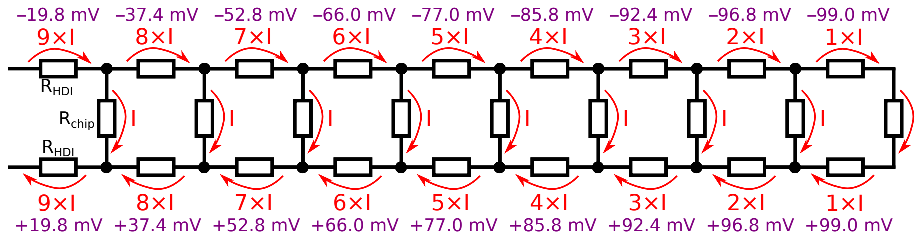
9×I 8×I 7×I 6×I 5×I 4×I 3×I 2×I 1×I

19.8 mV 17.6 mV 15.4 mV 13.2 mV 11.0 mV 8.8 mV 6.6 mV 4.4 mV 2.2 mV

ΔU = 99 mV

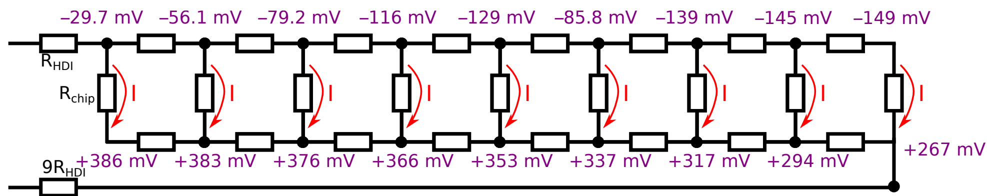
On ground too. Overall, almost 100 mV power drop on each rail for the last chip in the row.

HDI power distribution layer options in a nutshell



Lets add the voltage drop for every chip individually. Not nice.
Power loss in this case: 450 mW per half-ladder (50 mW per chip on average).

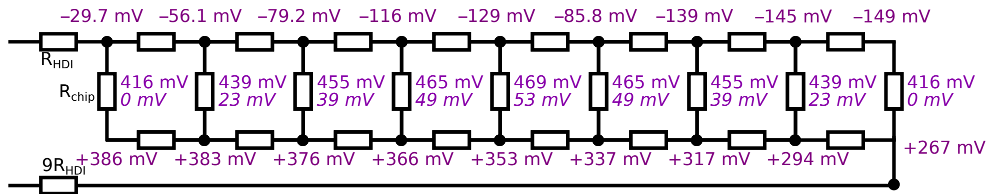
HDI power distribution layer options in a nutshell



The option with bringing in one rail from the end. No surprise: total losses higher (50% less cross section).

Power loss in this case: 1520 mW per half-ladder (170 mW per chip on average).

HDI power distribution layer options in a nutshell



This flattens the voltage drop spread. Every chip is floating on its own ground. Fine. For the triangular shaped traces, the voltage drops would be equal for every chip and the power loss is similar.

HDI power distribution layer options in a nutshell

Here is a material budget drilldown for pixel layers:

	Layer 1-2		Layer 3-4	
	thickness [μm]	X/X_0	thickness [μm]	X/X_0
MuPix Si	45	0.48×10^{-3}	45	0.48×10^{-3}
MuPix Al	5	0.06×10^{-3}	5	0.06×10^{-3}
HDI polyimide & glue	45	0.18×10^{-3}	45	0.18×10^{-3}
HDI Al	25	0.28×10^{-3}	28	0.28×10^{-3}
Polyimide support	25	0.09×10^{-3}	≈ 30	0.10×10^{-3}
Adhesives	10	0.03×10^{-3}	10	0.03×10^{-3}
Total	158	1.12×10^{-3}	163	1.13×10^{-3}

We miss the target a bit. But after we built that detector we will elarn where we can optimise more.

Conclusions

- Space is very restricted.
- Number of circuits cannot be expanded. Would need to merge power groups (1 half-module = one power group)
- Readout cables: space also very limited. Cannot go thicker.
  NB: HV cables not in drawing, additional lines for 3.3 V SciFi not in drawing
- Choice of aluminium flex imposes restrictions. Large voltage drop unavoidable. More layers or copper is no alternative (material).
- Power losses are non-uniform, i.e. higher towards the ladder ends. **Not yet modeled in cooling simulations.**
  The more structures used to equalize voltage drop, the worse the conductor to insulator ratio.
- Calculations shown are indicative and simplified. Final option requires detailed case studies with simulation and prototypes.

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