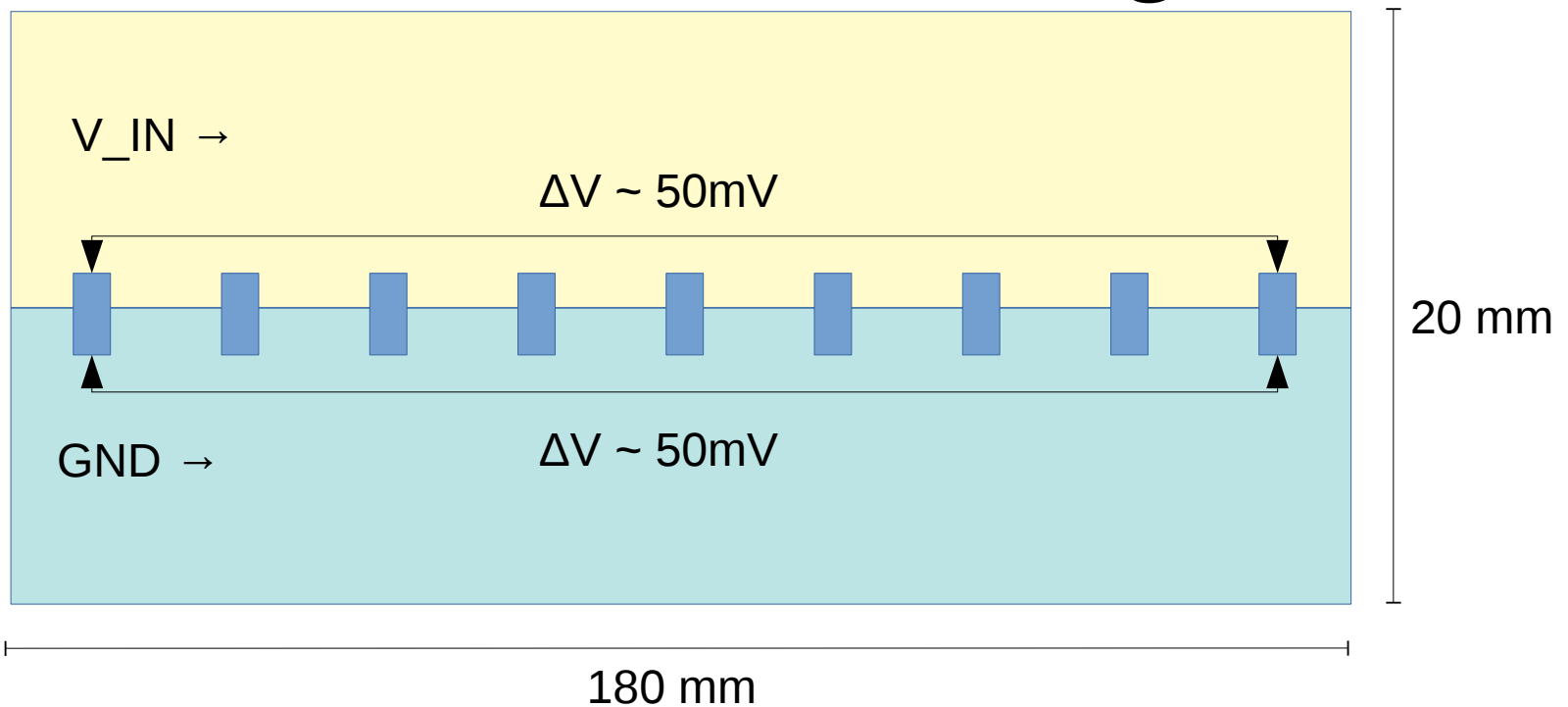
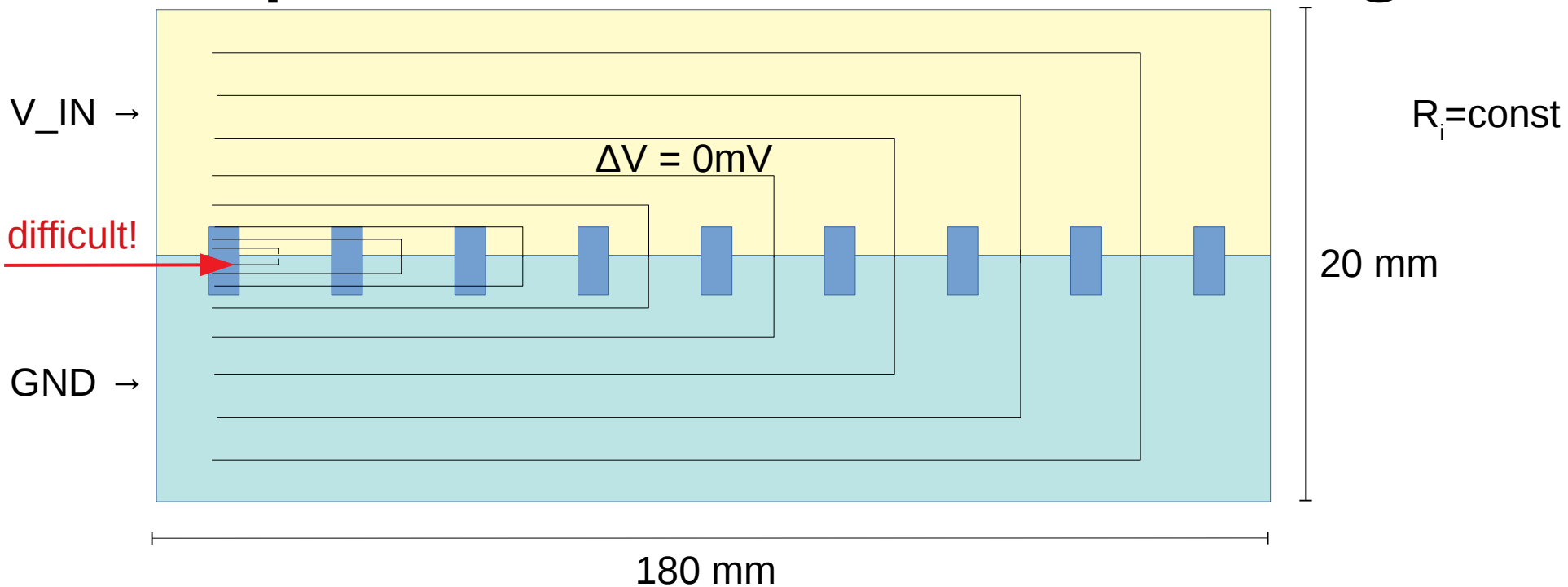
“Naive” Routing



- The “naive” routing scheme **minimizes** overall the power loss: **P_{loss}=375mW**
- The summed voltage drop between sensor 1 and 9 is 2 x 50 = 100mV

$$\mathbf{P_{loss} = 2 \cdot R_0 (I_0)^2 \cdot g}\ , \quad R_0 = 2.2\text{m}\Omega\ ,\ I_0 = 0.5\text{A}\ ,\ g = 342 \text{ (geometrical factor)}$$

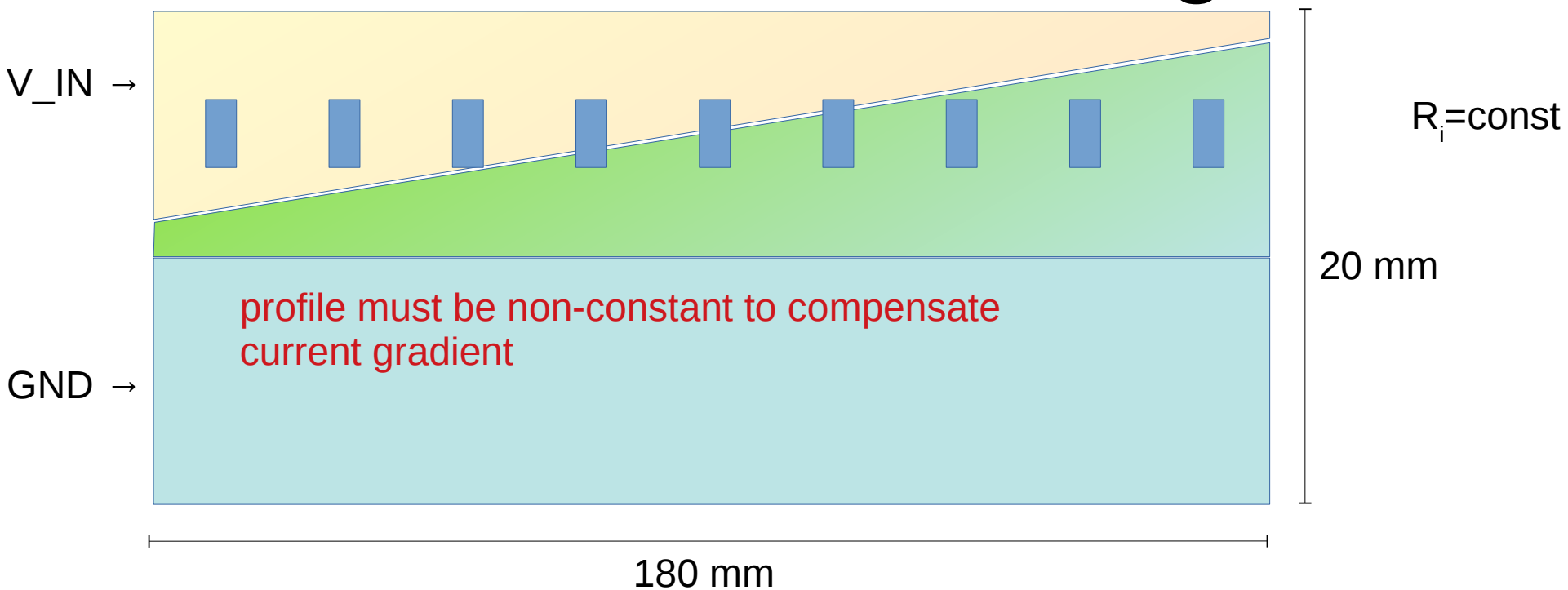
“Equal Resistance” Routing



- The “naive” routing scheme avoids voltage drops between chips; **ΔV = 0mV, V_{loss}= 2 x 50mV**
- Power loss is about **450mW**

$$P_{loss} = 2 \cdot R_0 (I_0)^2 \cdot g \;, \quad R_0 = 2.2 m\Omega \;, \; I_0 = 0.5A \;, \; g = n \cdot n(n+1)/2 = 405 \text{ with } n = 9$$

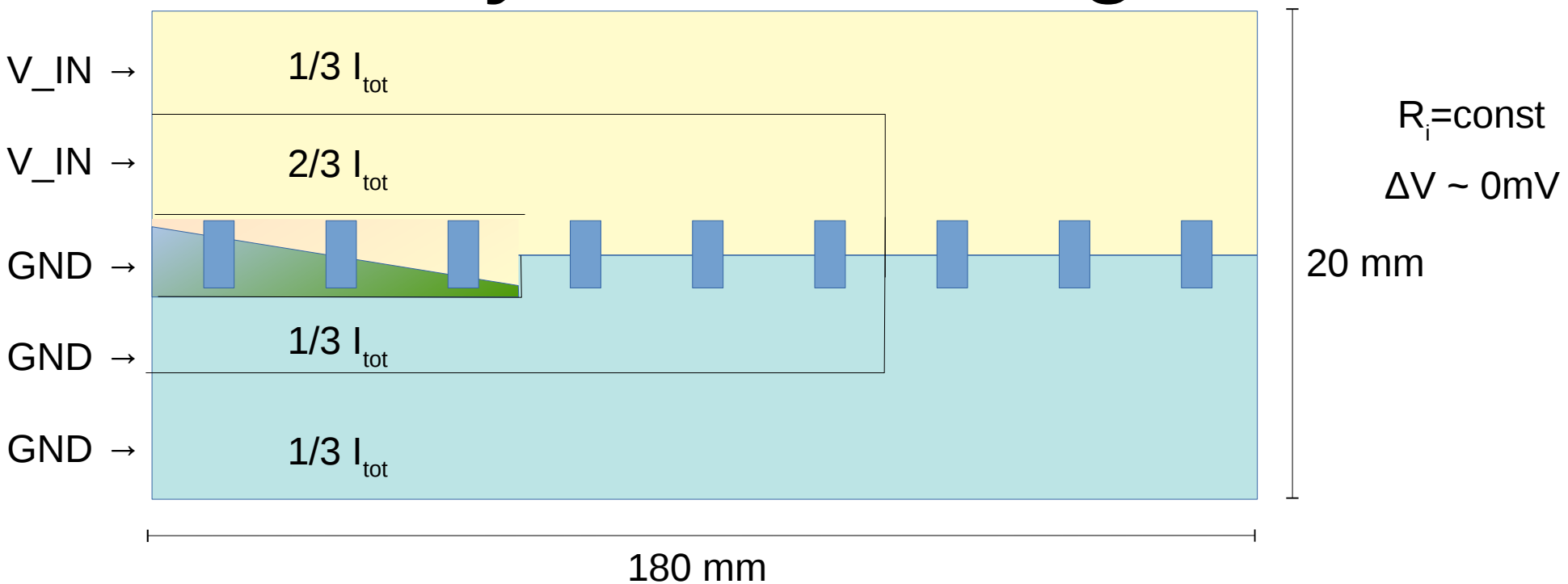
“Telemann” Routing



- This routing scheme **avoids** relative voltage drops between chips; but relative large voltage loss of $\mathbf{V_{loss} = 2 \times 90mV}$, all chips on slightly different potential
- Power loss is about **800 mW**

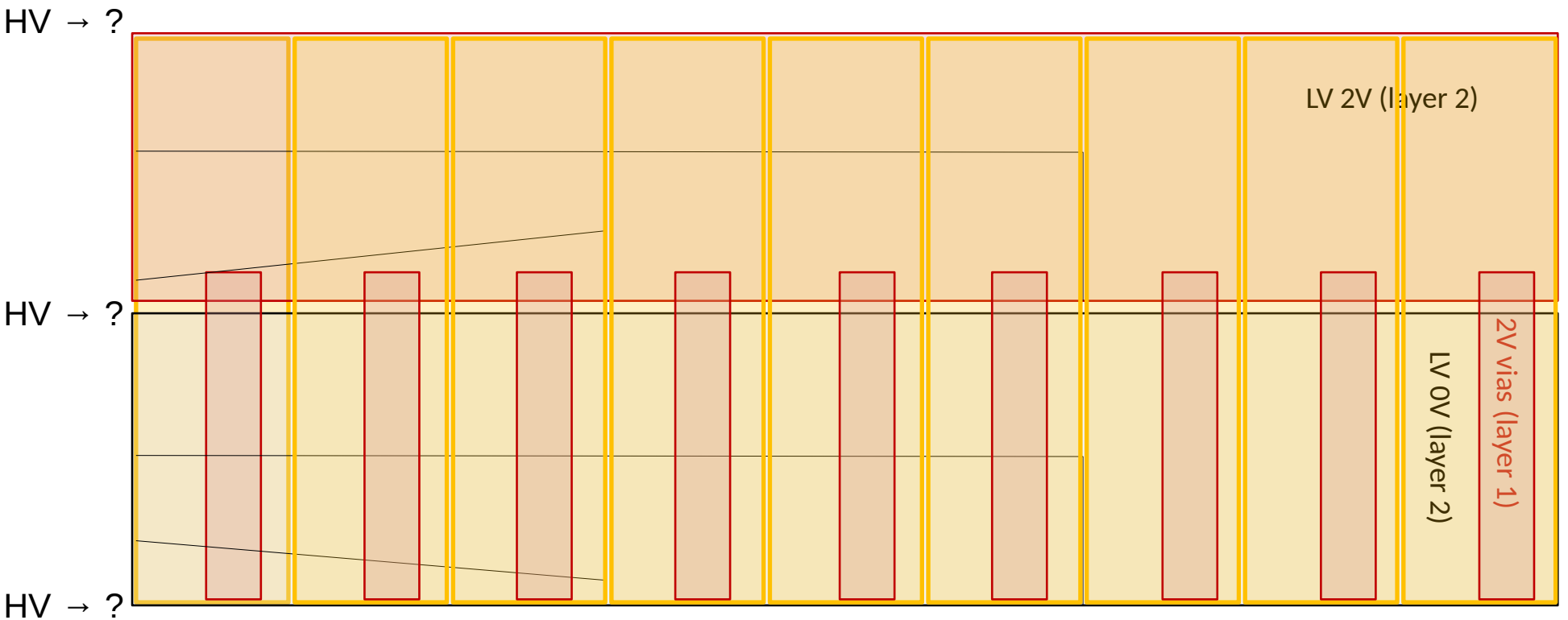
$$\mathbf{P_{loss} = 2 \cdot R_0 (I_0)^2 \cdot g}\ , \quad R_0 = 2.2m\Omega\ ,\ I_0 = 0.5A\ ,\ g = n \cdot n^2 = 729 \text{ with } n = 9$$

“Hybrid” Routing



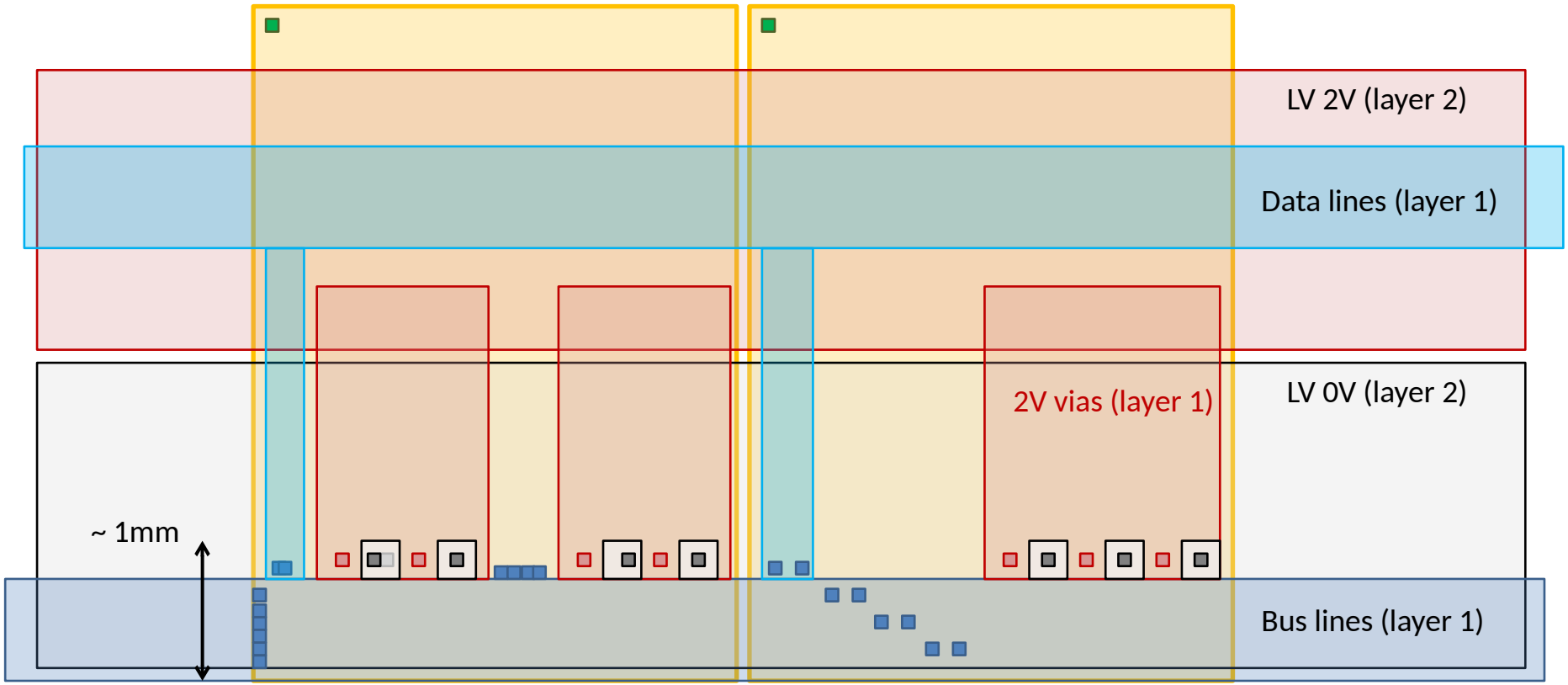
Mixture of “naive”, “equal” and “teleman” methods

Applied on HDI Design



possible and easy!

Richard's Slide



Summary

- Voltage drops can be avoided by simple HDI design changes
- Exact area proportions to be simulated

Backup

Summary Table

Routing schemes:

1) Naive Routing → needs 2 SF (no Zener) for all currents to level out voltage drops
2) Equal Resistance → needs 1 SF for all PLL and VSSA
3) Teleman → dito
4) Hybrid (Combination of 2.+3.) → dito

Scheme	P_{loss}(HDI)	#SF current	P_{loss}(SF) per chip	P_{loff}(total)	normalised to 9 Watt
Naive	375 mW	2 x 430mA @0.2-0.5V 2 x 70mA @0.8V	170-430 mW 110 mW	2.9-5.2 W	32% - 58%
Equal	440 mW	1 x 70mA @0.8V	56 mW	0.95 W	11%
Teleman	800 mW	1 x 70mA @0.8V	56 mW	1.30 W	14%

Pixel Tracker Voltage Drops and Power Consumption

- Voltage drops on LTU-HDI due to ohmic resistance
  - spec. resistance ρ_{alu} = 2.65 10^{-2} Ω mm^2/m (2.8?)
  - trace width 10mm, thickness 12µm → **2.2mΩ/cm** (oxide?)
  - Mupix power MPV=250 mW/cm^2 for V=2V, area=4cm^2 → I_{Mupix}=0.5A (rough estimated)

- Voltage loss in 10mm wide trace over full ladder (18cm) for 9 Mupix is **U_{Δ} =200mV** (defines scale and worst case scenario)
- Counter measures:
  - improve HDI routing
  - use on chip voltage regulators to compensate voltage drops

- Goal: Minimize voltage drops (→ reliability) and total power consumption (→ cooling)
- Note: power consumption is the results of **loss** in traces and **voltage regulators**!

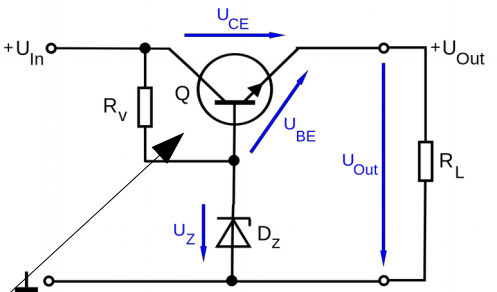
On chip Voltage Regulators

- Purpose of voltage regulators:
  - ➔ regulate voltage (mitigate power drops)
  - ➔ stabilize voltage

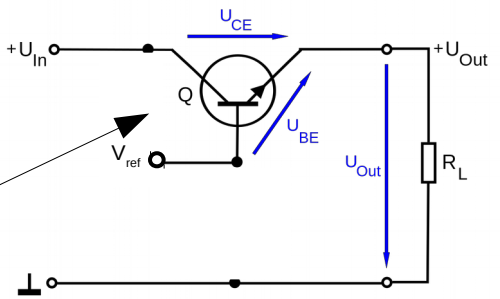
- Types of voltage regulators:
  - Zener diode
  - source follower
  - shunt (for serial powering only)

- For parallel powering (Mu3e) the source follower design is best suited
- However voltage drop of **0.2-0.5V** per SF!

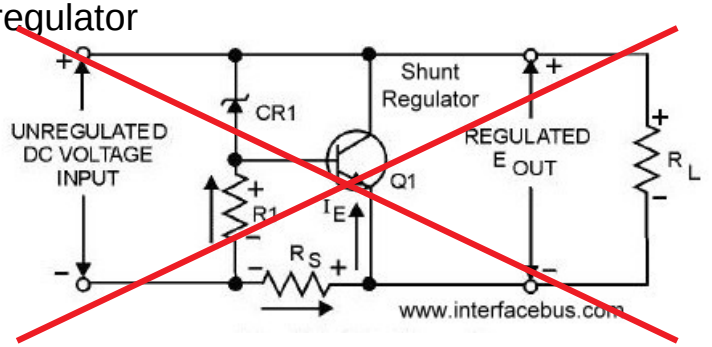
reference with Zener diode



reference external



shunt regulator



Mupix Voltage Stabilization

Remark: I define a voltage as “stable” if it is stable against GND (noise is filtered out).
If GND is noise the voltages must see the same noise!

digital VDD=1.8V:	→ level critical	~190 mA
analog VDDA=1.8V:	→ level critical	~140 mA
amplifier VSSA=1.0V:	→ **stable!**	~65 mA
LVDS driver:		~15 mA /per link
PLL:	→ **stable!**	small

- Life becomes easier if on PLL and VSSA are stabilized using voltage regulators
- Could work if voltage levels are stabilized by clever HDI routing