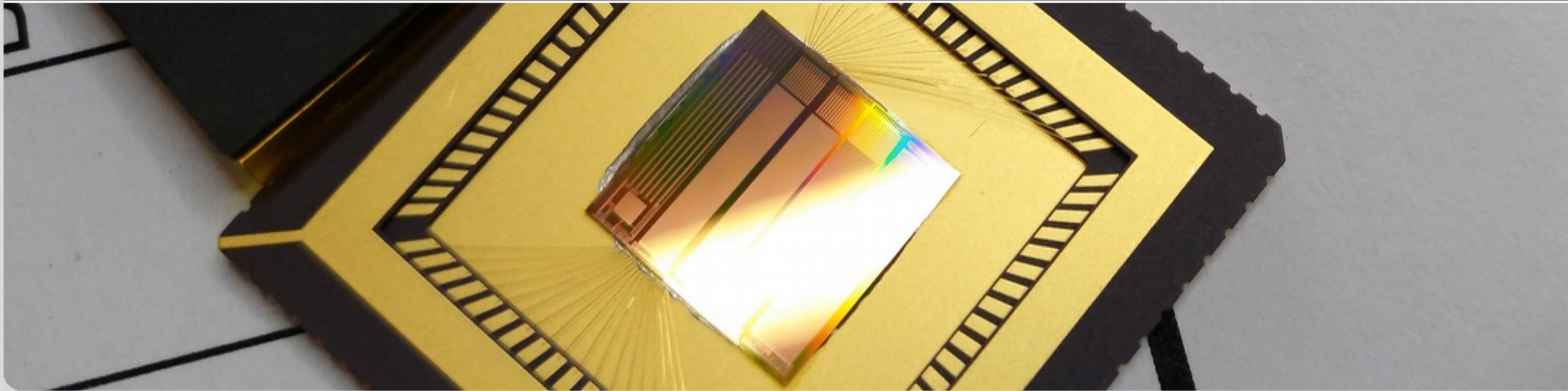


First Measurements on ATLASPix3

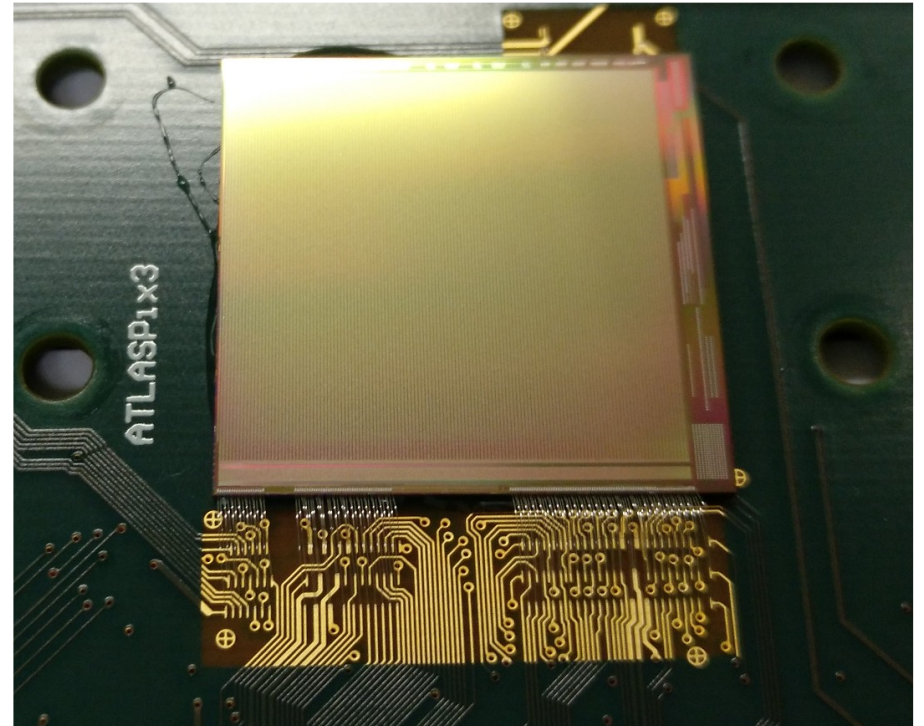
Rudolf Schimassek

Institute for Data Processing and Electronics (IPE)



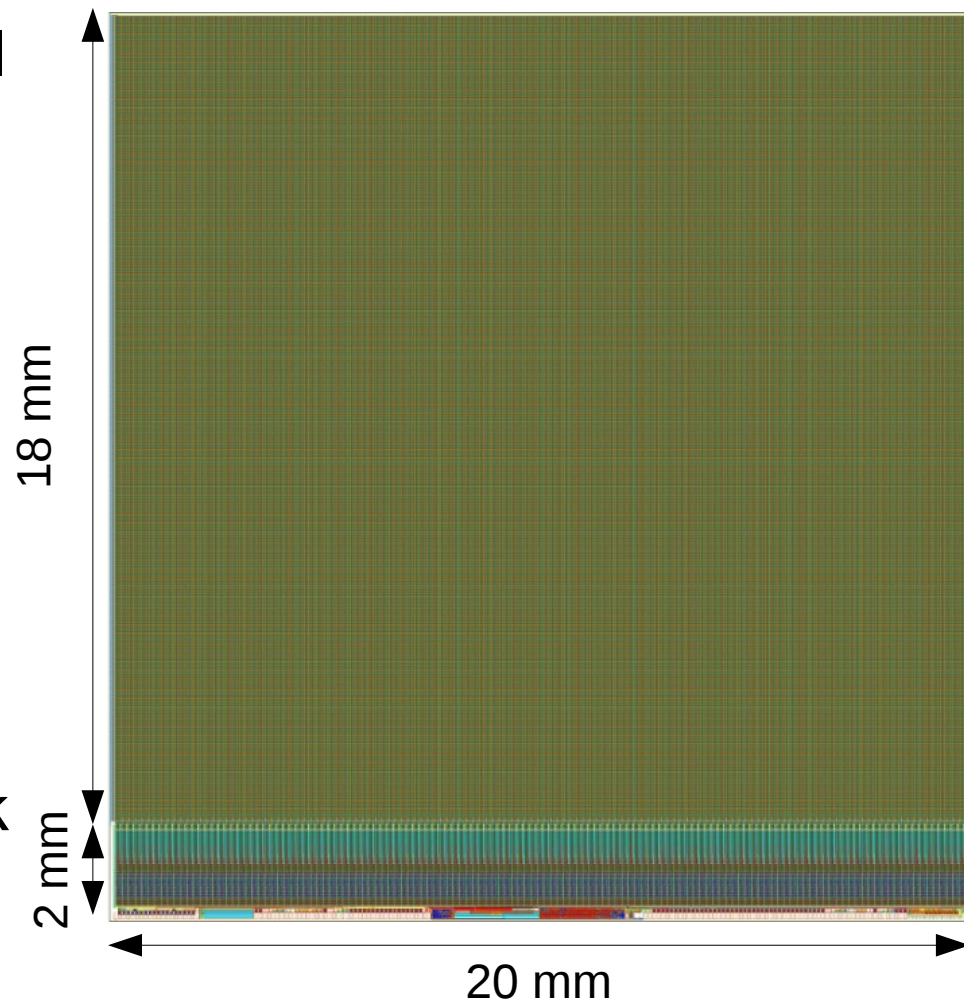
Outline

- ATLASPix3
- IV characteristics
- Power Regulators
- Untriggered Readout
- Matrix Trimming



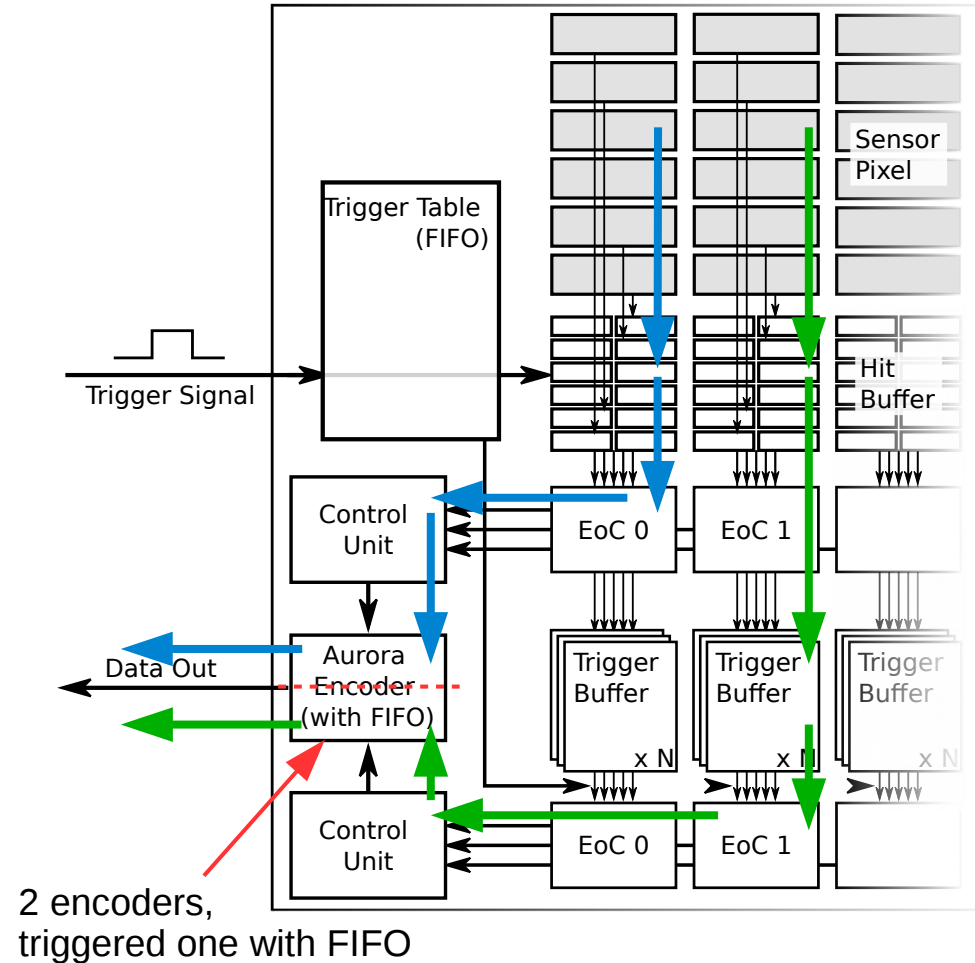
ATLASPix3

- Single matrix: 132 x 372 pixel
 - Pixel size 150 x 50 μm^2
- Column drain readout with and without trigger
- Radiation hard design with SEU tolerant global memory
- In-pixel comparator
- 64/66 bit Aurora encoder
- Command decoder with clock recovery



ATLASPix3 – Readout Structure

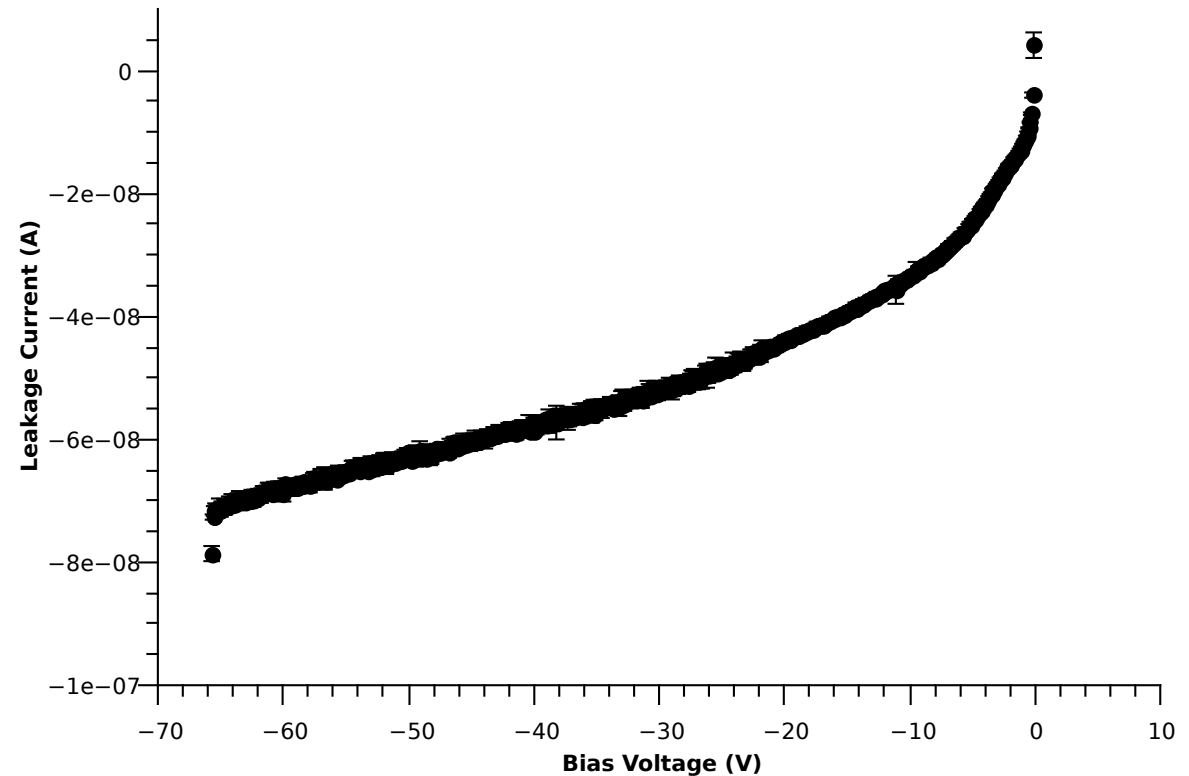
- **Triggered** and **triggerless** readout possible via two concurrent readout structures
 - separate control units
 - Configuration via SEU tolerant registers
- **Data transmitted:**
 - triggerless: 8/10b Aurora encoded
 - triggered: 64/66b Aurora encoded



IV Characteristics

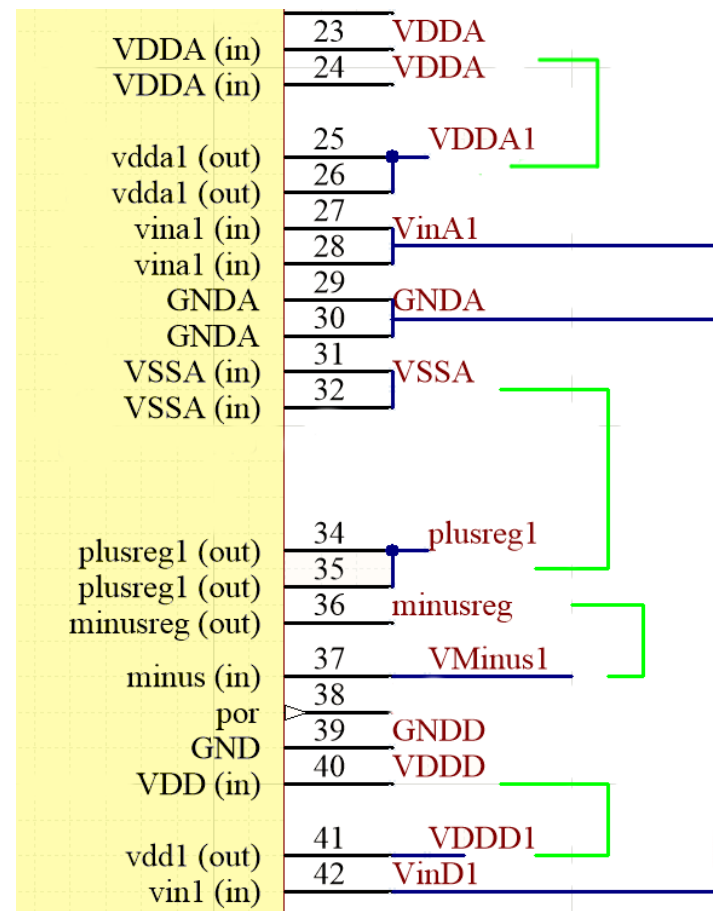
- Low leakage current of $< 50 \text{ nA}$ @ -20 V
- Breakdown at -65.8 V
 - Chip powered during measurement
 - Current jumps to compliance ($100\mu\text{A}$)

IV-Curve for ATLASPix3 Sample AP3.2



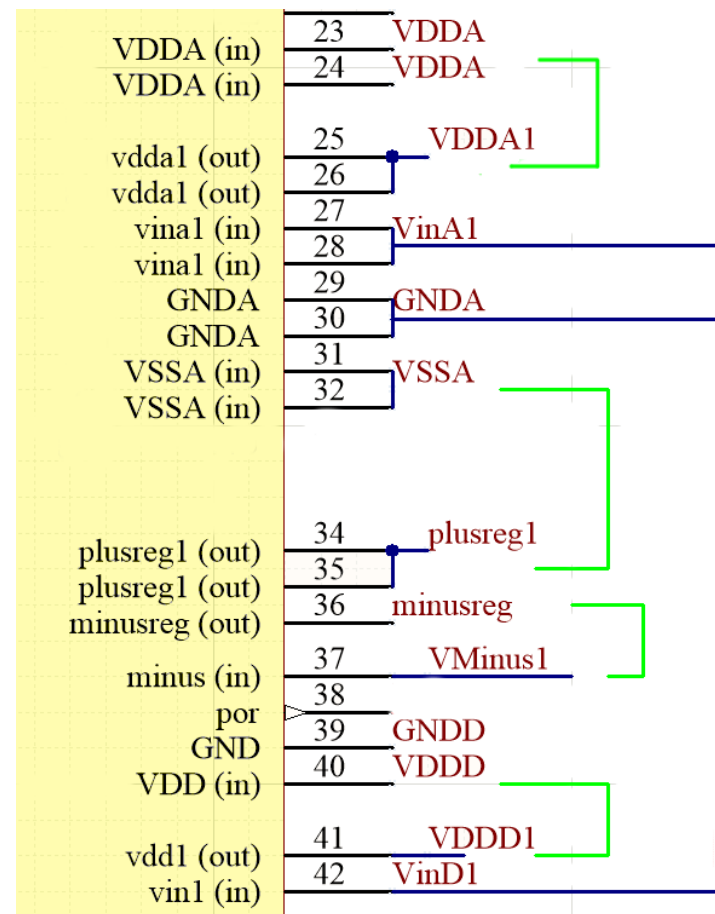
Power Regulators

- ATLASPix3 has regulators for
 - V_{DD}
 - V_{DDA}
 - V_{plus}
 - V_{minus}
- Implemented as optional feature
- All regulators have tuning means



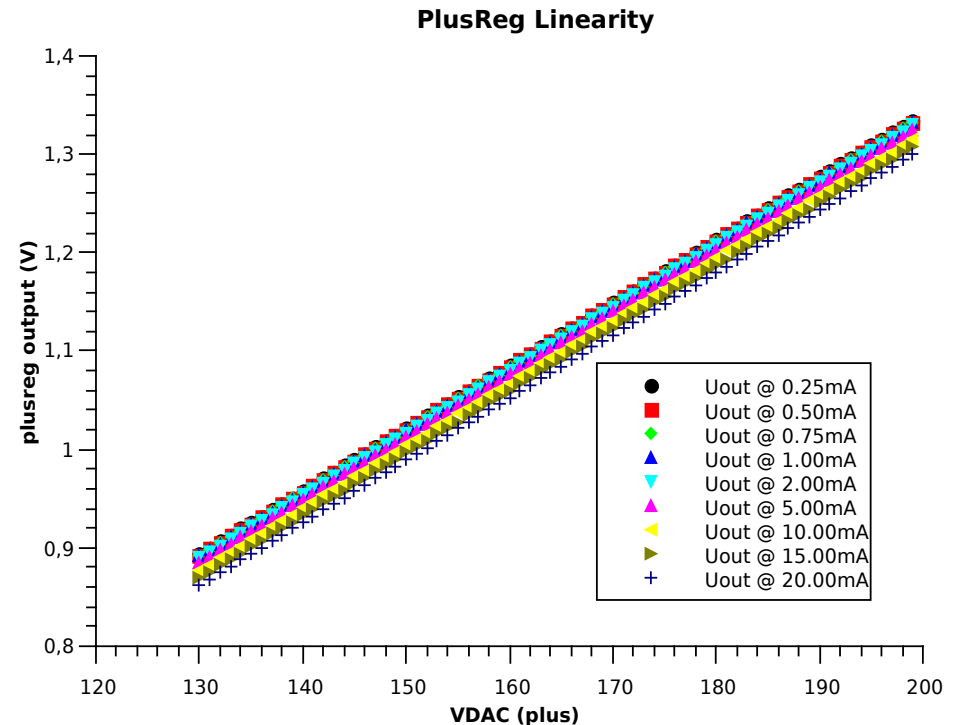
Power Regulators – V_{plus} , V_{minus}

- Regulators for V_{plus} and V_{minus} use V_{DDA} as supply voltage
- Can be configured using voltage DACs
- Behaviour similar, therefore only plots for V_{plus} are shown



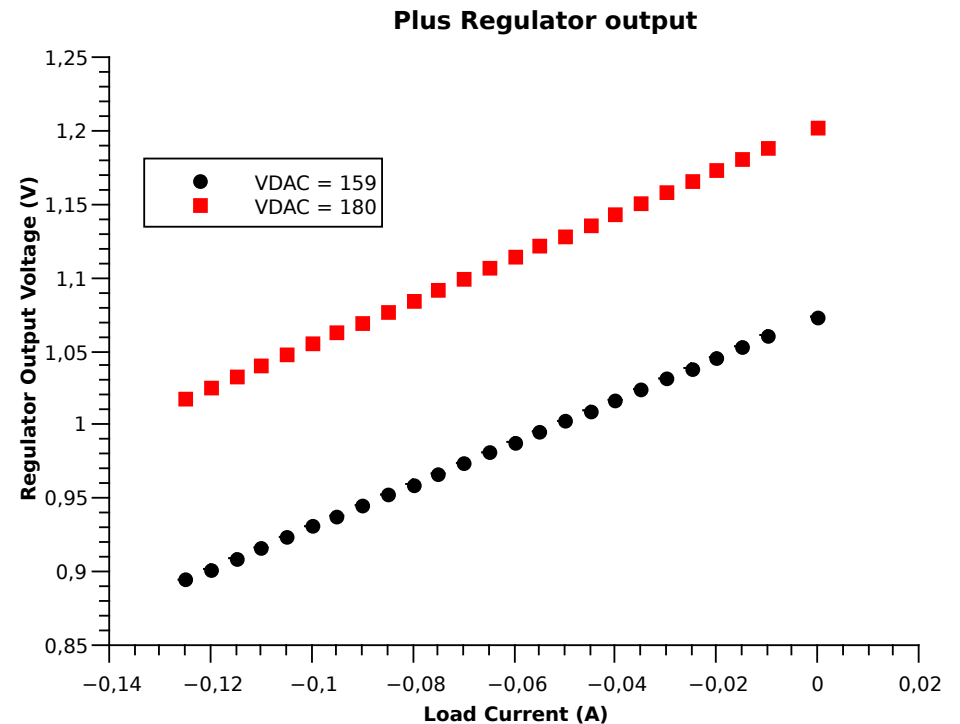
Power Regulators – V_{plus}

- Both regulators show good linearity with the voltage DAC controlling them
- A small series resistance of about 1Ω is visible



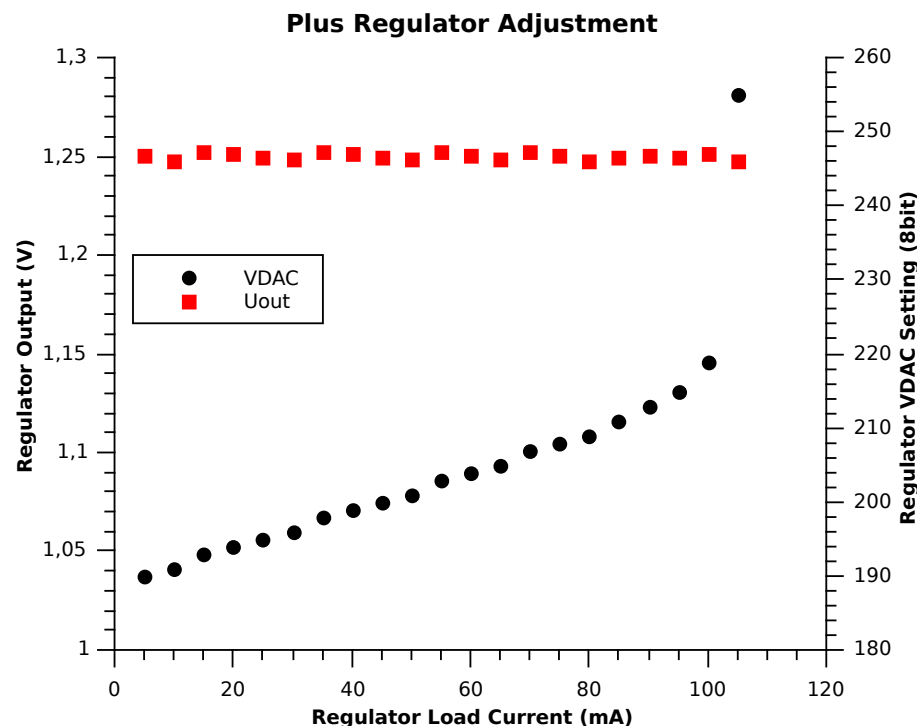
Power Regulators – V_{plus}

- Both regulators show good linearity with the voltage DAC controlling them
- A small series resistance of about 1Ω is visible
 - Probably in the measurement setup, not the chip itself
- Currents above 100 mA drawn for testing



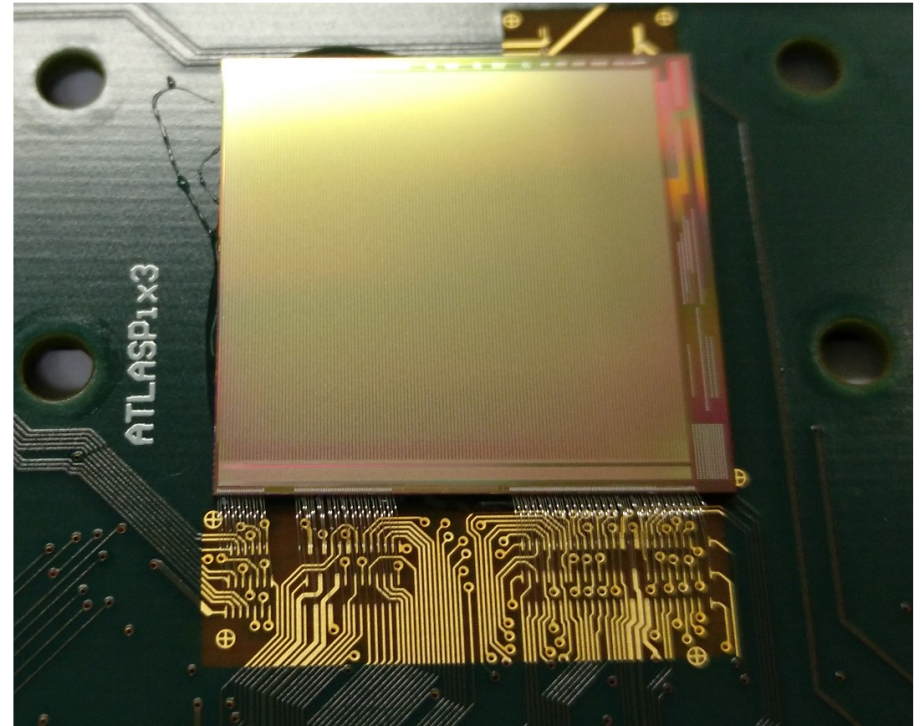
Power Regulators – V_{plus}

- Stable voltage achieved by adjusting the VDAC setting
- 100 mA output for 1.25 V achieved
 - About V_{SSA} power consumption for unoptimised settings
- Untriggered Readout working with V_{SSA} provided from plusreg
 - At 100 mA, V_{SSA} can be increased above 1.25 V with VDAC > 180
 - Strong indication that the series resistance was in the measurement setup not in the regulator



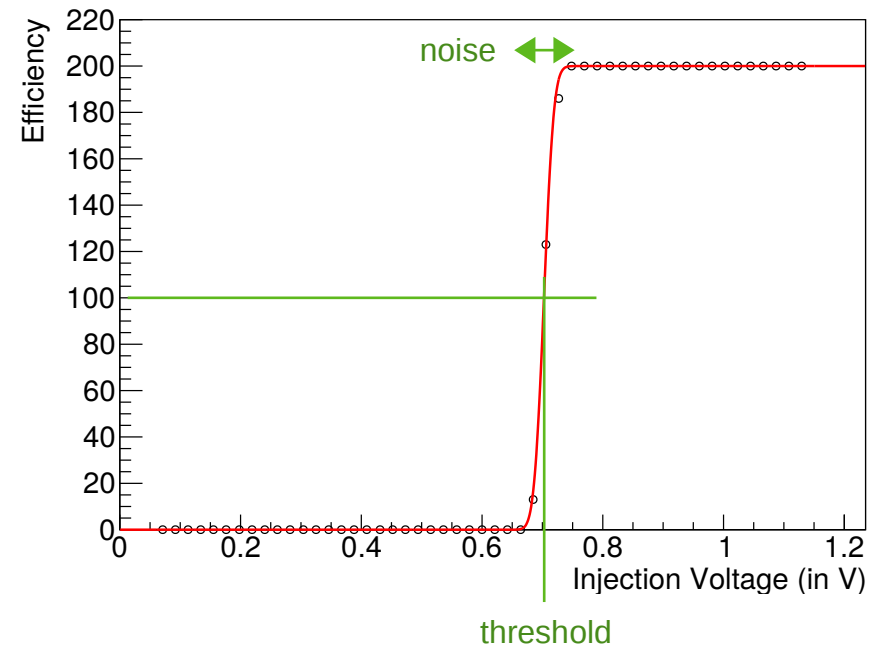
Configuration and Readout

- Serial and SPI configuration tested to work
- RAM writing is working
- Reference clock output works
- Untriggered readout tested to work at 400 Mbps (DDR, results in 25 ns time stamp)



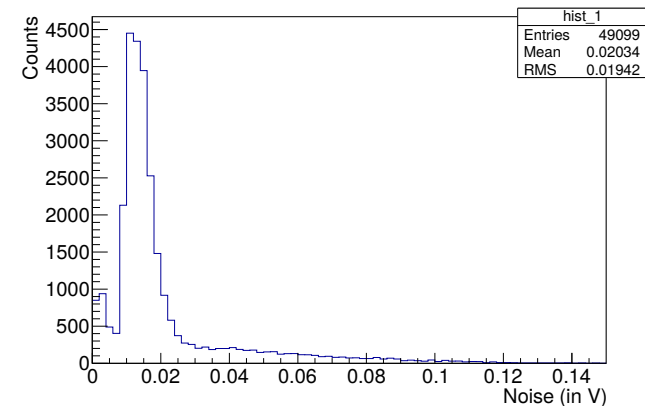
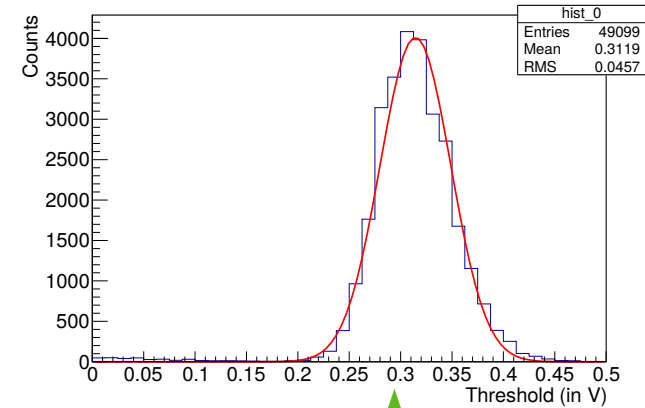
Threshold and Noise Definitions

- Charge injections of increasing strength are sent into a pixel
- Count number of detected signals \rightarrow detection efficiency
- Shifted and scaled gaussian error function is fitted to the data points



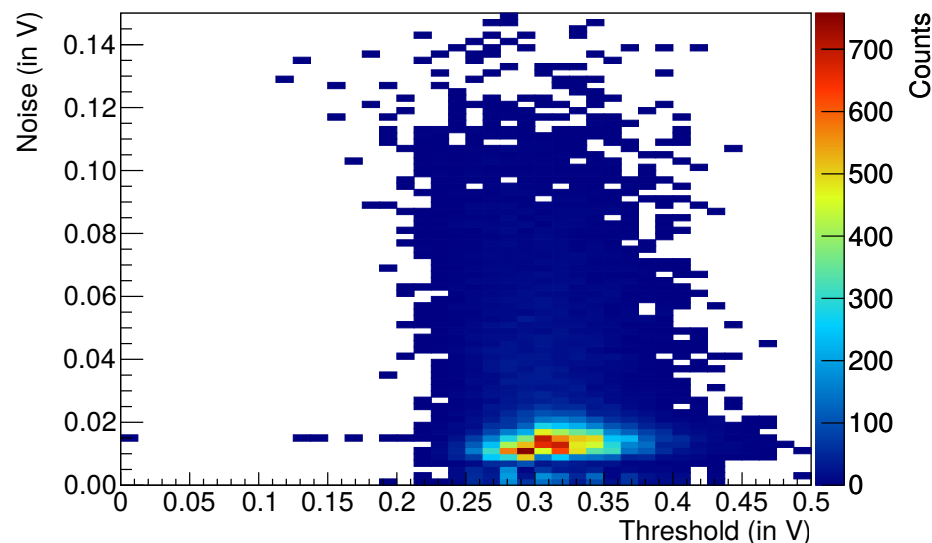
Threshold Distribution

- Using untriggered digital readout and charge injections, a threshold scan has been performed for the whole matrix
- ^{55}Fe decay signals equal a charge injection of about 300 mV
- Untuned matrix



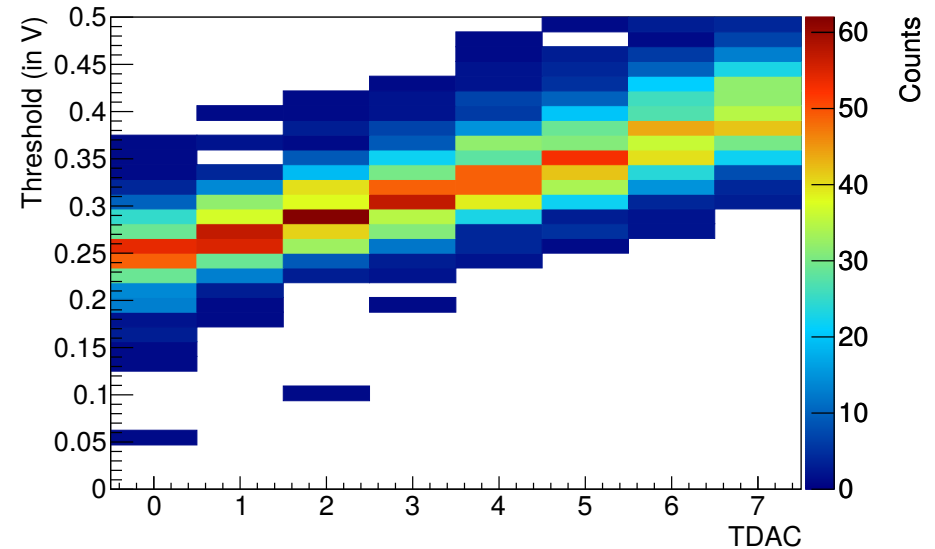
Threshold Distribution

- Large noise for some pixels due to measurement algorithm
- Threshold in same range as for good fits



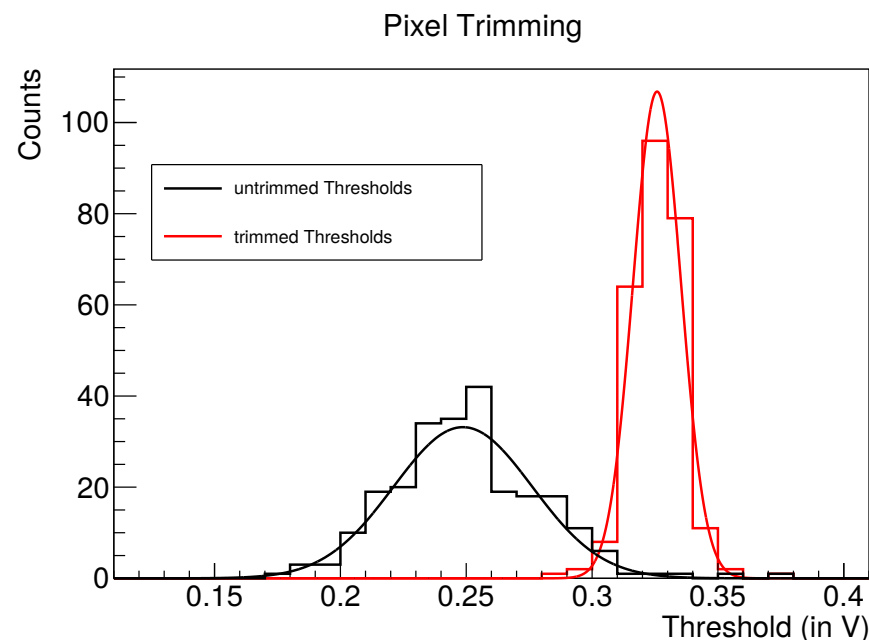
Matrix Tuning

- The matrix implements a 3 bit tuning DAC and a disable bit for each pixel
- Writing of the pixel memories is working and the detection threshold changes linearly with the setting



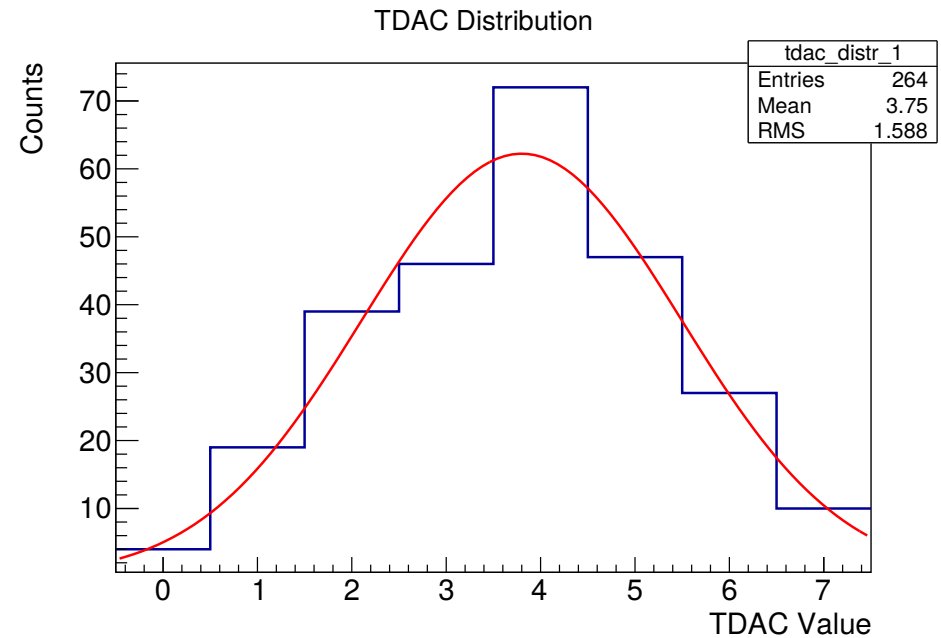
Matrix Tuning

- Threshold tuning implemented:
 - Detection thresholds are adjusted to $\mu + 3\sigma$ of untuned distribution
- Conducted for 2 rows (in total 264 pixels):
 - Distribution width $\sim 3x$ smaller
 - $\sigma_{\text{trimmed}} = 9.5\text{mV} \leftrightarrow \sim 50 e^-$



Matrix Tuning

- Threshold tuning implemented:
 - Detection thresholds are adjusted to $\mu+3\sigma$ of untuned distribution
- Conducted for 2 rows (264 pixels):
 - Distribution width 3x smaller
 - $\sigma = 9.5\text{mV} \leftrightarrow \sim 50 e^-$
 - TDAC setting distribution is gaussian like and using the whole range



Conclusions

- ATLASPix3 is being tested and is working up to the expectations
 - Serial configuration and SPI configuration are working
 - Regulators are working, measurements ongoing
 - Untriggered readout is working at 25 ns time stamping
 - Trimming of the matrix is possible

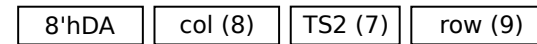
- Many more measurements to come:
 - Triggered readout
 - Command decoder
 - Clock recovery

BACKUP

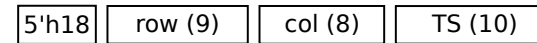
ATLASPix3 – Triggered Readout Data Structure

- Data transmission in 32 bit words:
 - beginning-of-data word
 - Hit word
 - End-of-event word
 - Spacing word
- Multiplexer structure to use full width of the Aurora code
- Spacer words used to make event word number even
- Configurable data contents

Hit Word (format 1):



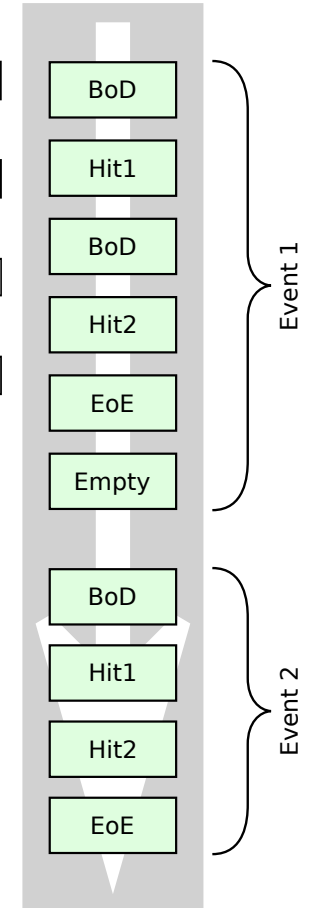
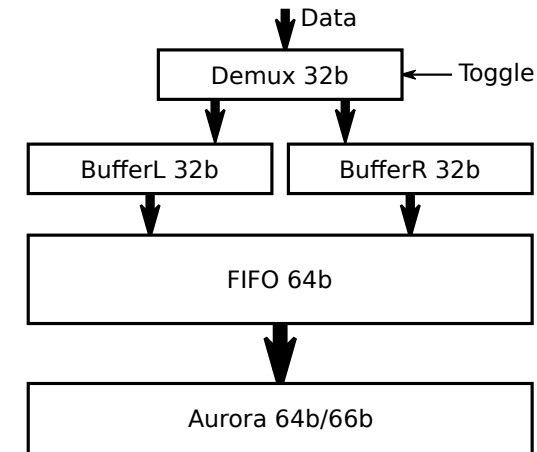
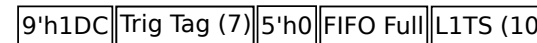
Hit Word (format 2):



Beginning-of-Data Word (BoD):

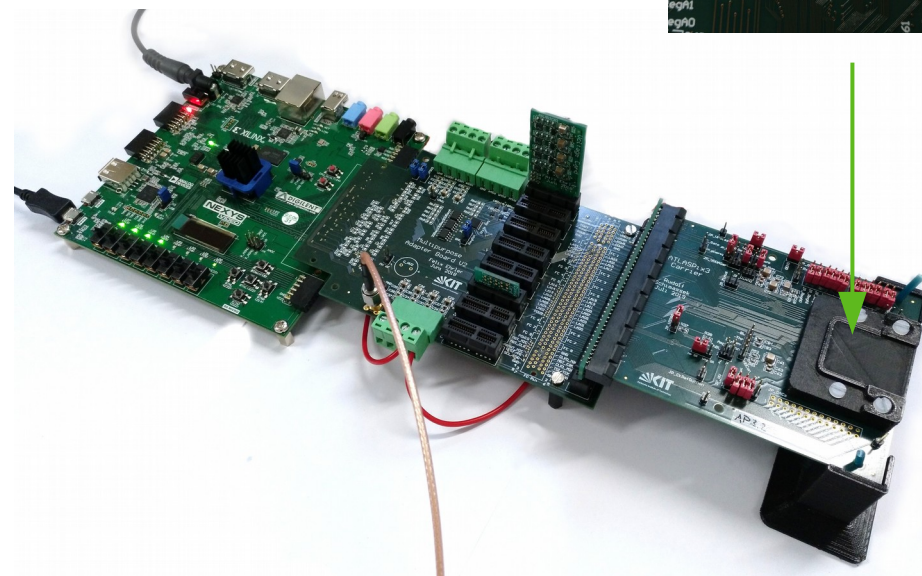
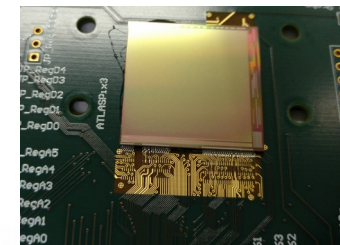


End-of-Event Word (EoE):



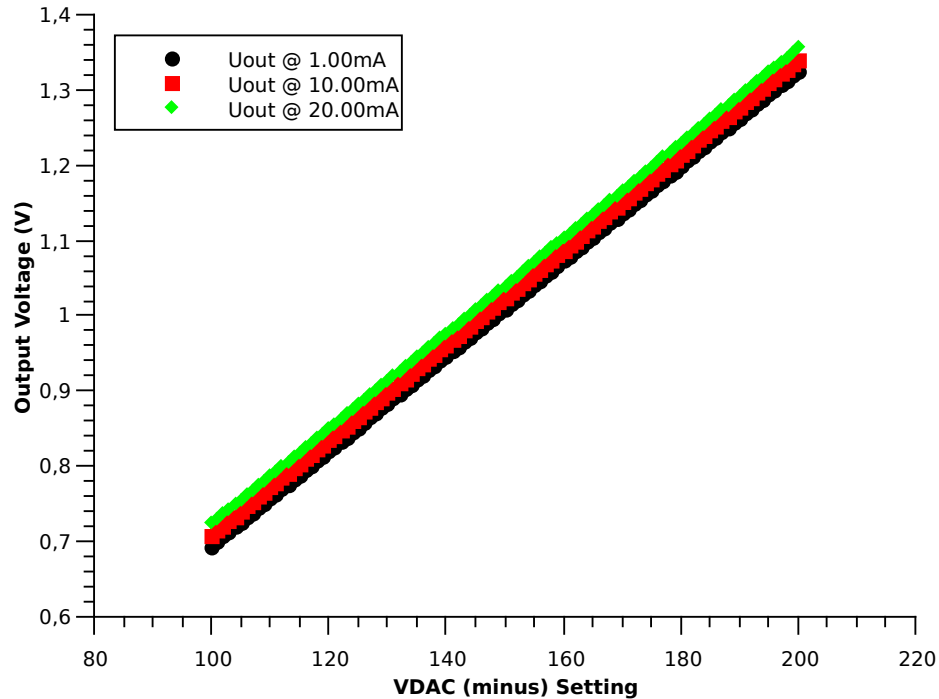
Measurement Setup

- Artrix-7 FPGA board
- GECCO adapter board
(GEneric sensor Configuration and COntrol System)
 - PCIe connector
 - Highly modular with function cards
 - No cable connections to carrier PCB
- ATLASPix3 carrier PCB
- Firmware
 - Chip configuration
 - Data decoding and reduction
- Software (Qt based)

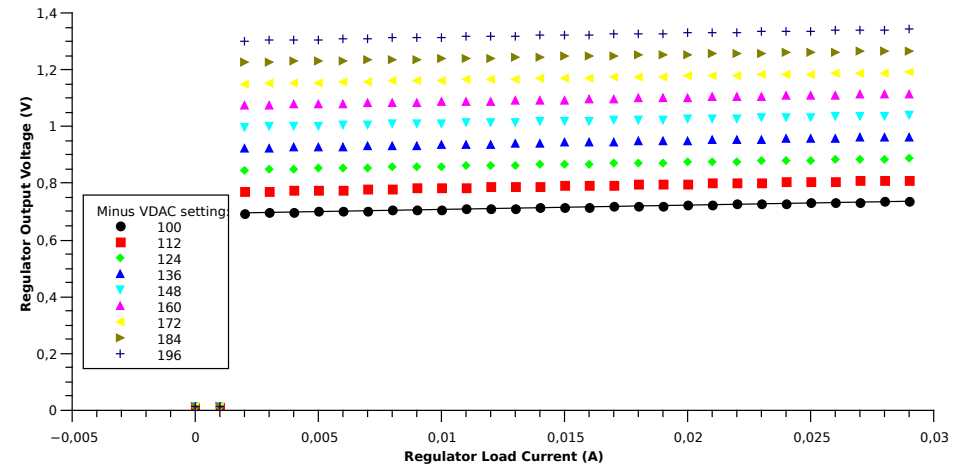


Power Regulators – MinusReg

MinusReg Linearity



Regulator Characteristics for Minus



TDAC Effect

- Single pixels show linear threshold changes
 - No fluctuations cancelling out in the histogram for 264 pixels
- Slope of the connection changeable via a global DAC

