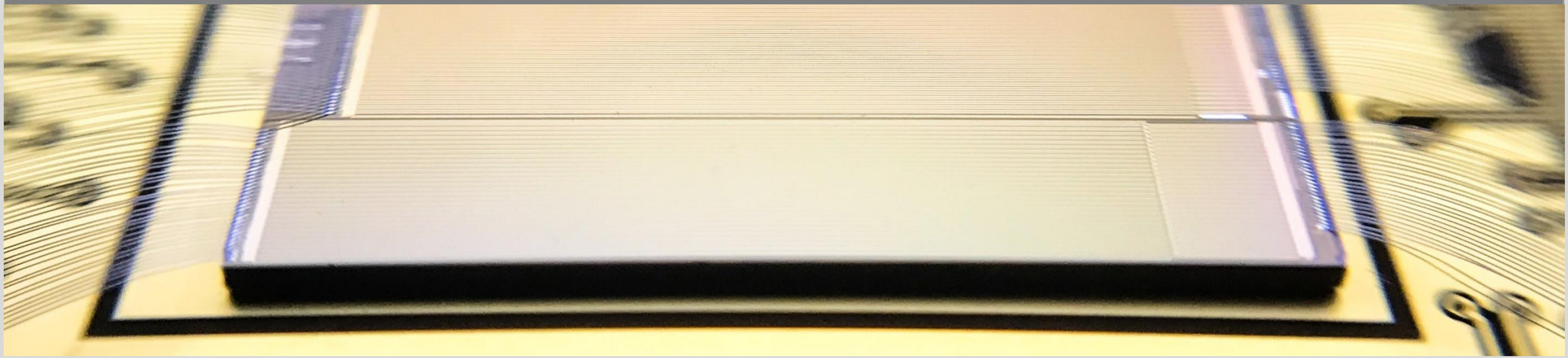
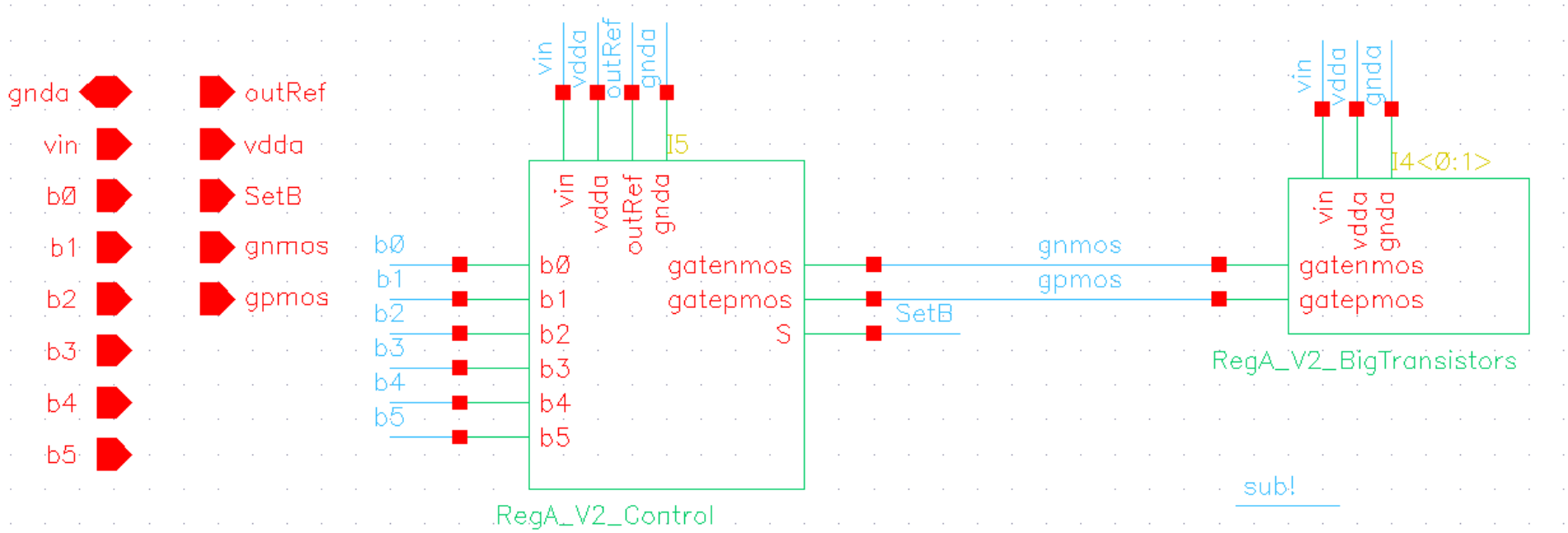
Power Regulator on ATLASPix3

Alena Weber

ASIC and Detector Laboratory, Karlsruhe Institute of Technology and University Heidelberg



Schematics of the power regulator



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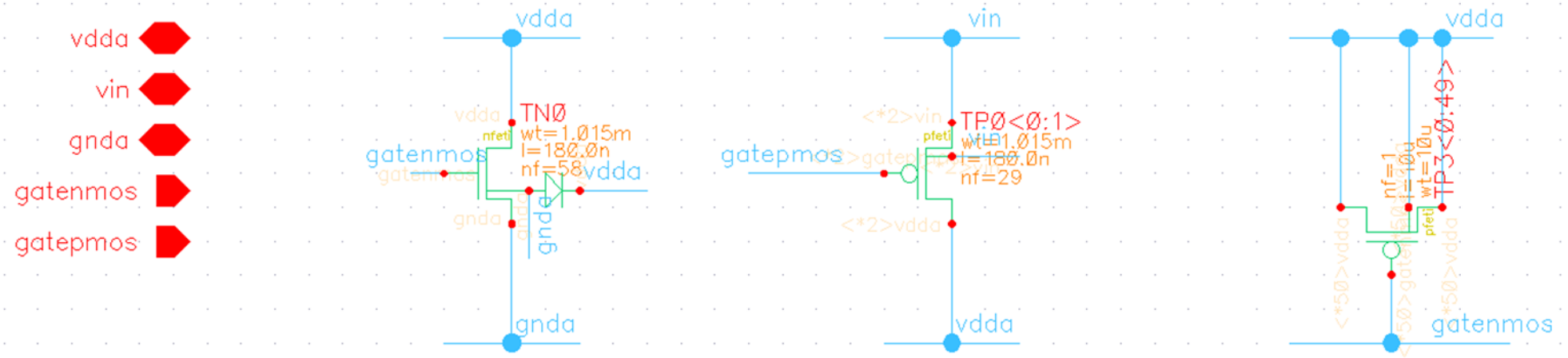
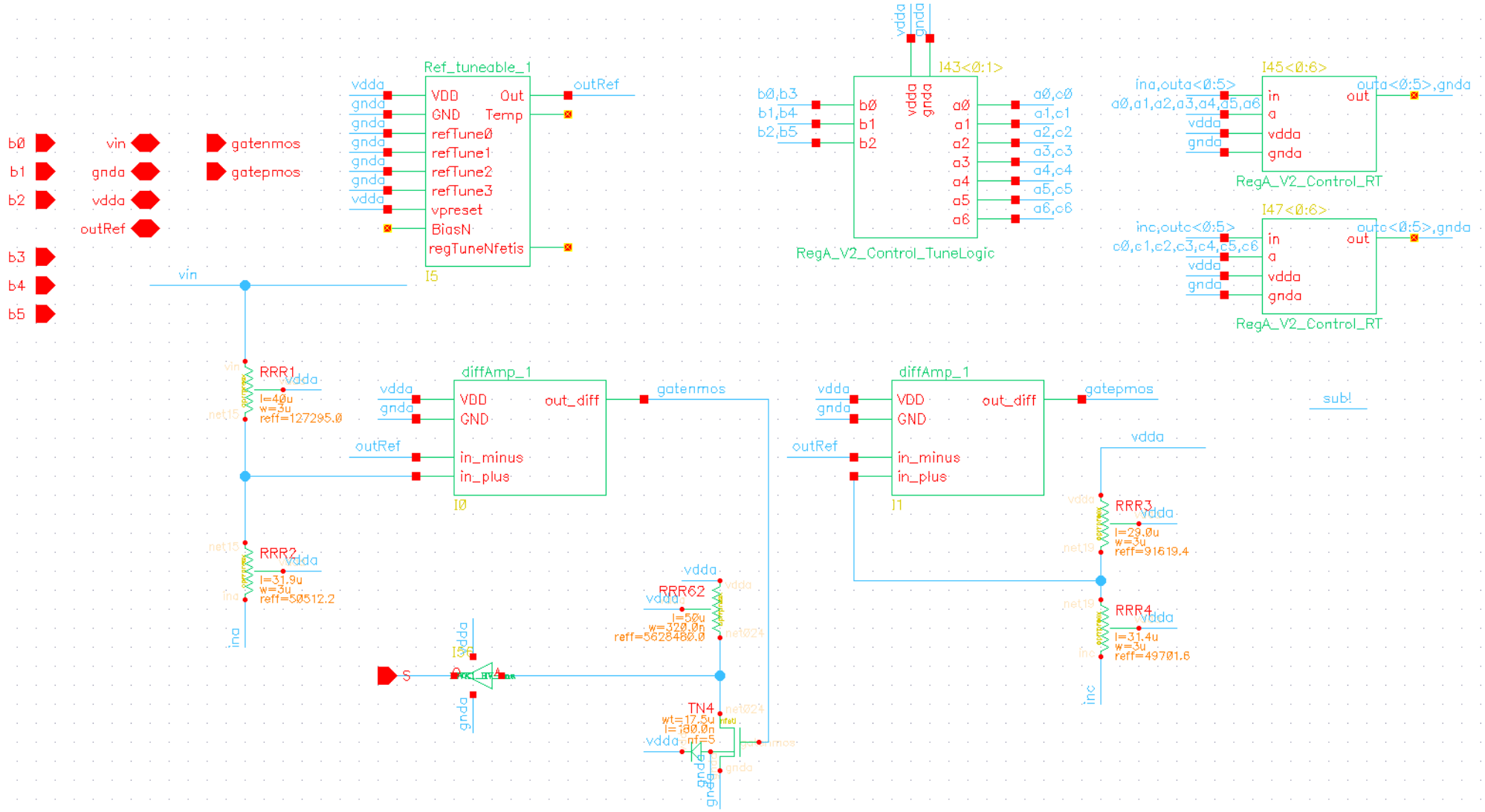


Schematics of the power regulator



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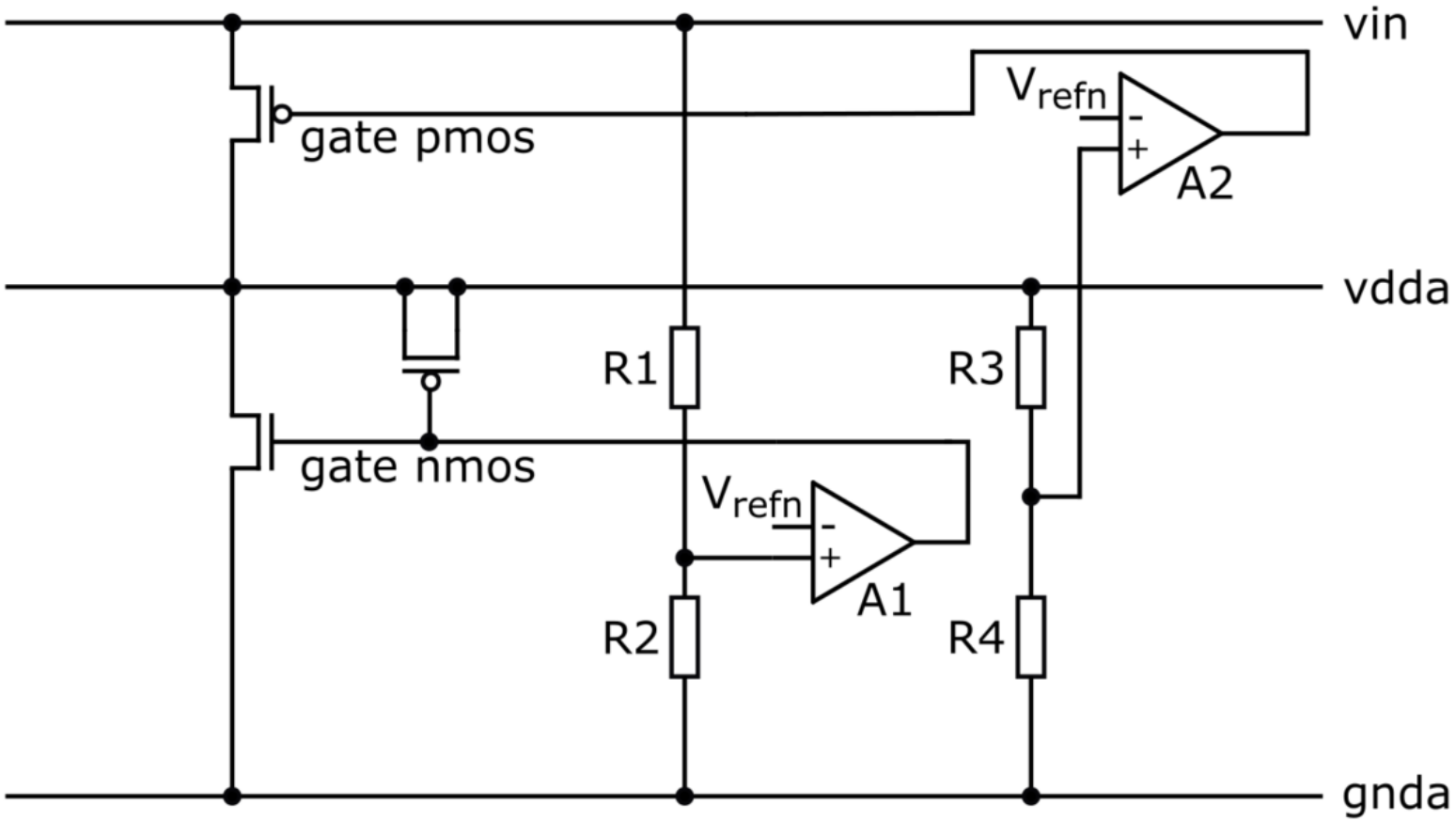

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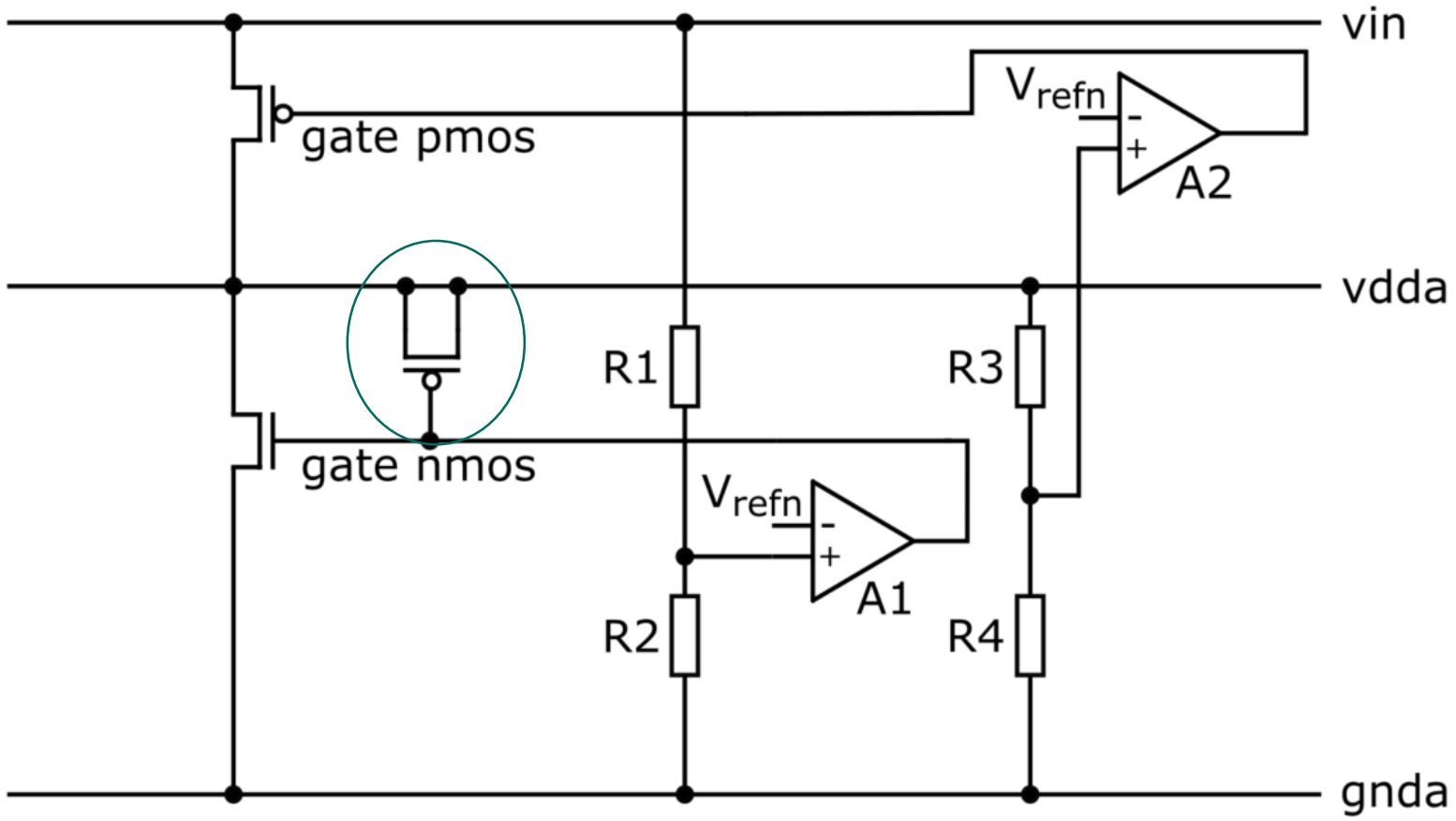
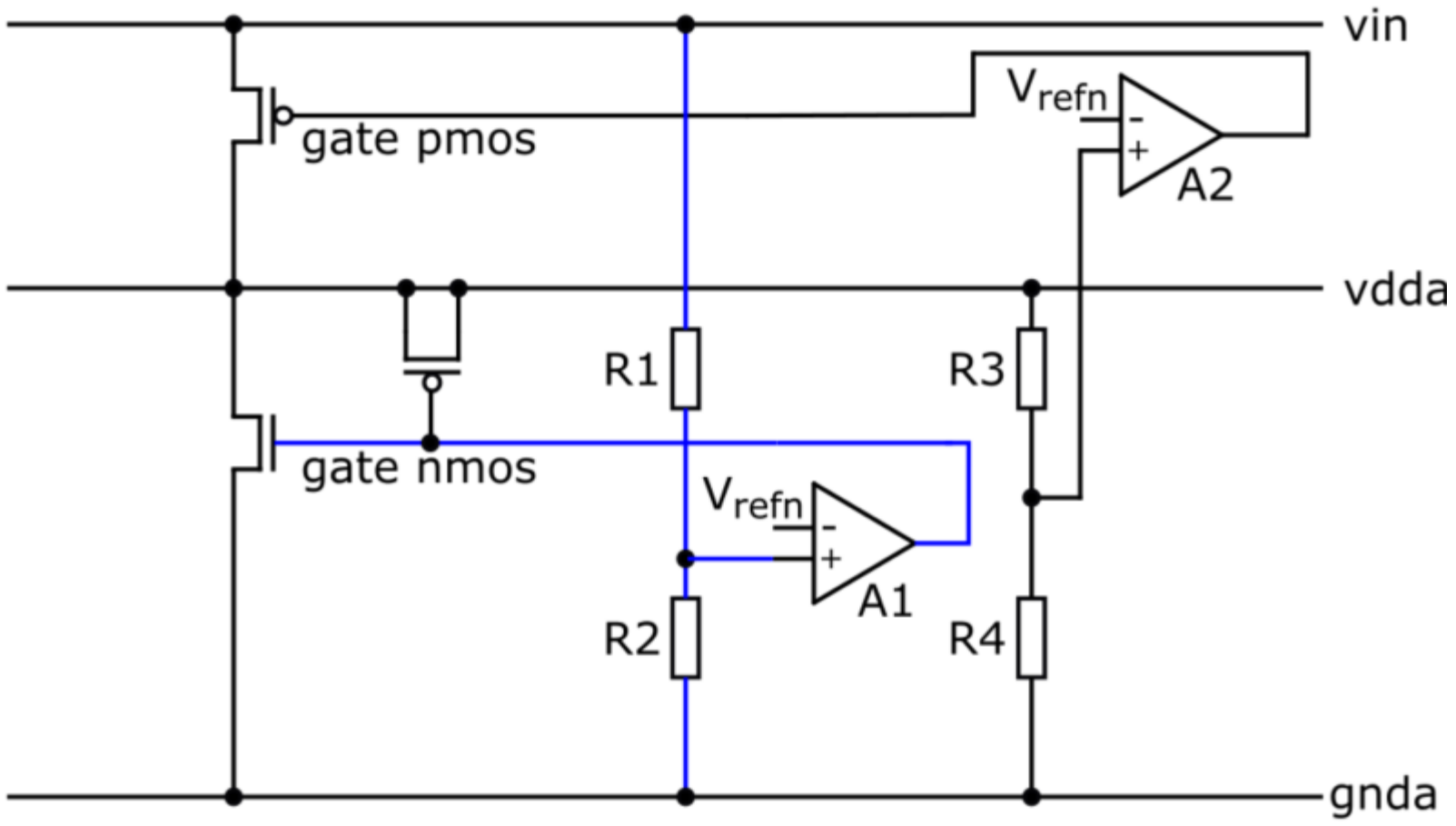


Stabilisation
Gate Kapazität = 7.75 fF/um2

hier 100 Transistoren mit w = 10 um und l = 10 um

→ C =

Schematics of the power regulator



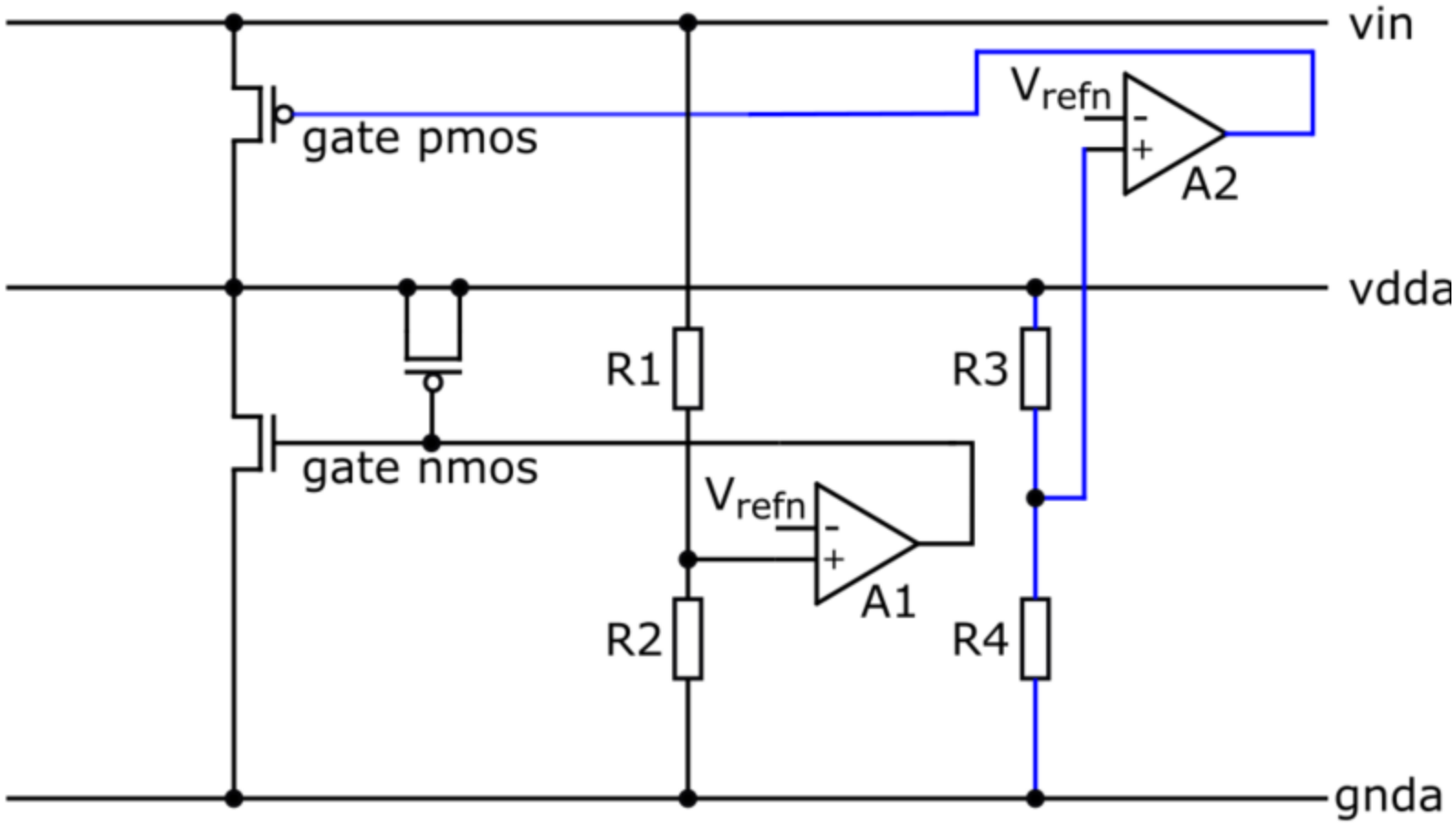
1. Regulation Loop

Out von A1 ändert sich mit vdda.

Bei Bedarf wird das „zu viel“ an Strom über Tn geleitet.

Ist vin zu hoch, leitet Tn mehr, ist vin „nah“ an vdda sperrt Tn.

Schematics of the power regulator



2. Regulation Loop

Out von A2 ändert sich mit vdda und steuert Tp an.

Wenn vdda zu hoch wird, schließt A2 Tp, vdda sinkt bis zum gewünschten Wert und Tp leitet wieder.

Test schematics similar to the one Michael Karagounis has shown

Fachhochschule Dortmund
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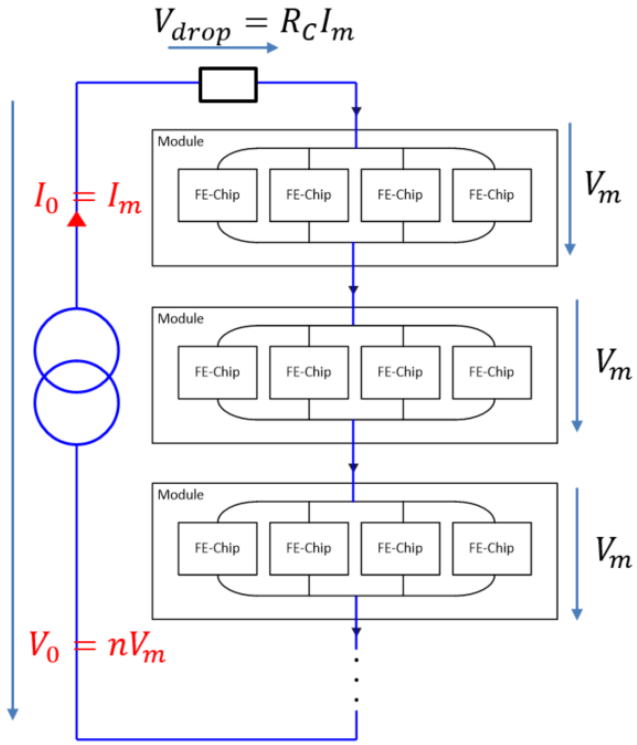
Parallel vs Serial Powering Scheme II



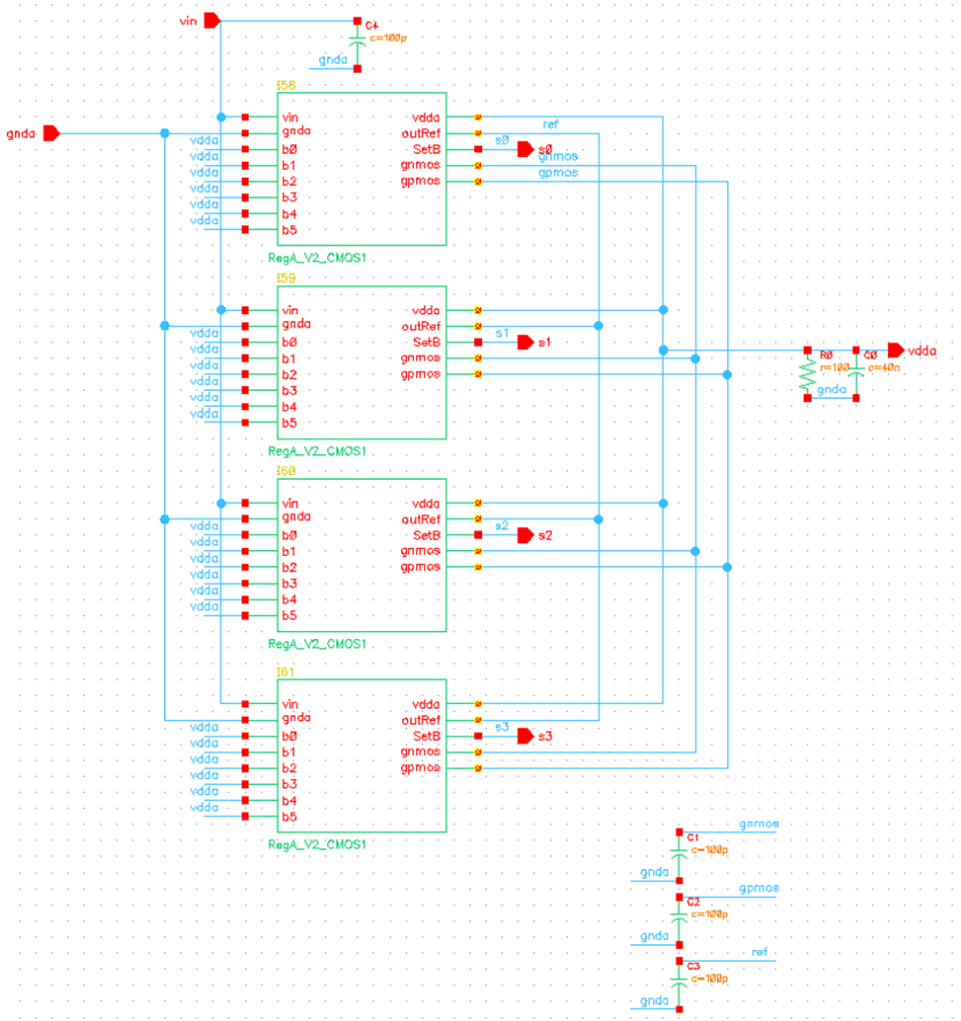
- Modules are connected in series
- Powered by constant current source
- Total supply current is defined by maximum load current of a single module
- Total supply voltage across the chain scales with the number of powered modules

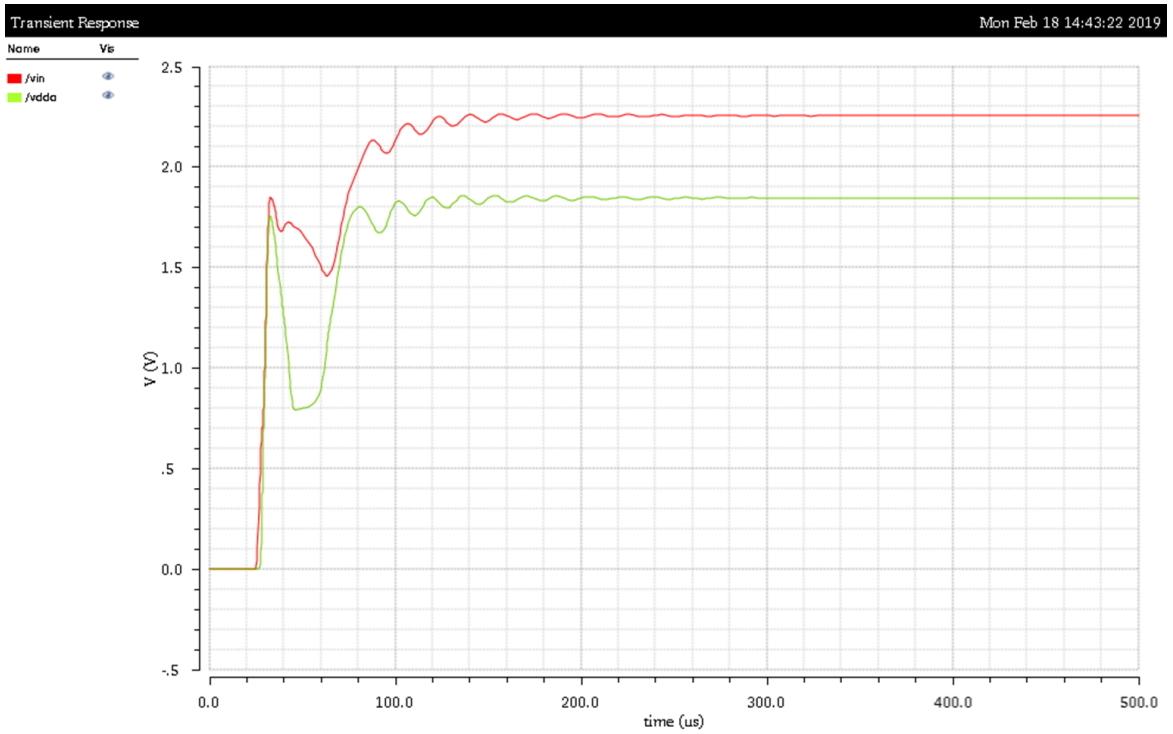
$$\eta = \frac{1}{1 + \frac{R_C I_m}{n V_m}}$$

- Regulator circuitry required to generate constant supply voltage out of constant current

21.02.2019 Shunt-LDO regulator in C65nm | RD53 General Meeting at RAL | michael.karagounis@hshl.de Folie 24

Test schematics for simulations





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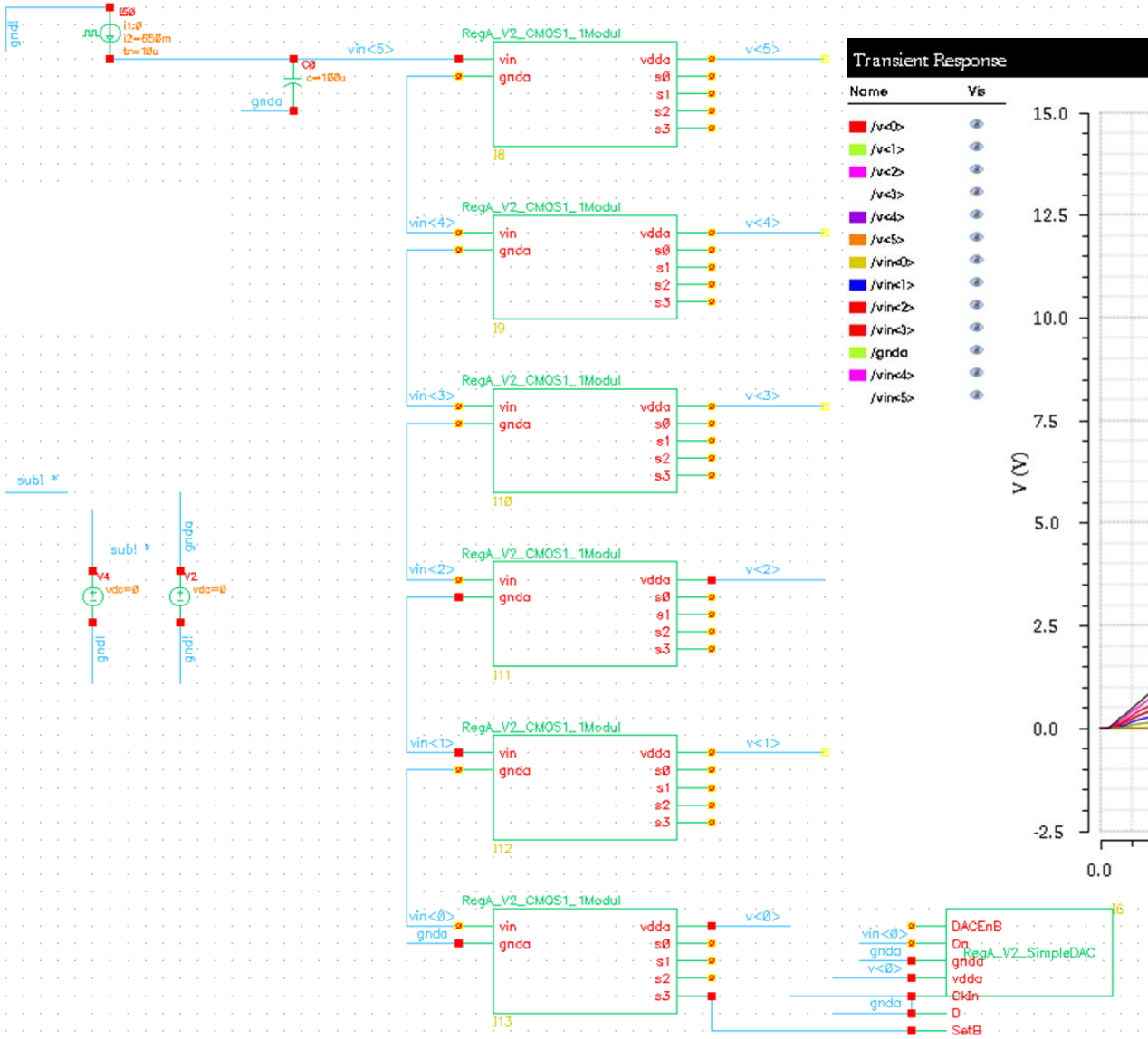
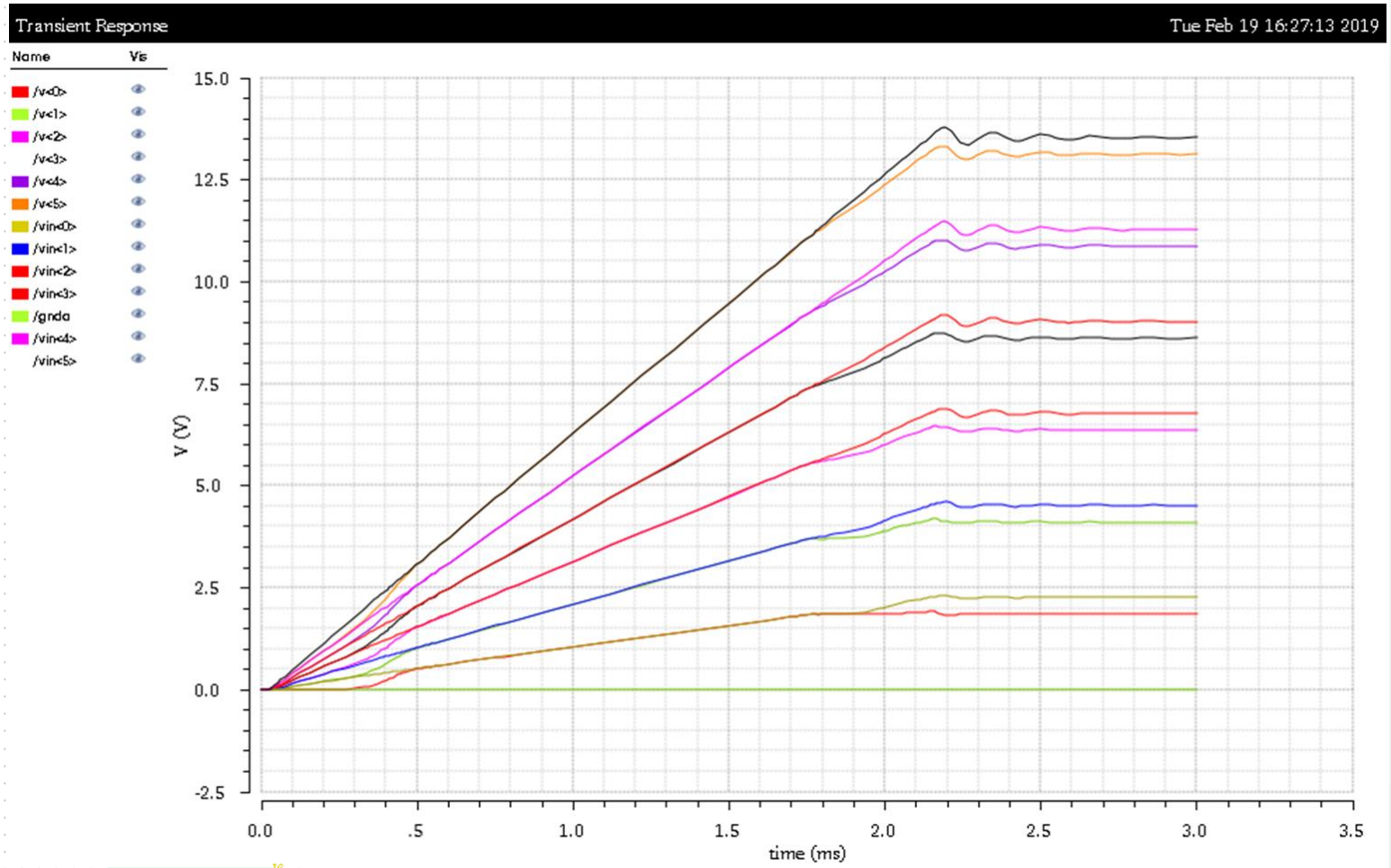
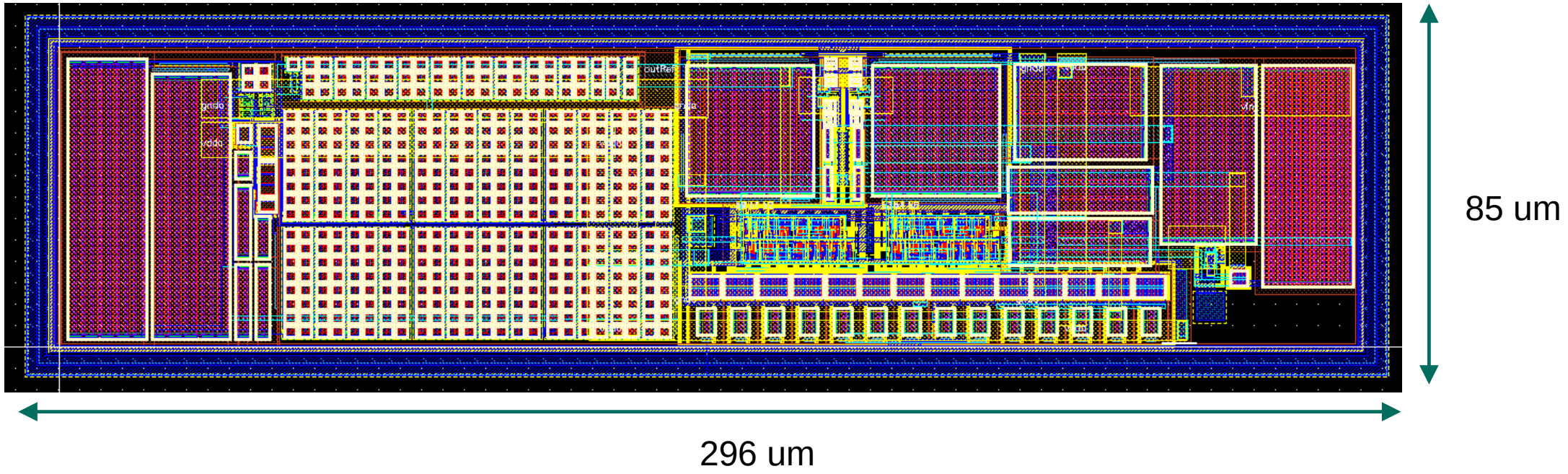




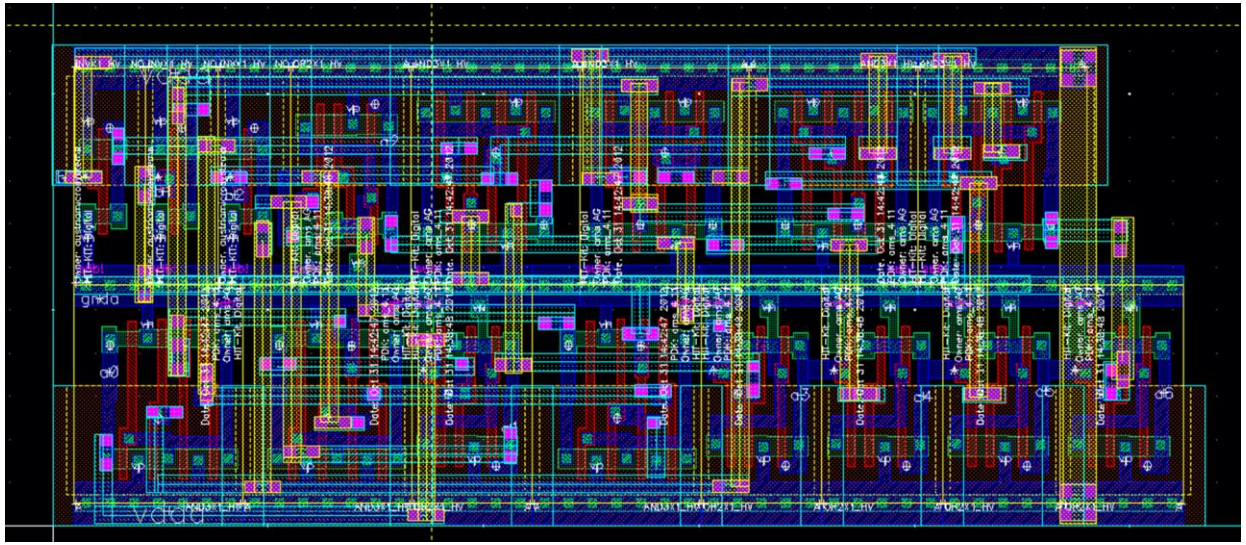
Layout Dimensions

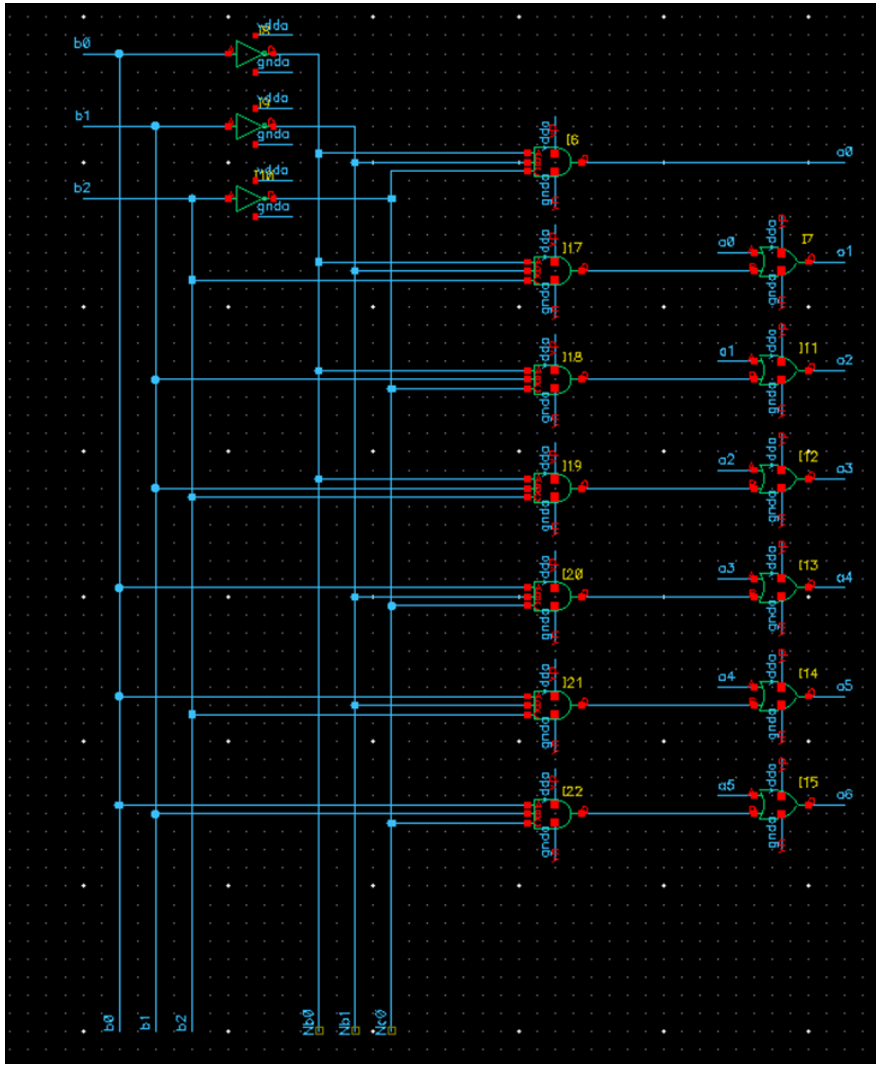
- Layout of the control block



Layout Dimensions

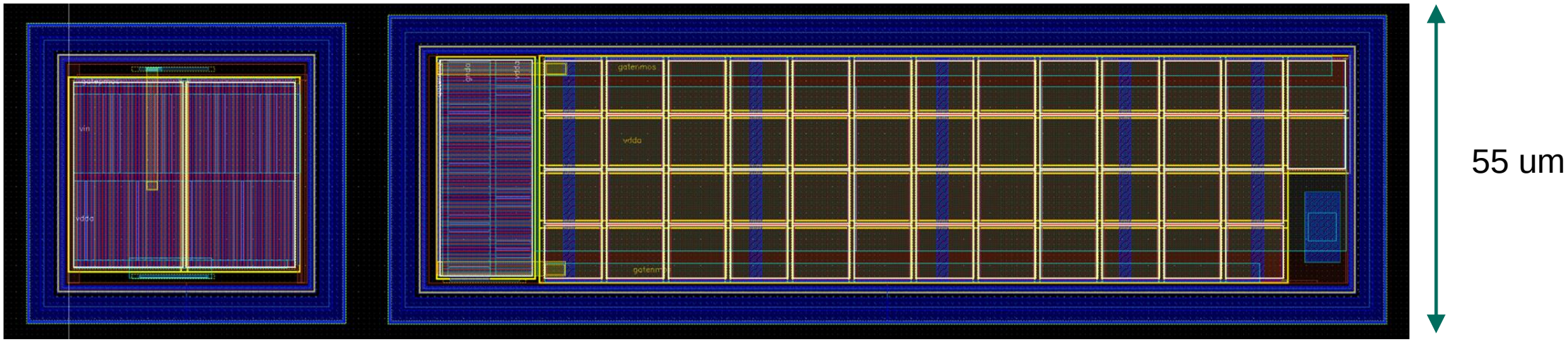
- Tune Logic: 3 input bits to control 7 tune steps with identical resistors





Layout Dimensions

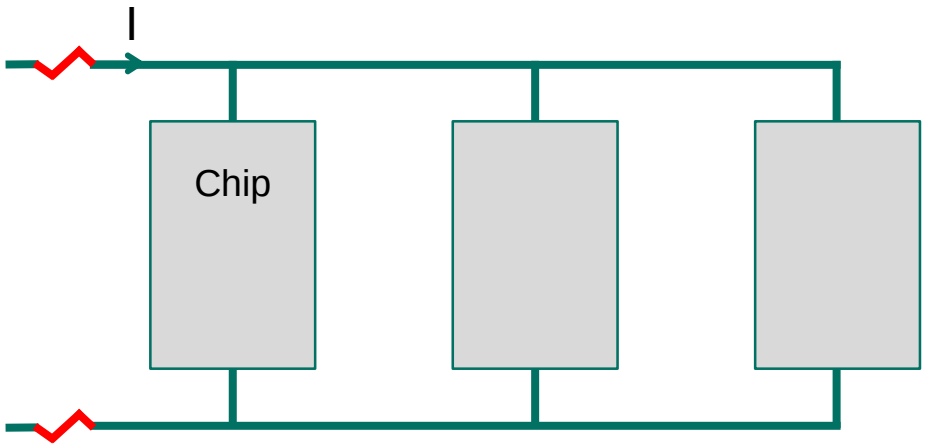
- Big Transistors and stabilisation capacitor



BACKUP

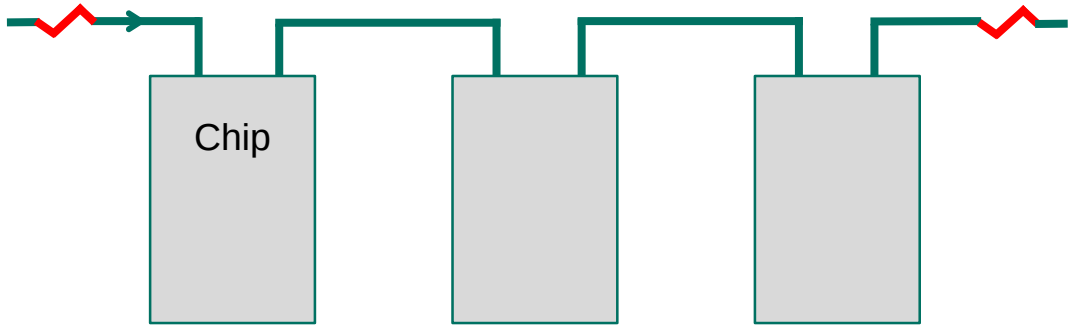
Serial Powering

- Parallel Powering



- chip connection parallel, all outputs on same voltage level

- Serial Powering



- chip connection serial, all outputs on a different voltage level

Serial Powering

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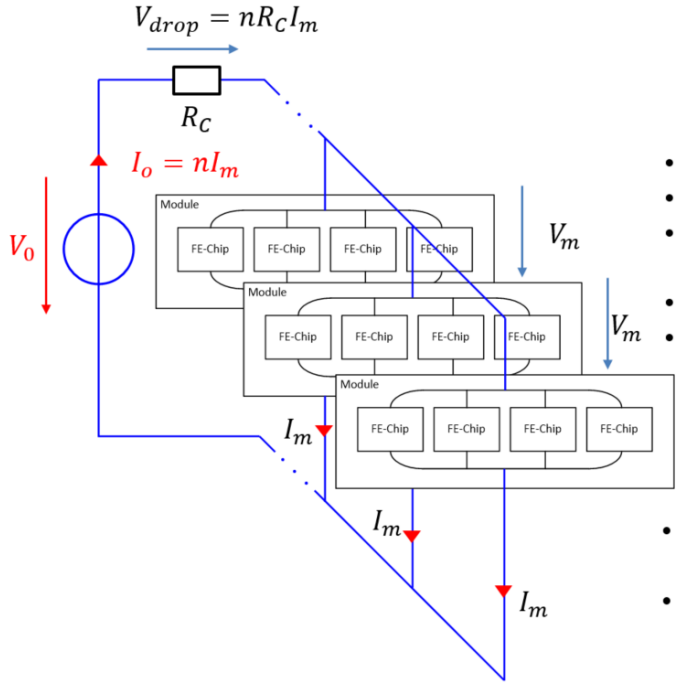

- Modules are connected in parallel
- Powered by constant voltage source
- Total supply current scales with the number of modules
- Large supply currents affect efficiency
- IR drops on power cables

$$\eta = \frac{1}{1 + n\frac{I_m R_C}{V_m}}$$

- DC/DC conversion decreases supply current and increases efficiency
- DC/DC conv. has high material budget

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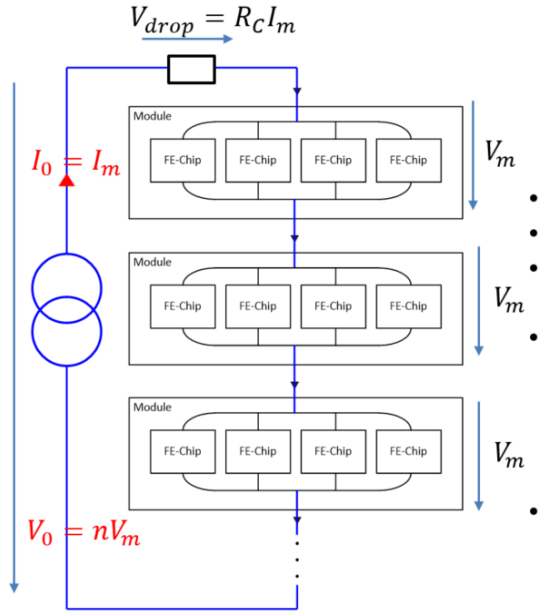
Parallel vs Serial Powering Scheme II



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Overview of simulated circuits

Description of the circuit	Modification A	Modification B
FE-I 3 ATLAS hybrid pixel readout chip	Connection of transistor M1 changed	
LDO regulator with shunt (1)		
Regulator implemented on MuPix9		
Extended LDO regulator with shunt (2)	Modified circuit before A4, without A2	Like Modification A but with A2
Bandgap for reference voltage implemented on MuPix9		
Differential Amplifier implemented on MuPix9	Modified dimensions	

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will be implemented on ATLASPix3

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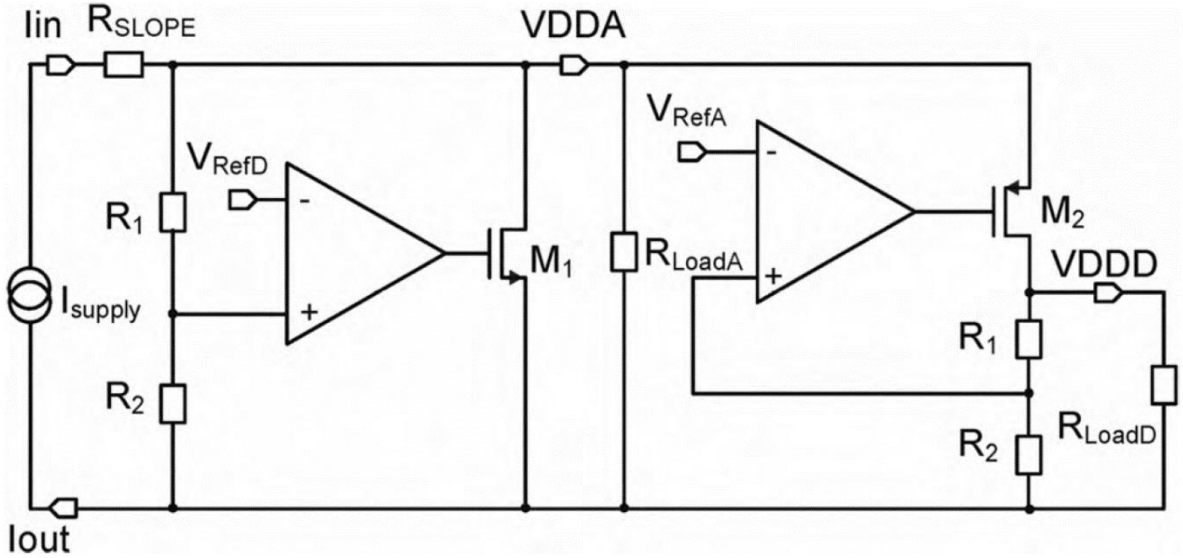
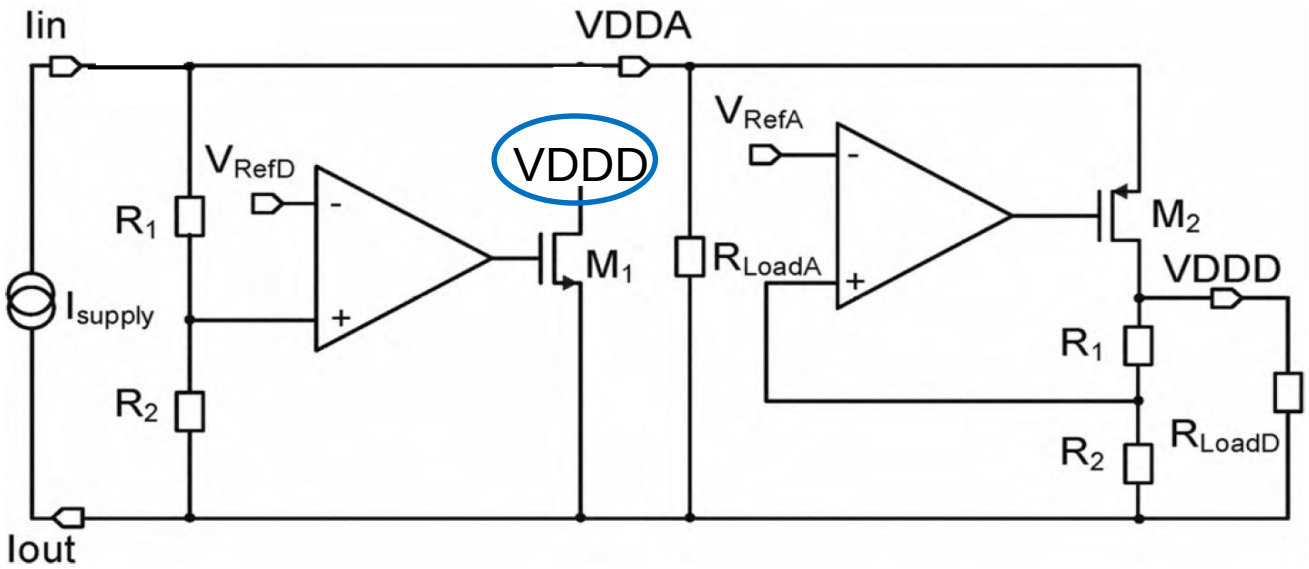
FE-I 3 ATLAS hybrid pixel readout chip



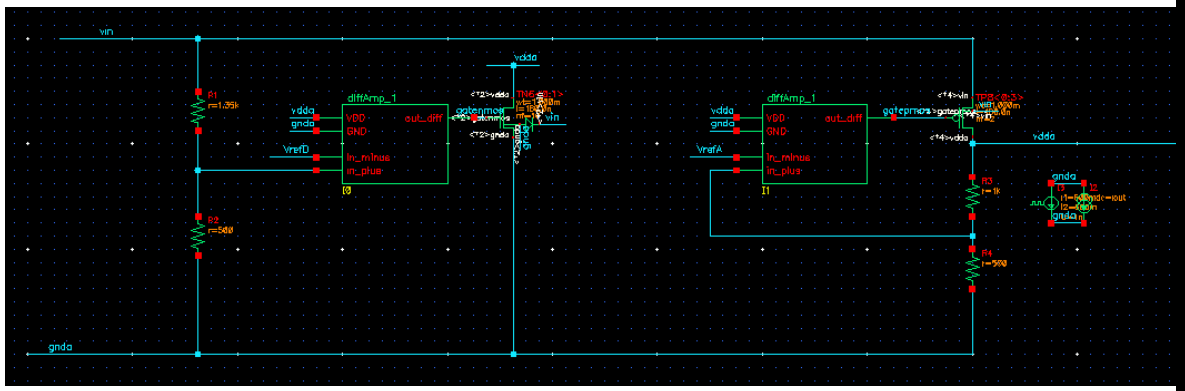
Power Regulator for ATLAS Pix3

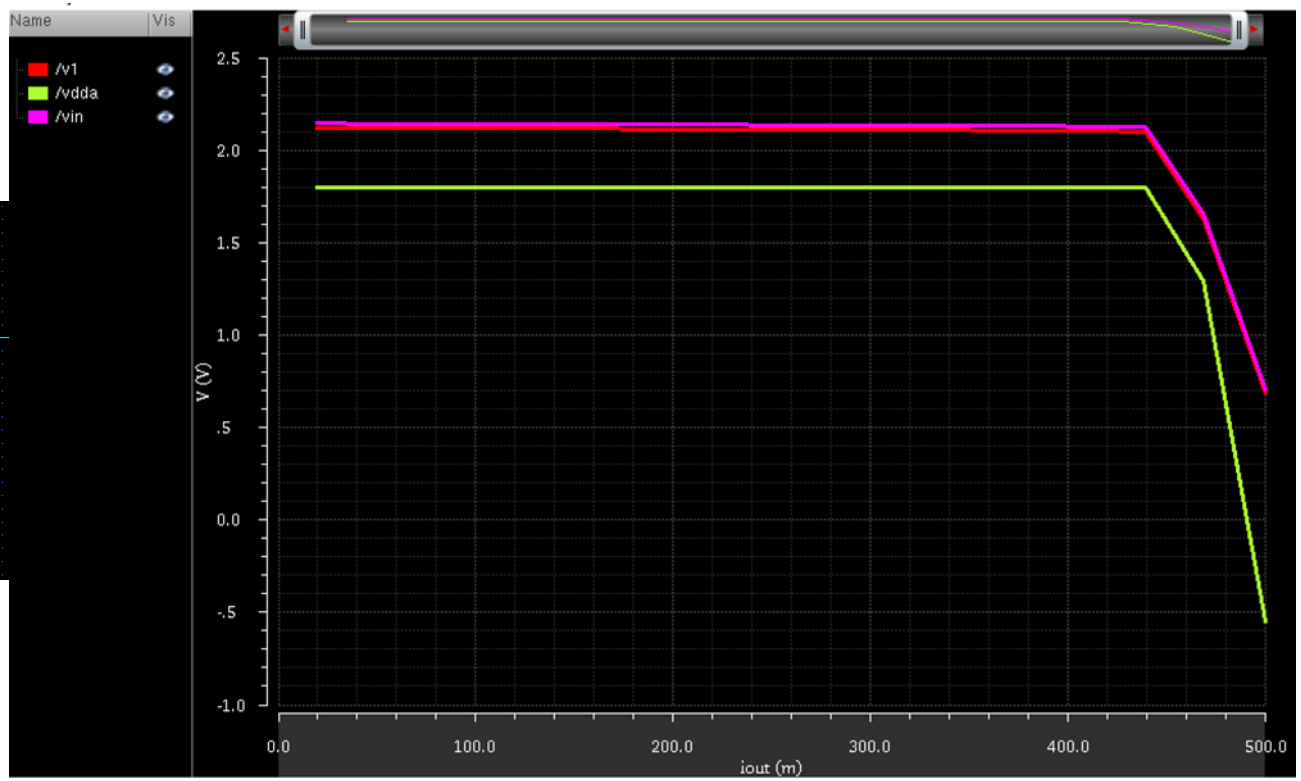


- VDDA = ~ 2.2 V
- VDDD = 1.8 V
- to protect M1 from to high voltages connected to VDDD

DC Analyse

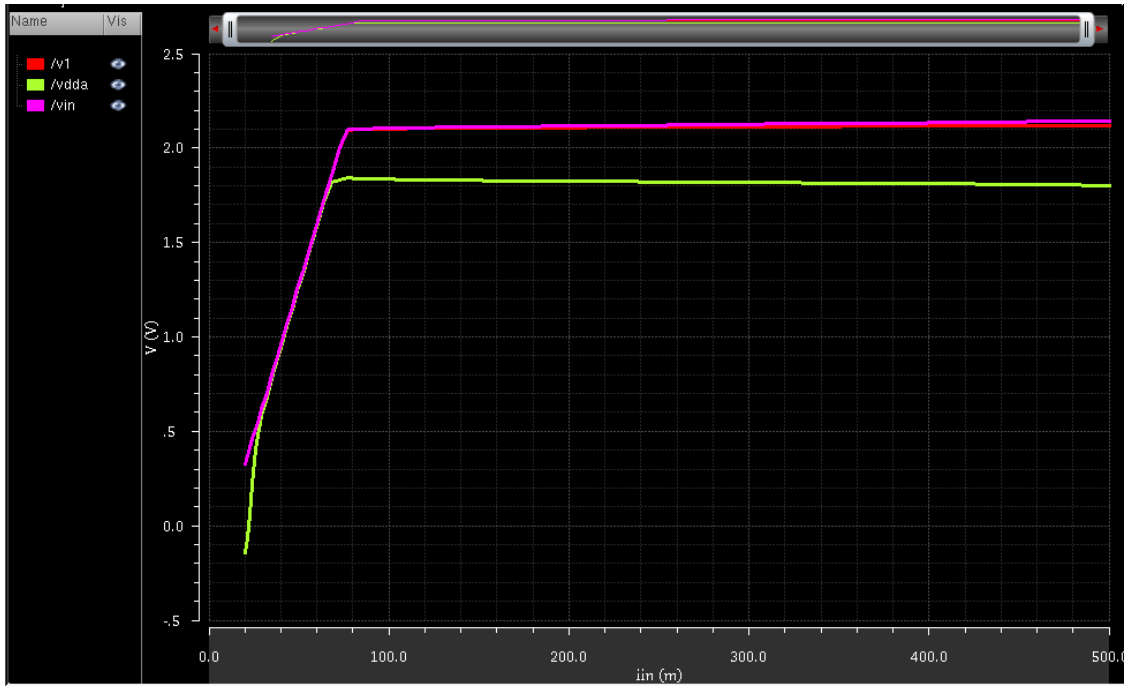
- Iin = 520 mA und Iout sweep 0…500mA





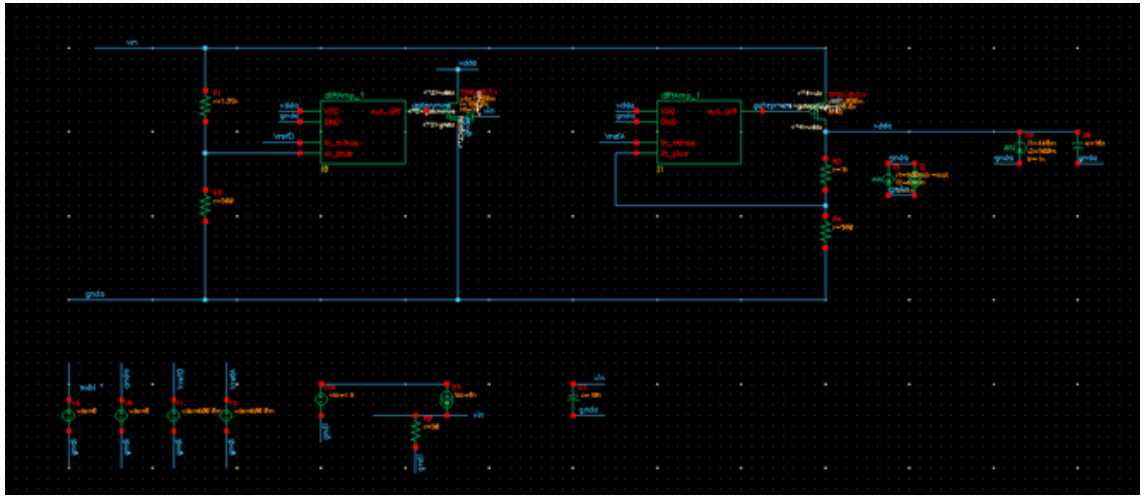
DC Analyse

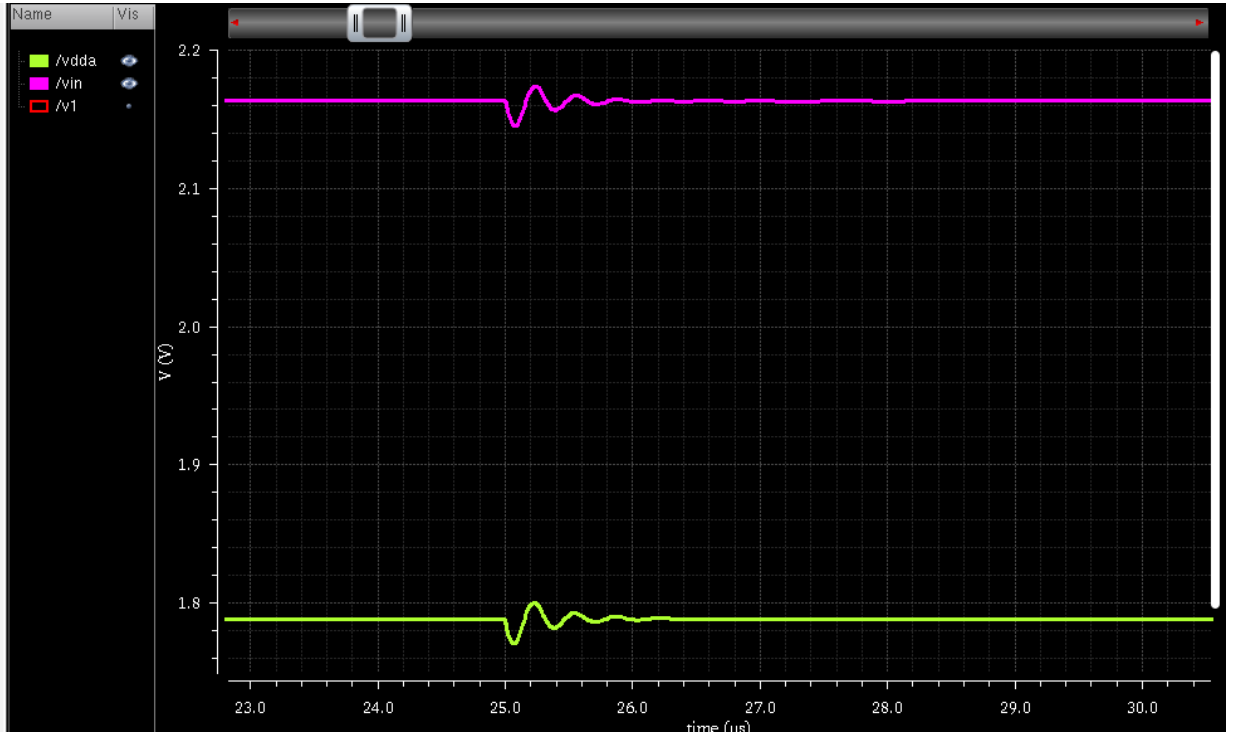
- Iin sweep 20…500mA und Iout = 10mA



Transient Analyse

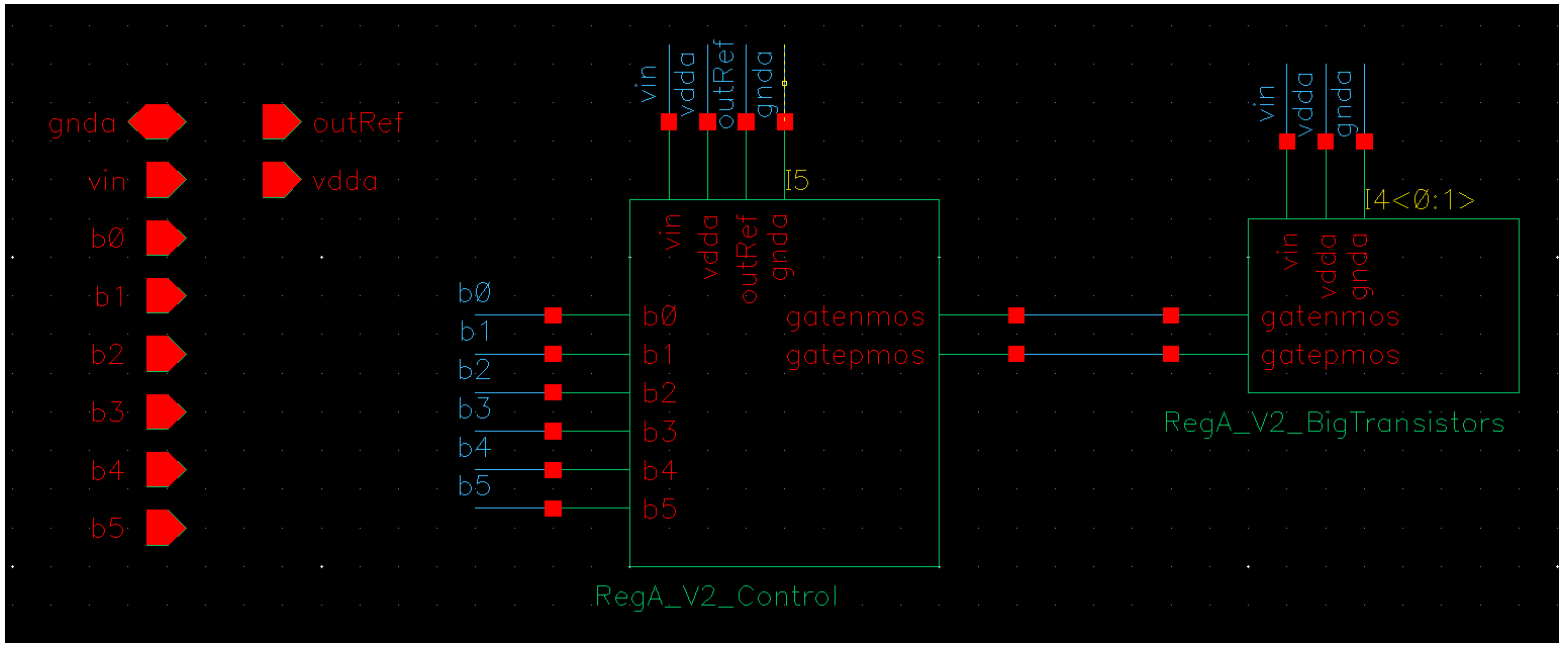
- Iin = 600 mA and Iout = Ipulse 490 mA -> 500





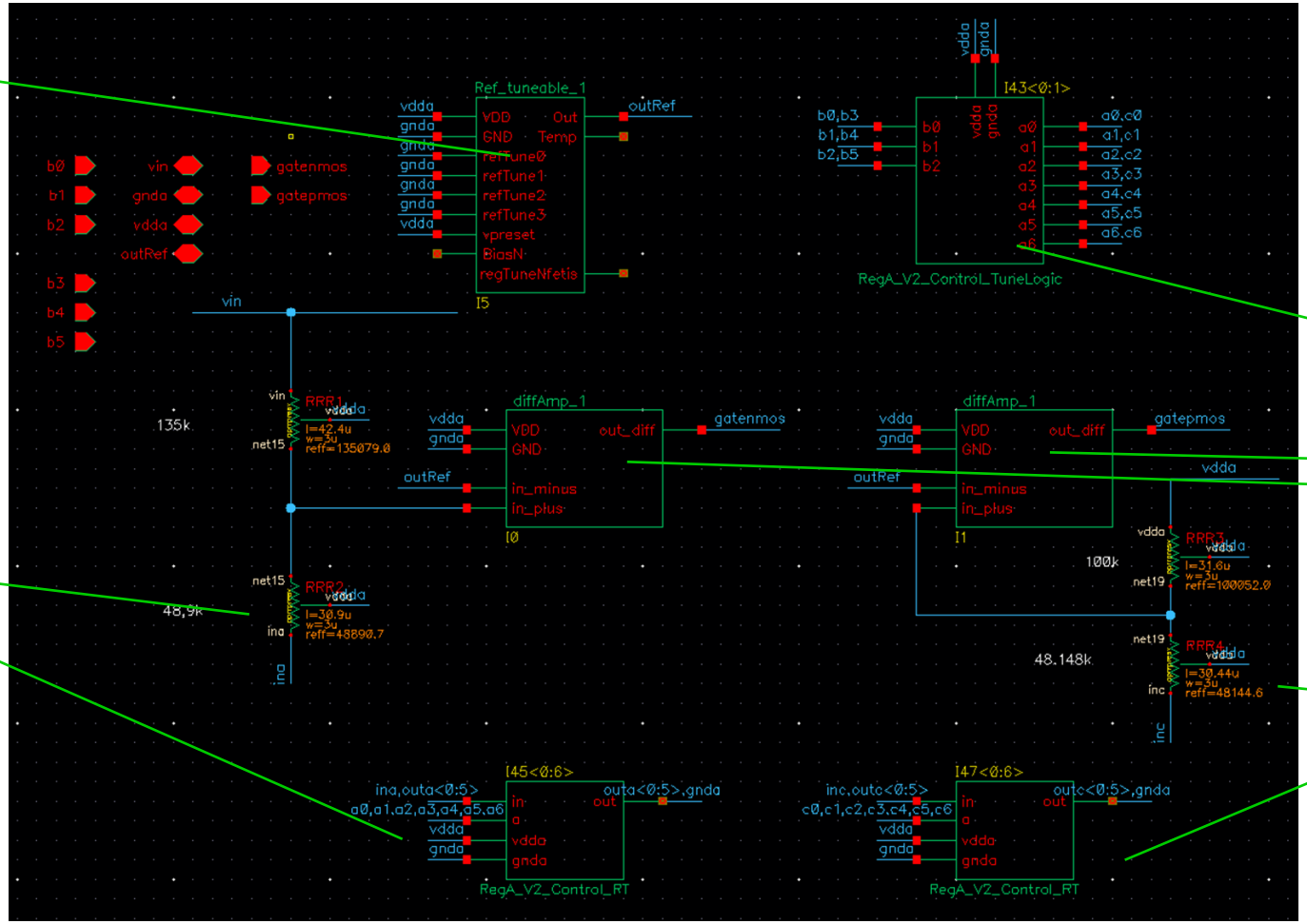
Power Regulator for ATLAS Pix3

- Top schematic
- The circuit is split in 3 parts:
  - Control block
  - two times the same block with the big power transistors



Power Regulator for ATLAS Pix3

- Schematic of the control block



reference voltage

tune logic

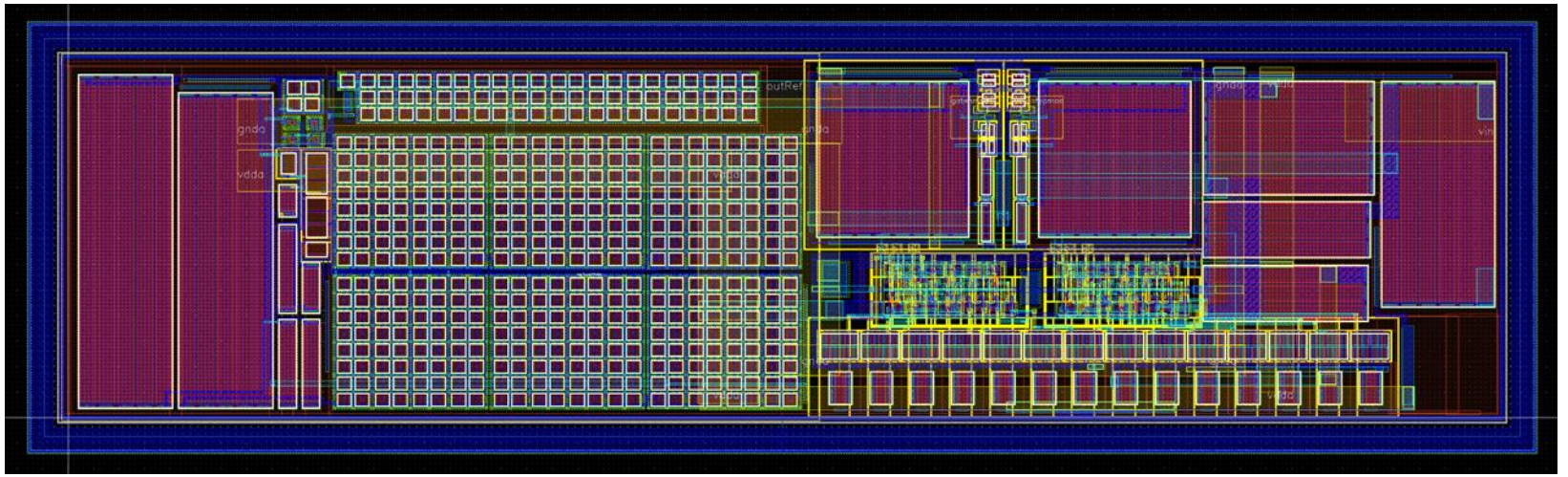
2 differential amplifiers

3 tune bits for R

3 tune bits for R

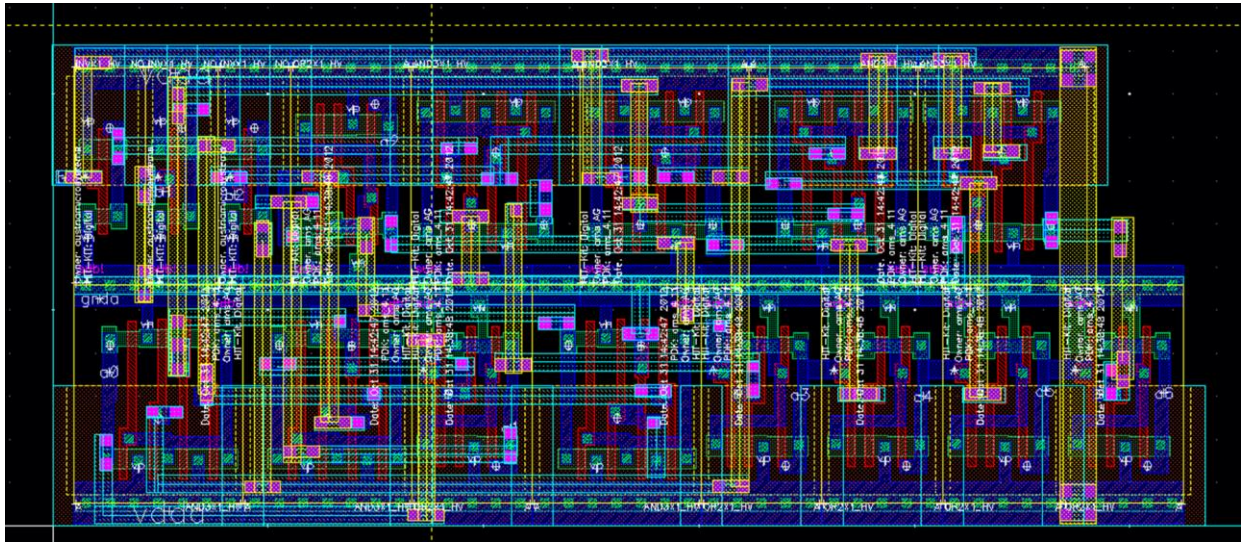
Power Regulator for ATLAS Pix3

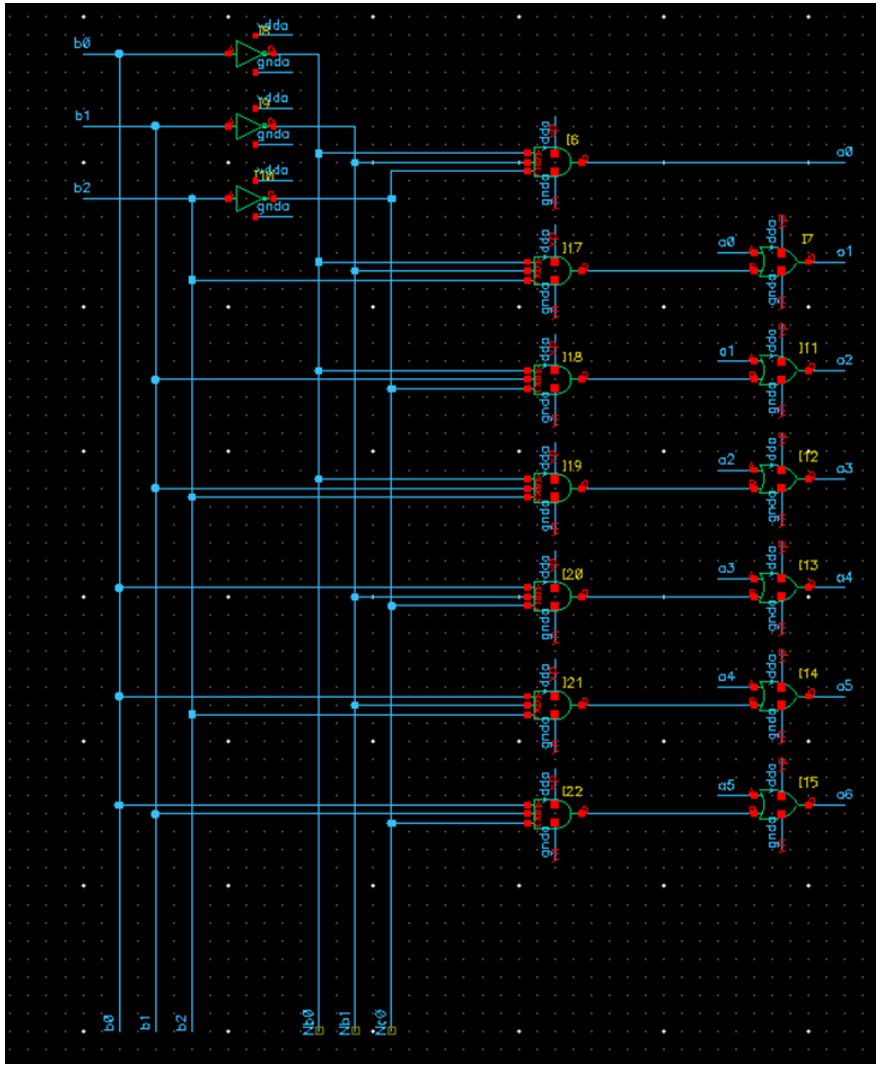
- Layout of the control block



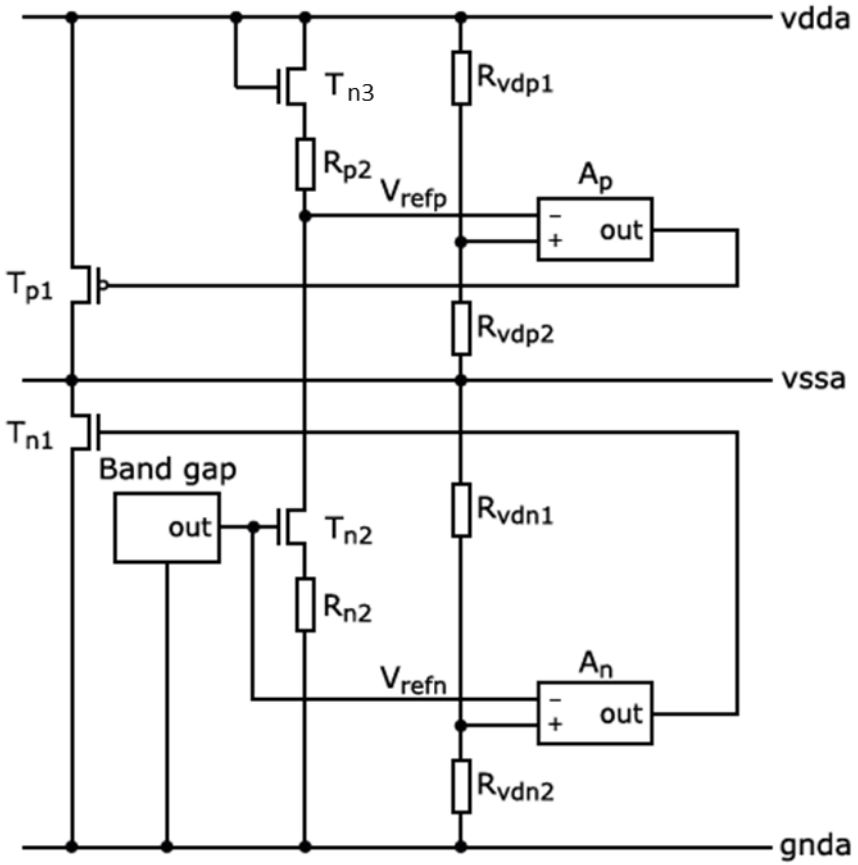
Power Regulator for ATLAS Pix3

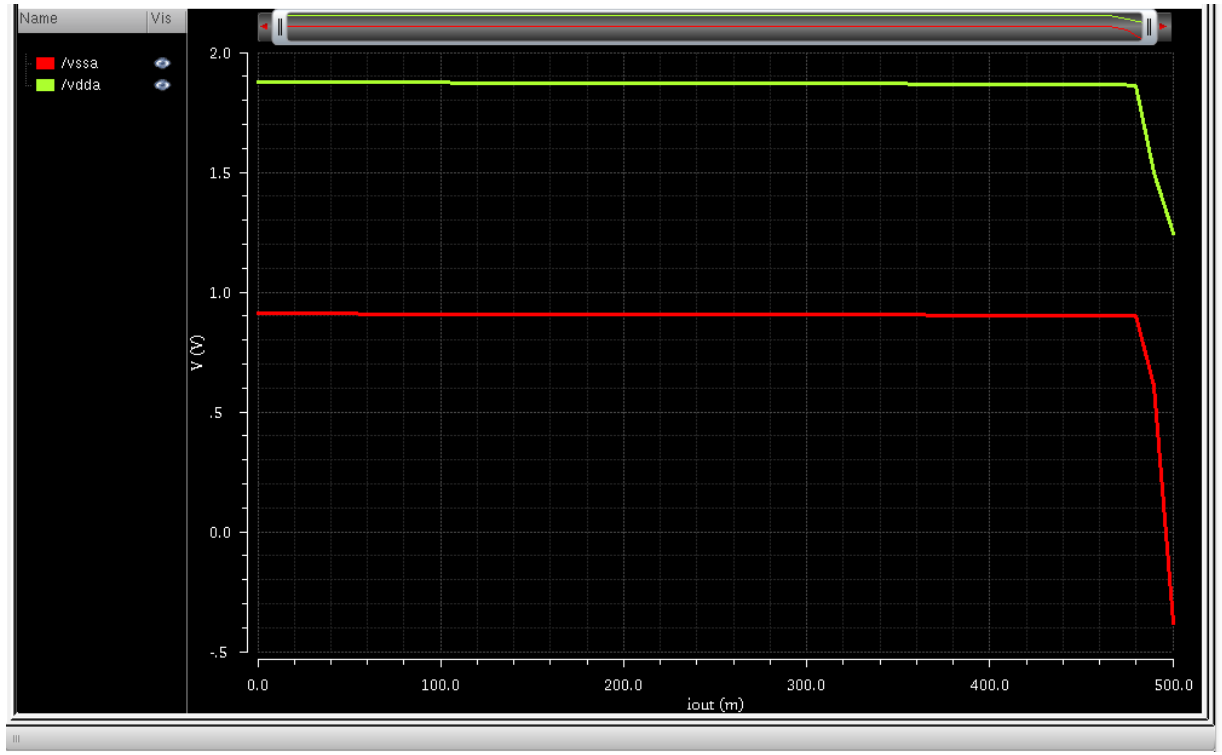
- Tune Logic: 3 input bits to control 7 tune steps with identical resistors



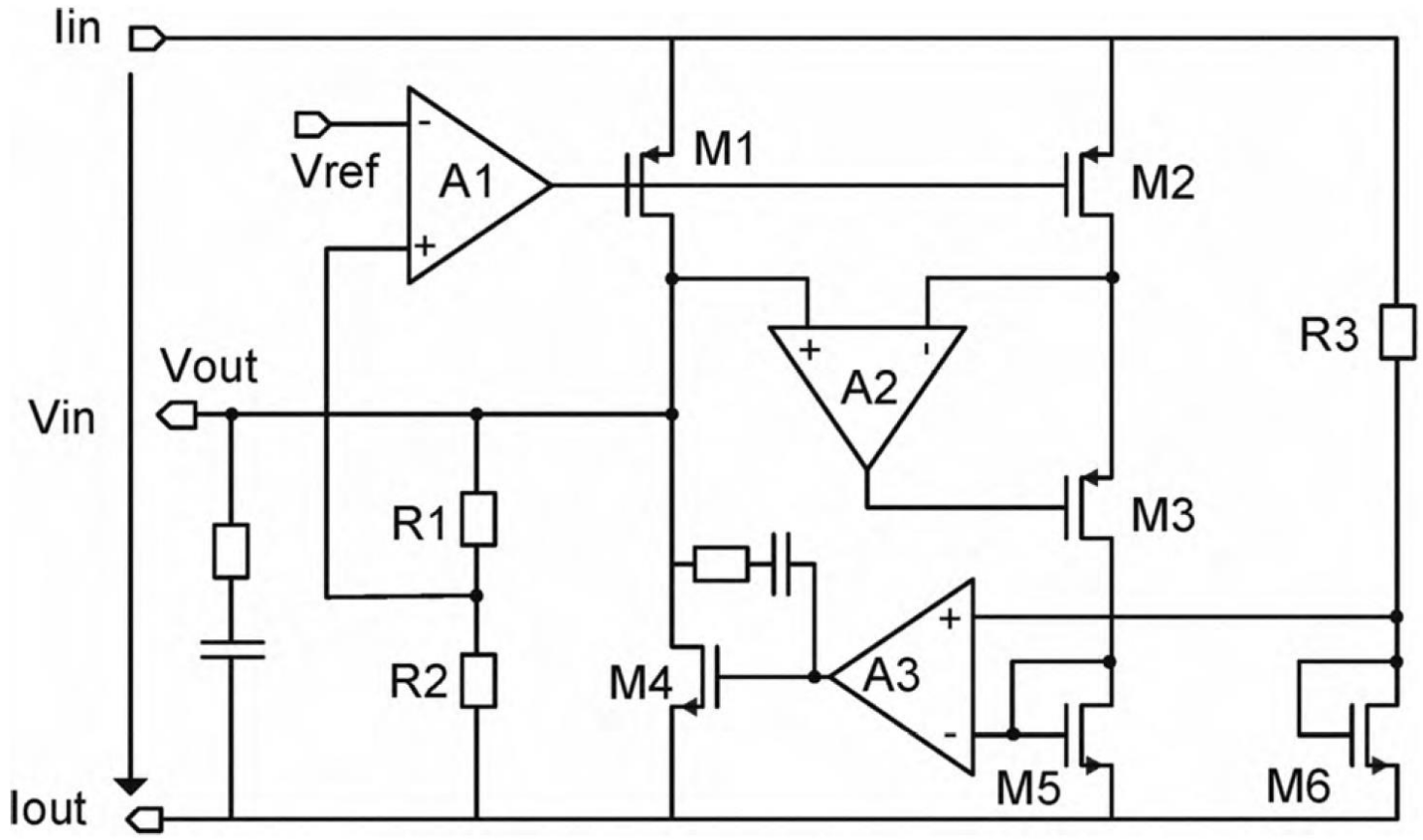


Regulator implemented on MuPix9





LDO regulator with shunt (1)



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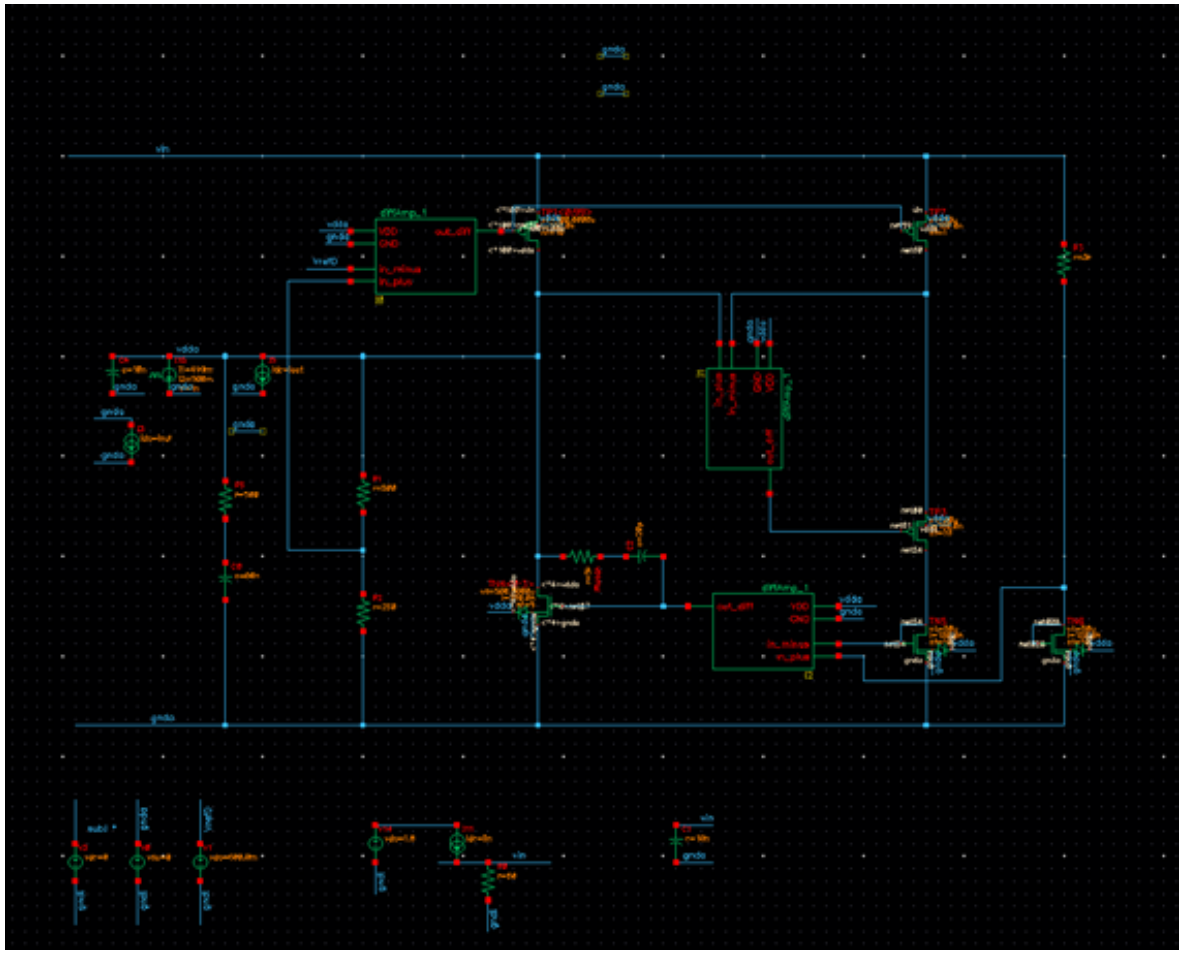

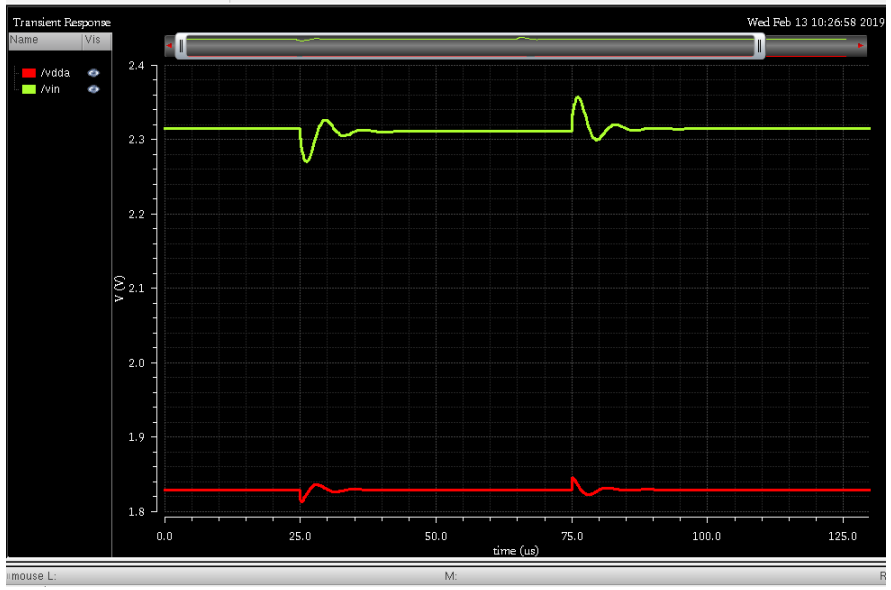

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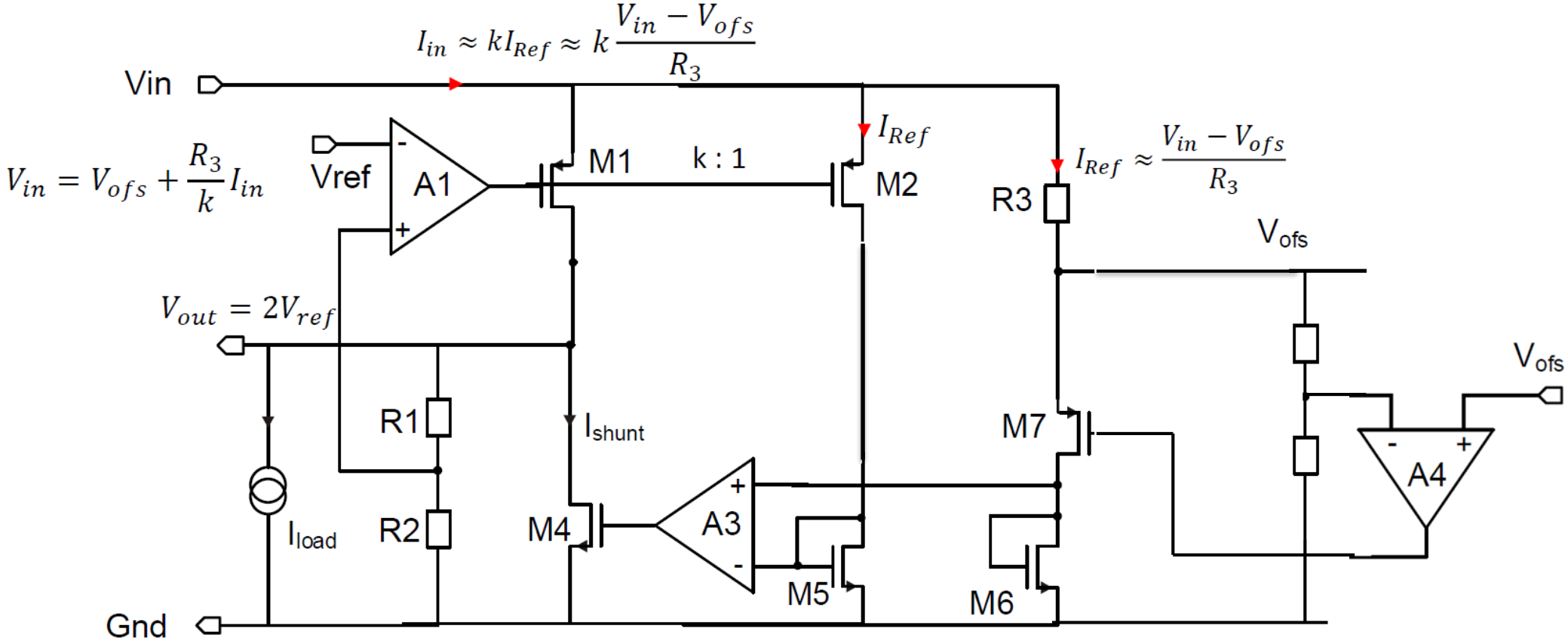
Modified LDO regulator with shunt (2)

- Modified circuit before A4, without A2



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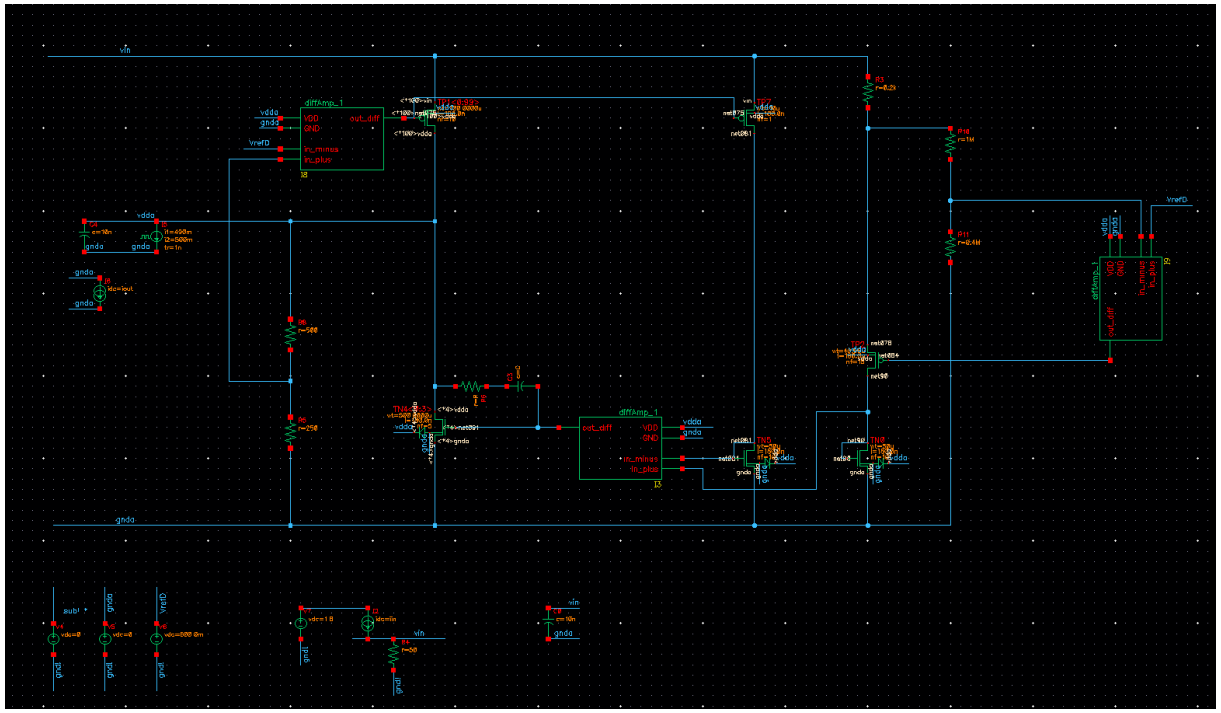

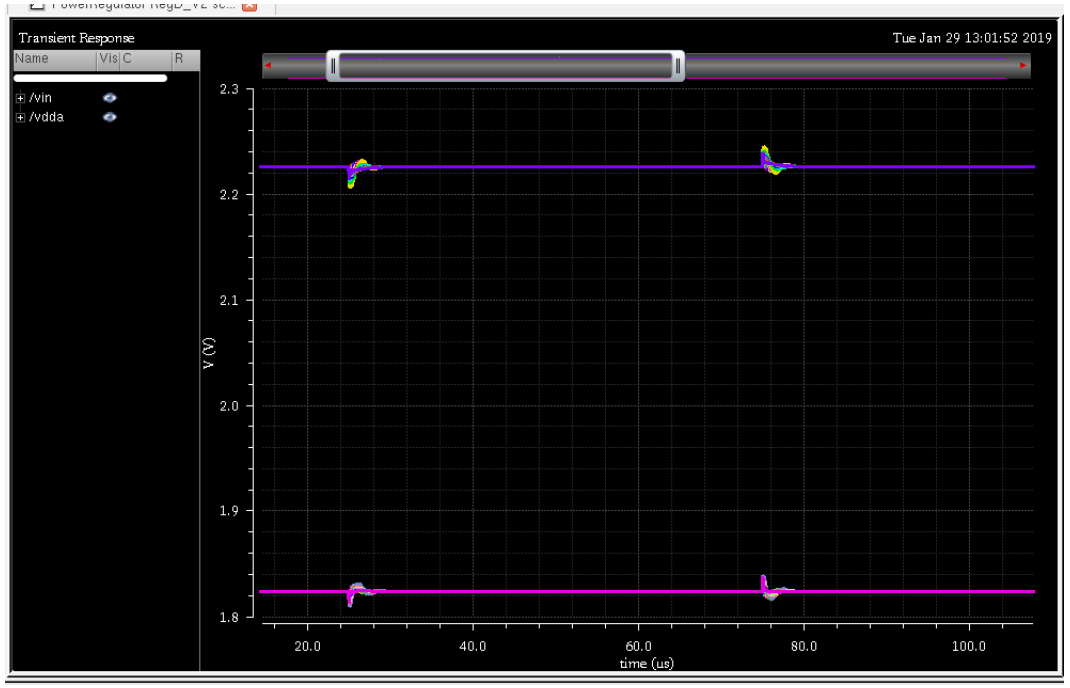

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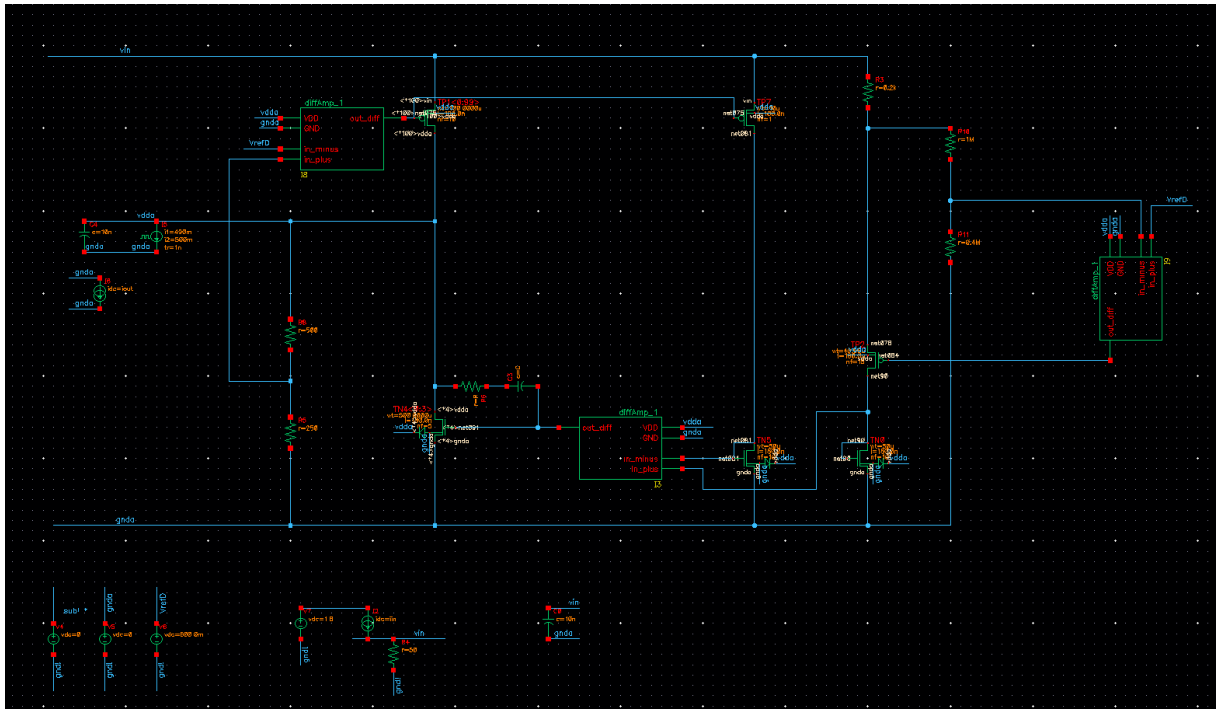

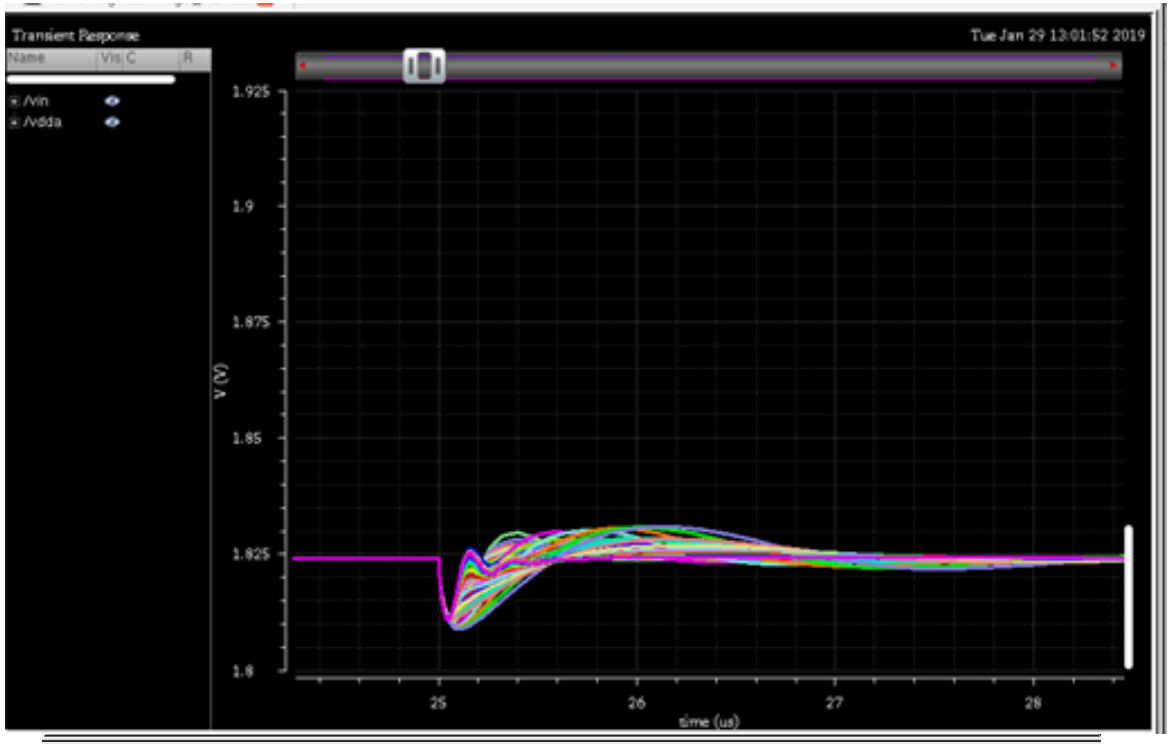

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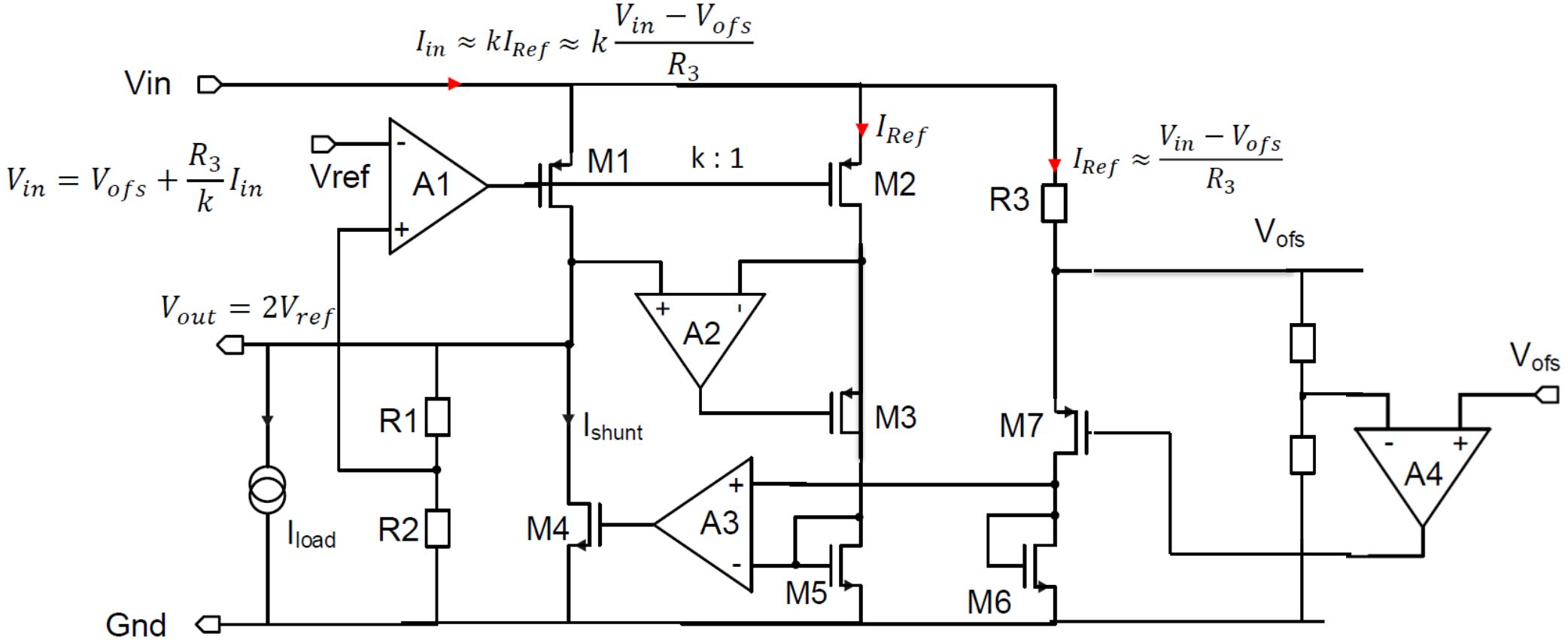

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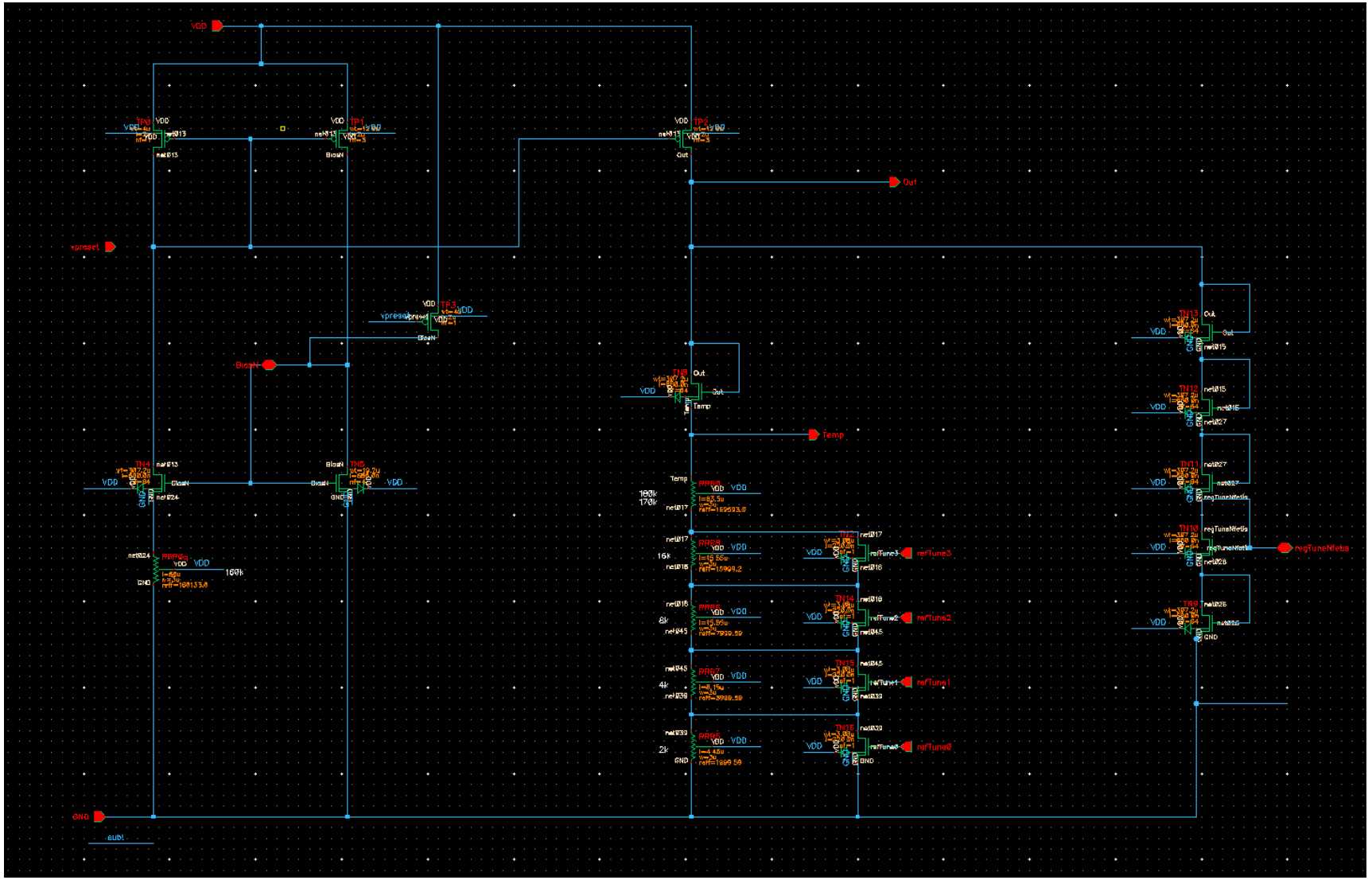
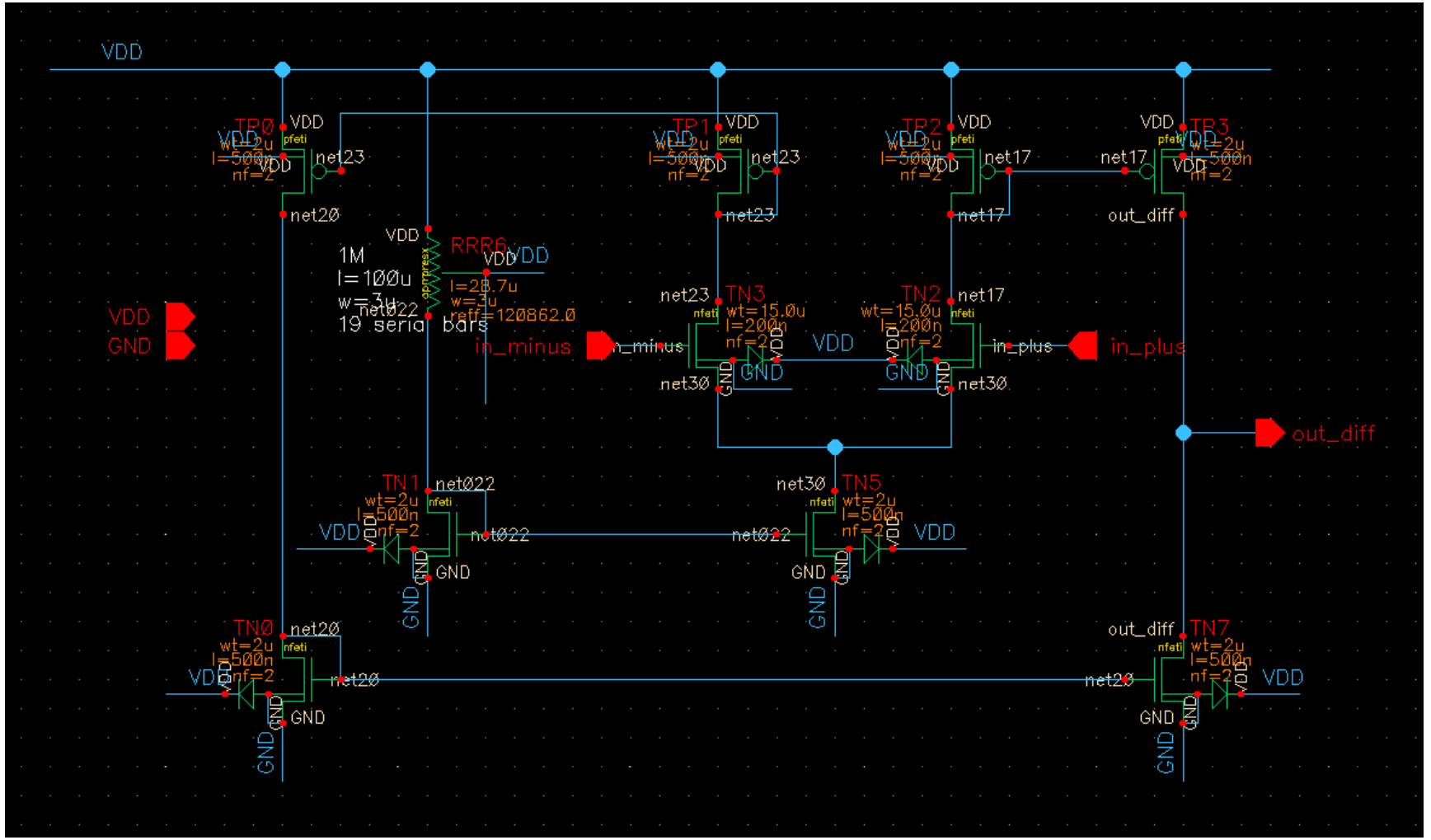
Bandgap for reference voltage implemented on ATLAS Pix3



Differential Amplifier implemented on ATLAS Pix3



Measurements with Power Regulator on MuPix9

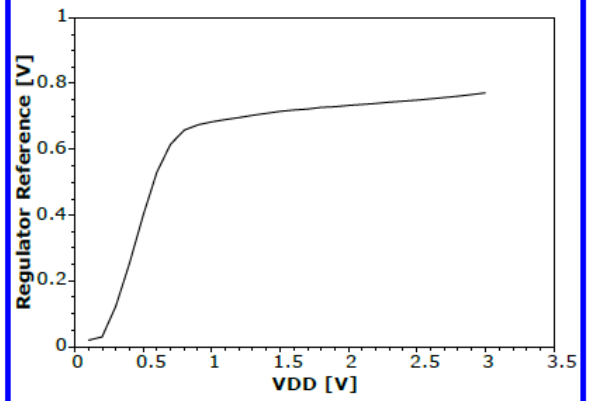


Fig. 1: The regulator's output voltage is flat in a wide range of VDD

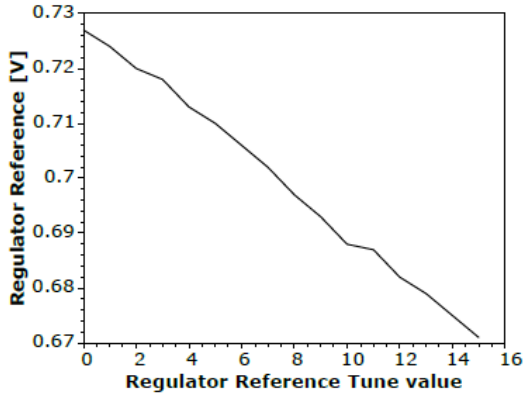
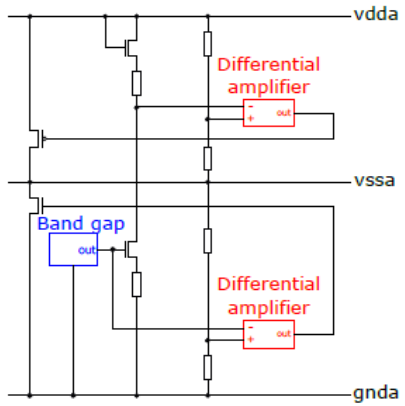


Fig. 2: Tune bits can fine tune the regulator's output voltage



Schematic of the power regulator used in MuPix9

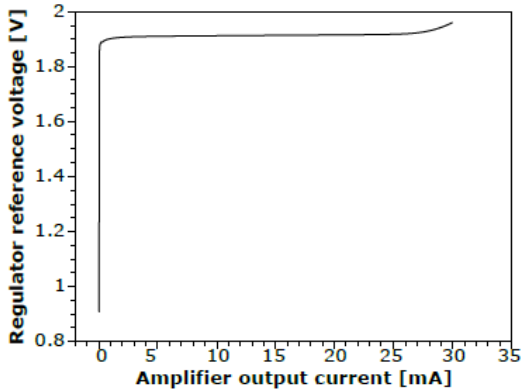


Fig. 3: The amplifier provides a stable voltage for a wide currant range

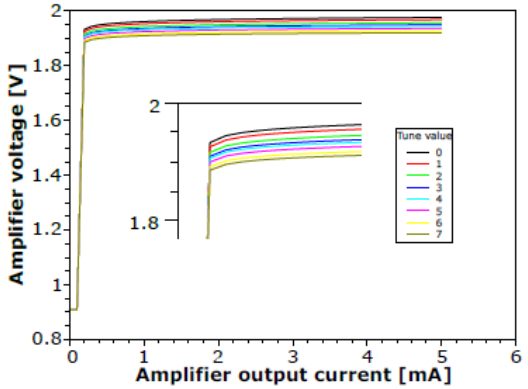
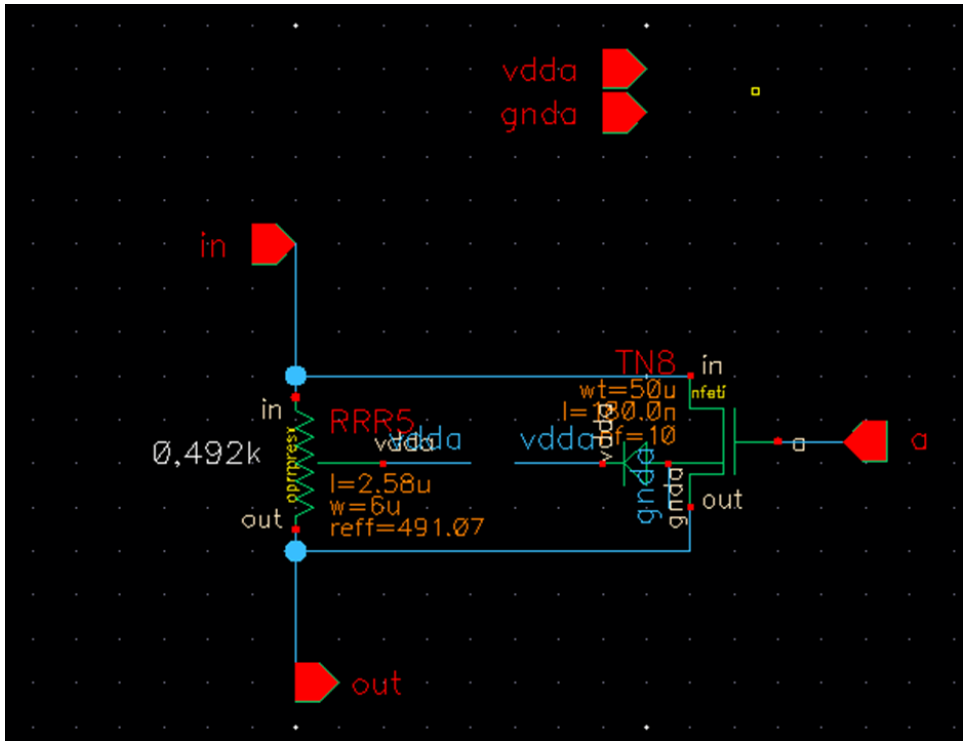
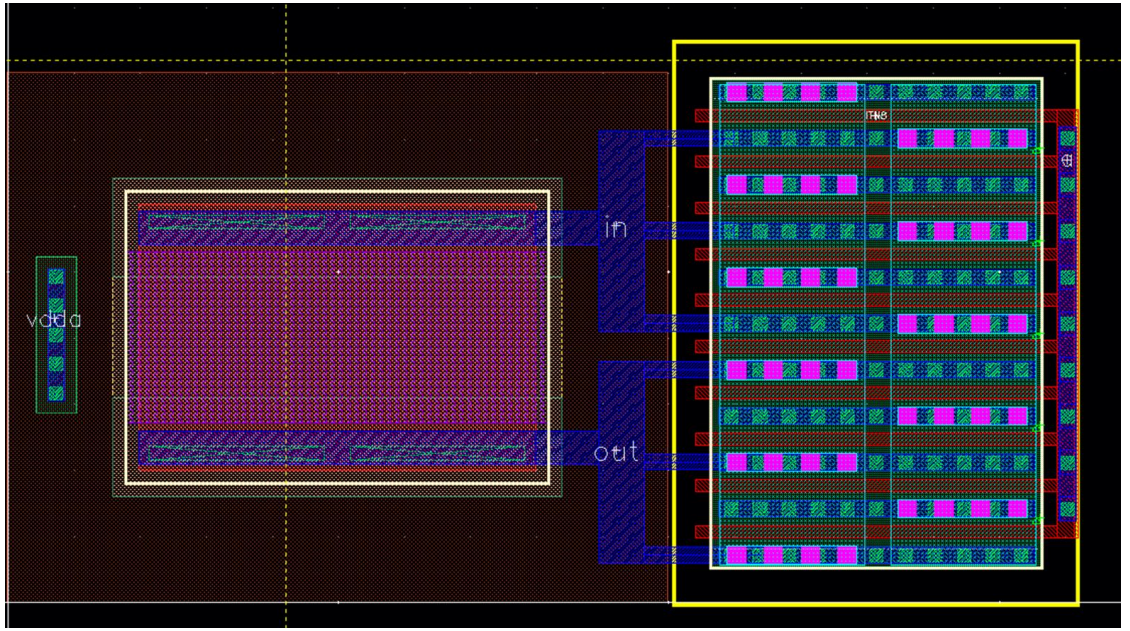


Fig. 4: Tune bits can fine tune the amplifier's output voltage

Power Regulator for ATLAS Pix3

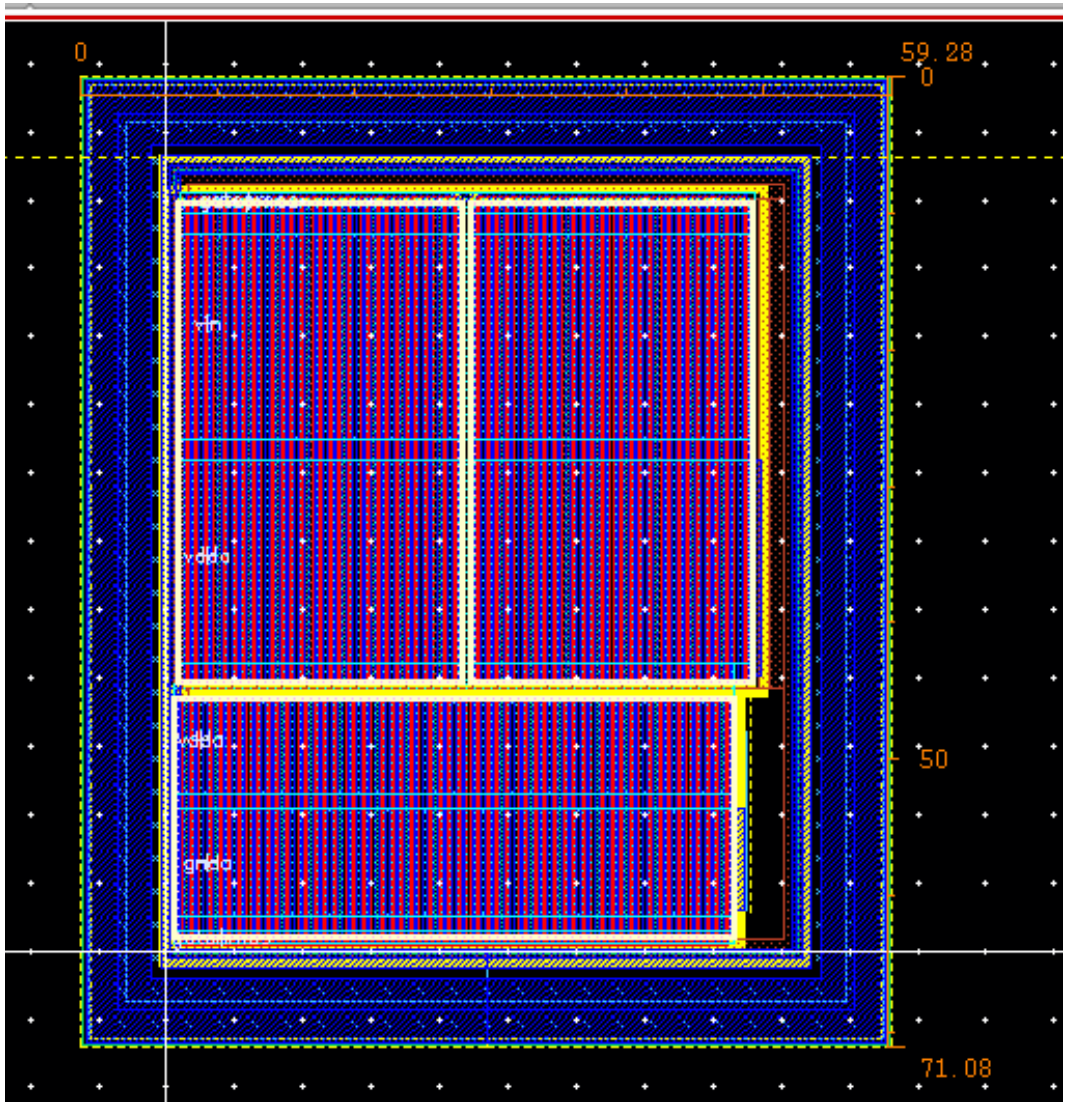
- RT Block





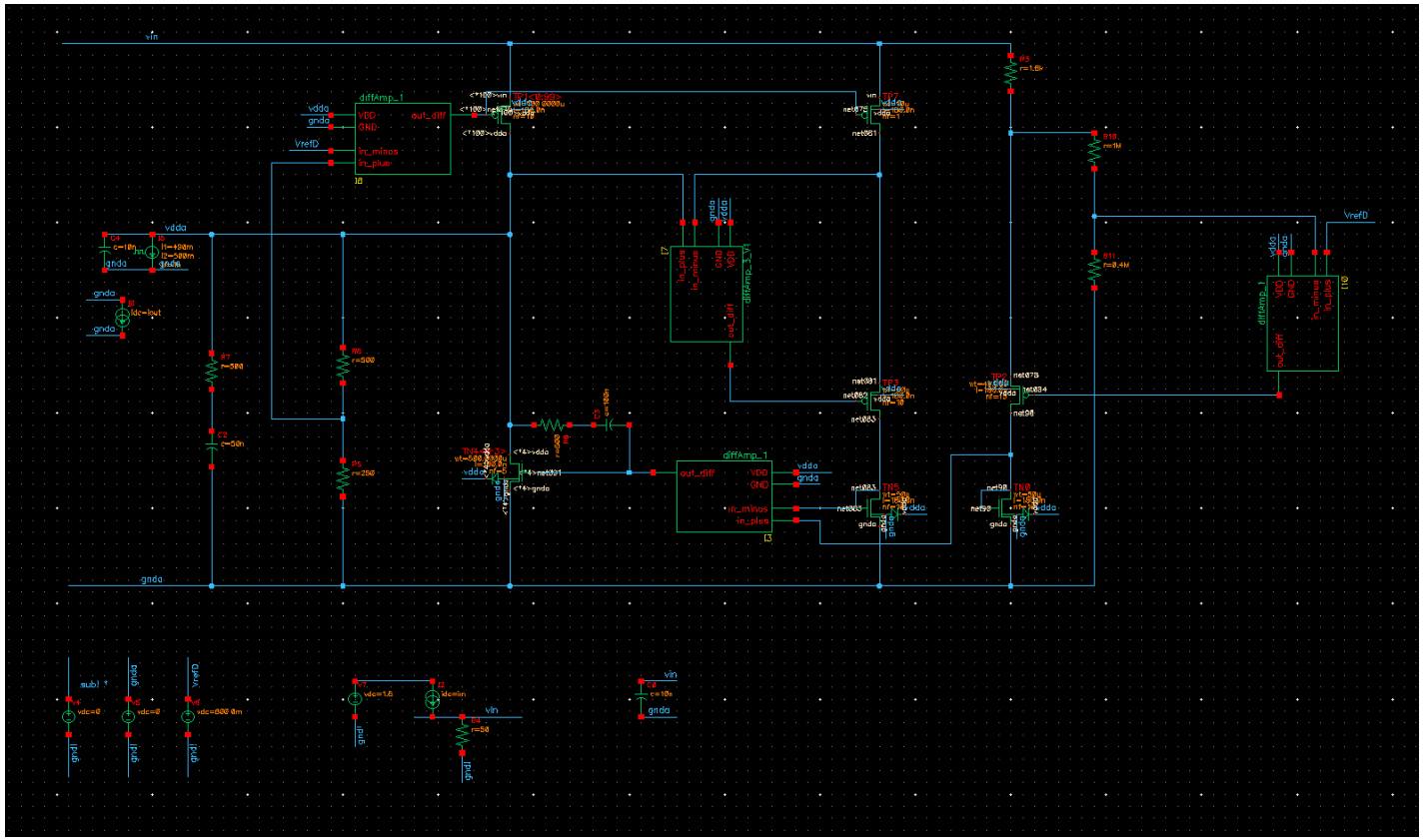
Power Regulator for ATLAS Pix3

- Big Transistors



Modified LDO regulator with shunt (2)

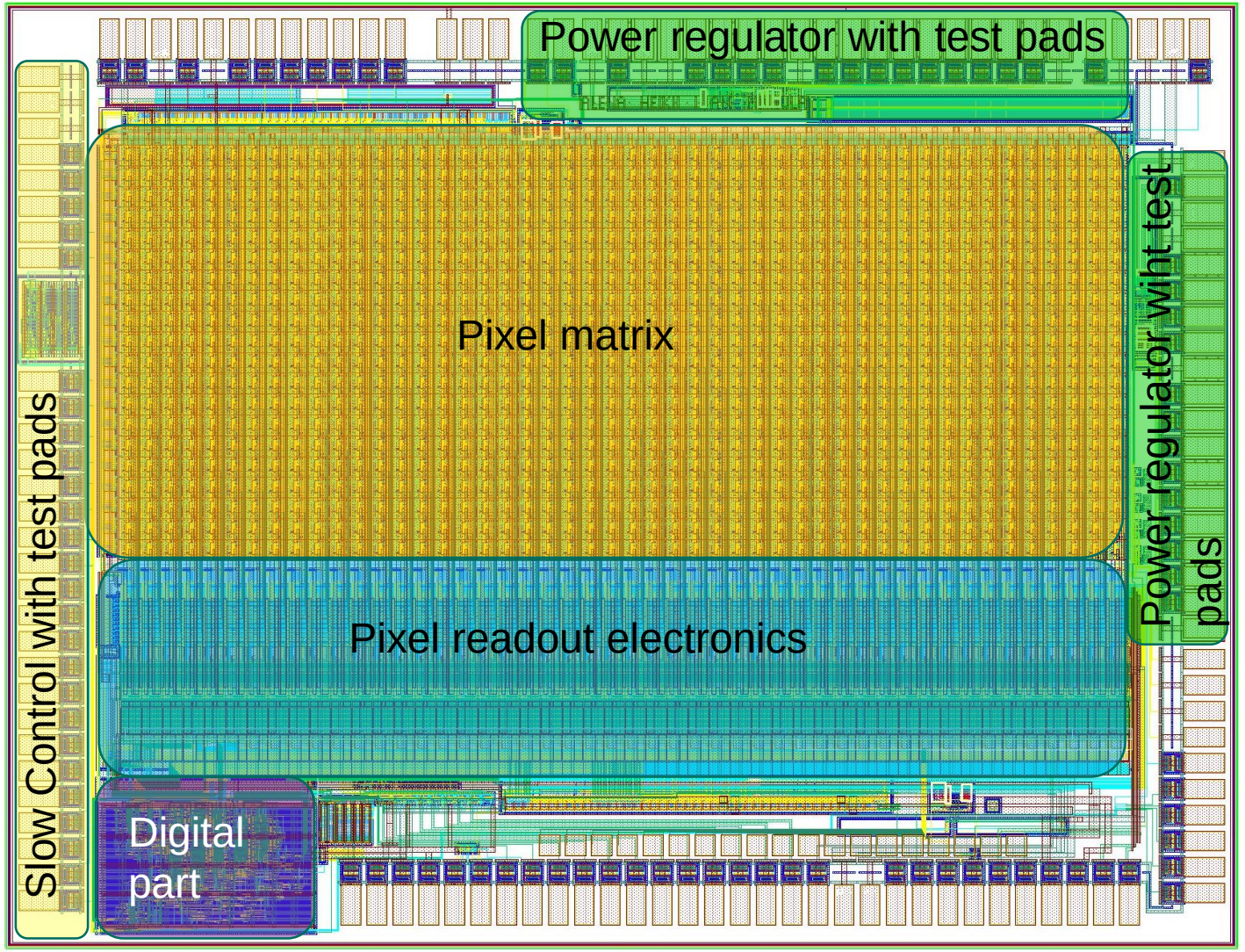
- Modified circuit before A4, with A2



(1) Michael Karagounis et al., “An Integrated Shunt-LDO Regulator for Serial Powered Systems”, Proceedings of ESSCIRC, 2009
(2) Michael Karagounis, “Serial Powering with the Shunt-LDO Regulator”, ATLAS Upgrade Week, 16.04.2018

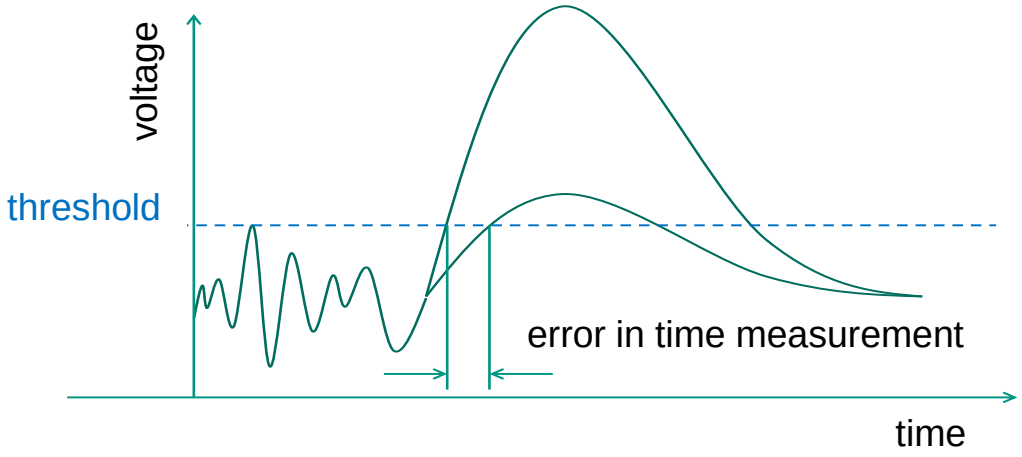
Overview of the MuPix9

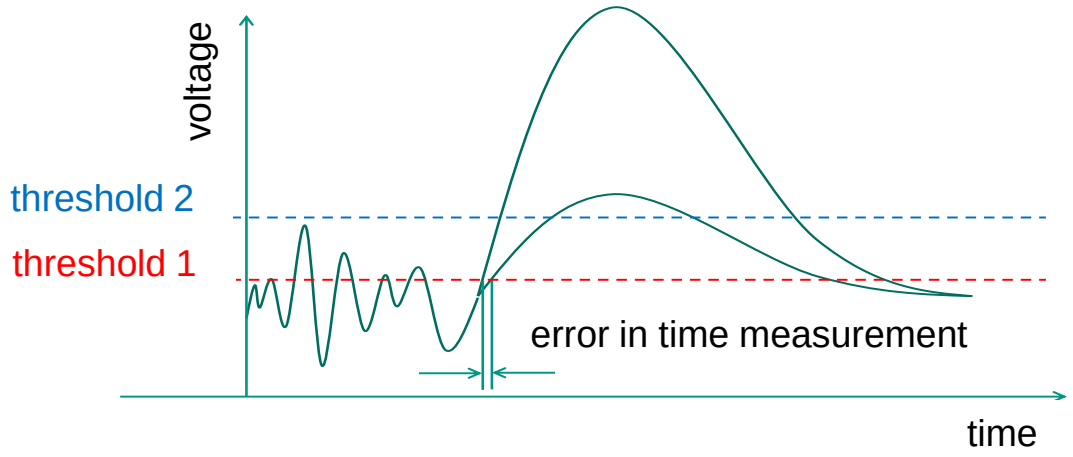
- Small sensor prototype (4700 um x 3600 um)
- AMS aH18 HV-CMOS
  - Minimal gate length of 180nm
  - Substrate with 20 Ωcm
  - 48 columns each with 20 pixels
- Main parts:
  - Pixel matrix
  - Pixel readout electronics
  - Digital part with slow control
  - Slow control as stand-alone part
  - Two power regulators



Overview of the MuPix9

- Changes in comparison to MuPix8
  - one pixel matrix
  - Pixels in NMOS instead of PMOS
  - Readout cells are modified: now with capacitor for capacitive coupling for serial powering. Three modes concept from MuPix8 is kept.

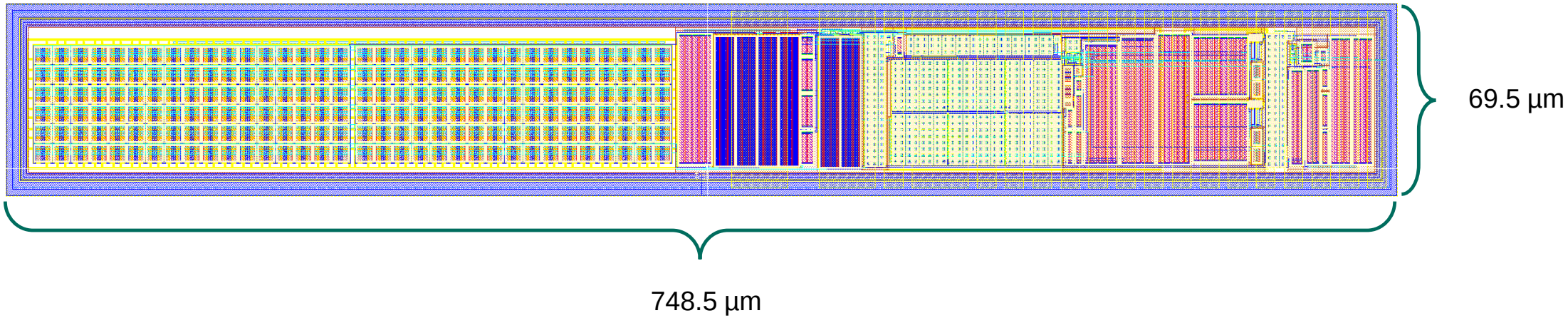




  - Digital part with modified state machine and new slow control
  - slow control as stand-alone part

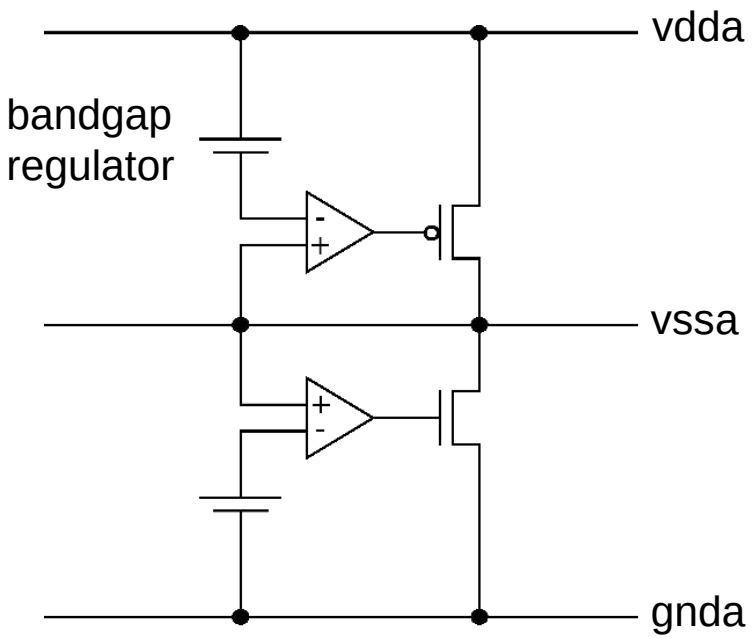
Regulator Element

- Same element with very small modifications for every solution
- Very small temperature dependency
- 8 tune bits
- Actual design as simple as possible, without linear regulator and as less space consuming as possible



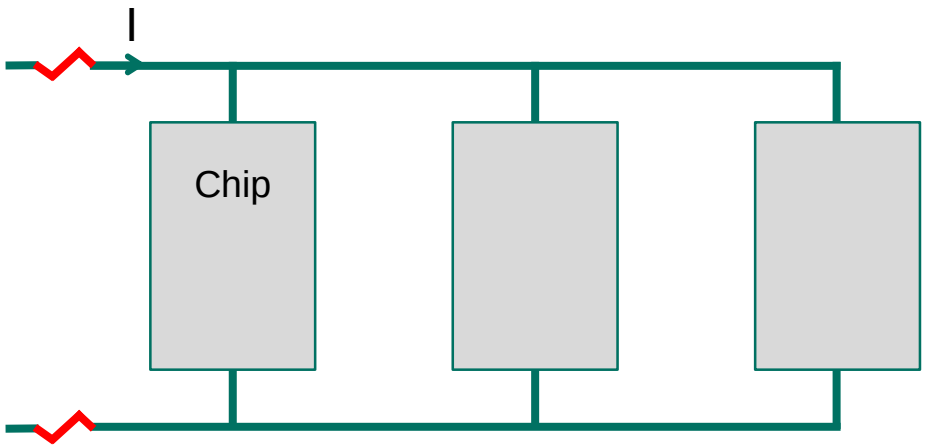
Regulator Element

- Same element with very small modifications for every solution
- Very small temperature dependency
- 8 tune bits
- Actual design as simple as possible, without linear regulator and very compact
- Functional concept is shown here:
  - bandgap regulator works like a battery, which supply a fixed current
  - in real circuit only one bandgap, current is mirrored
  - two differential amplifiers



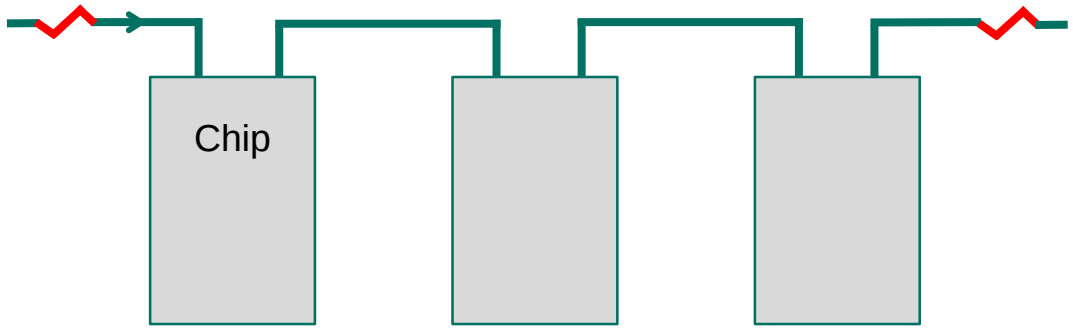
Serial powering – Introduction to standard concepts

- Parallel Powering



  - chip connection parallel, all outputs on same voltage level

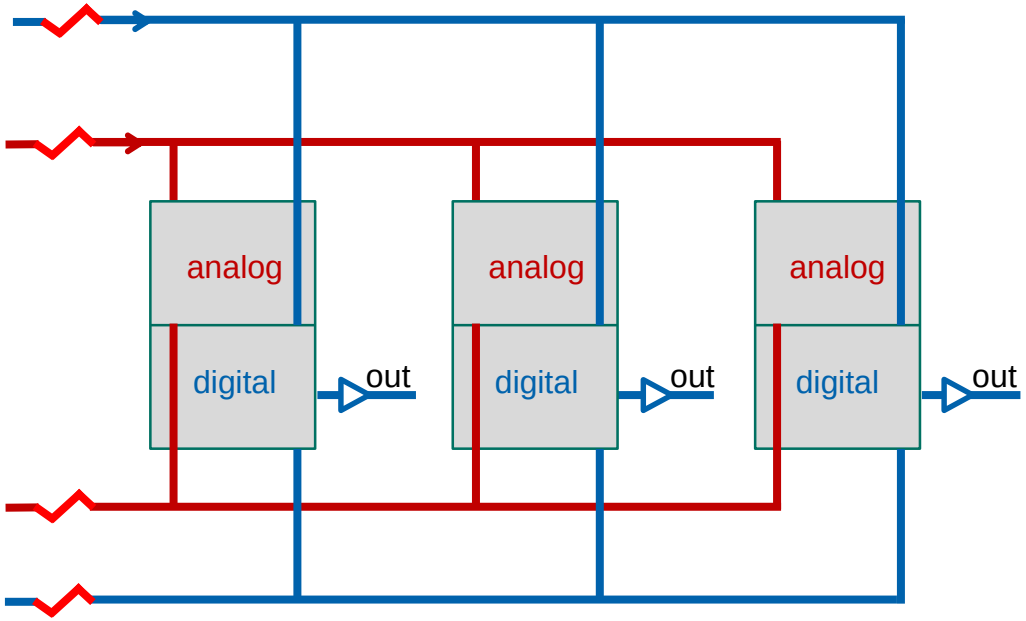
- Serial Powering



  - chip connection serial, all outputs on a different voltage level

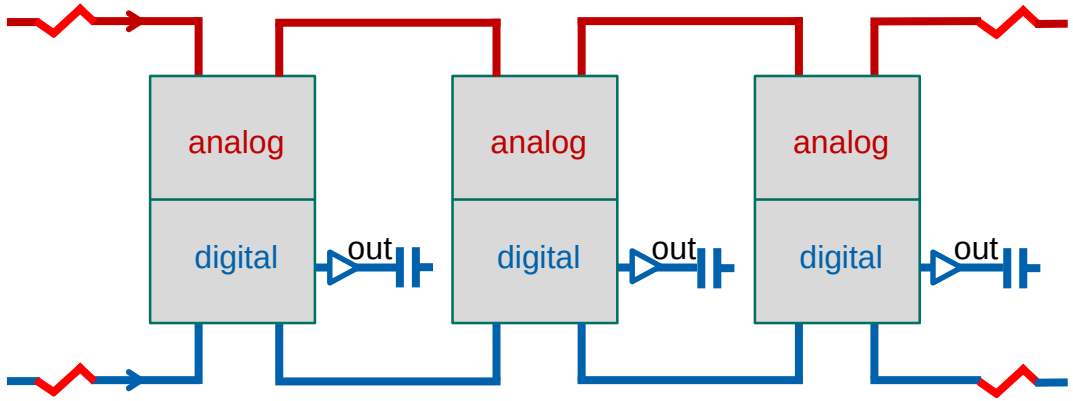
Serial powering – Introduction to HVCMOS concepts

- Parallel Powering



  - Analog and digital powering separated in two circuits
  - All digital levels are the same

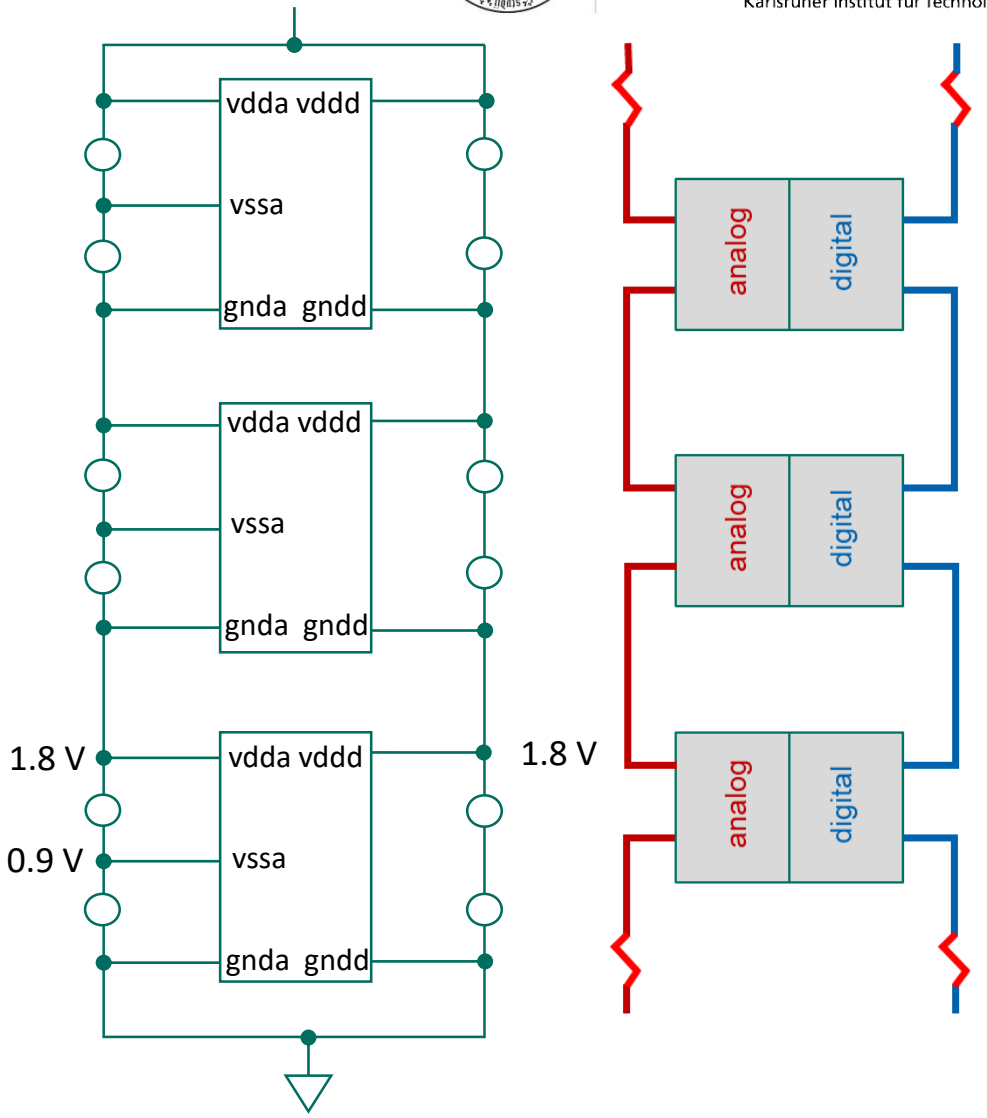
- Serial Powering



  - chip connection serial, all outputs on a different voltage level
  - Solution: conductive coupling

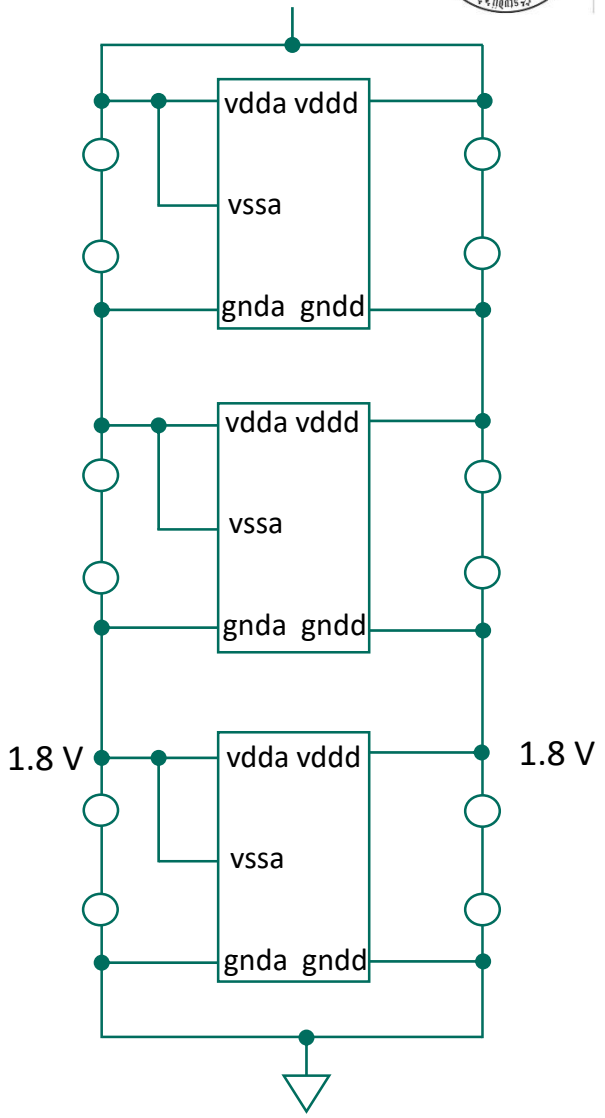
Chip interconnection concepts for serial powering
Concept 1: vdda and vssa separated

- Analog and digital voltage separated for lower noise
- Analog part with vdda (1.8 V) and vssa (0.9 V)
- Regulator element represented with two circles



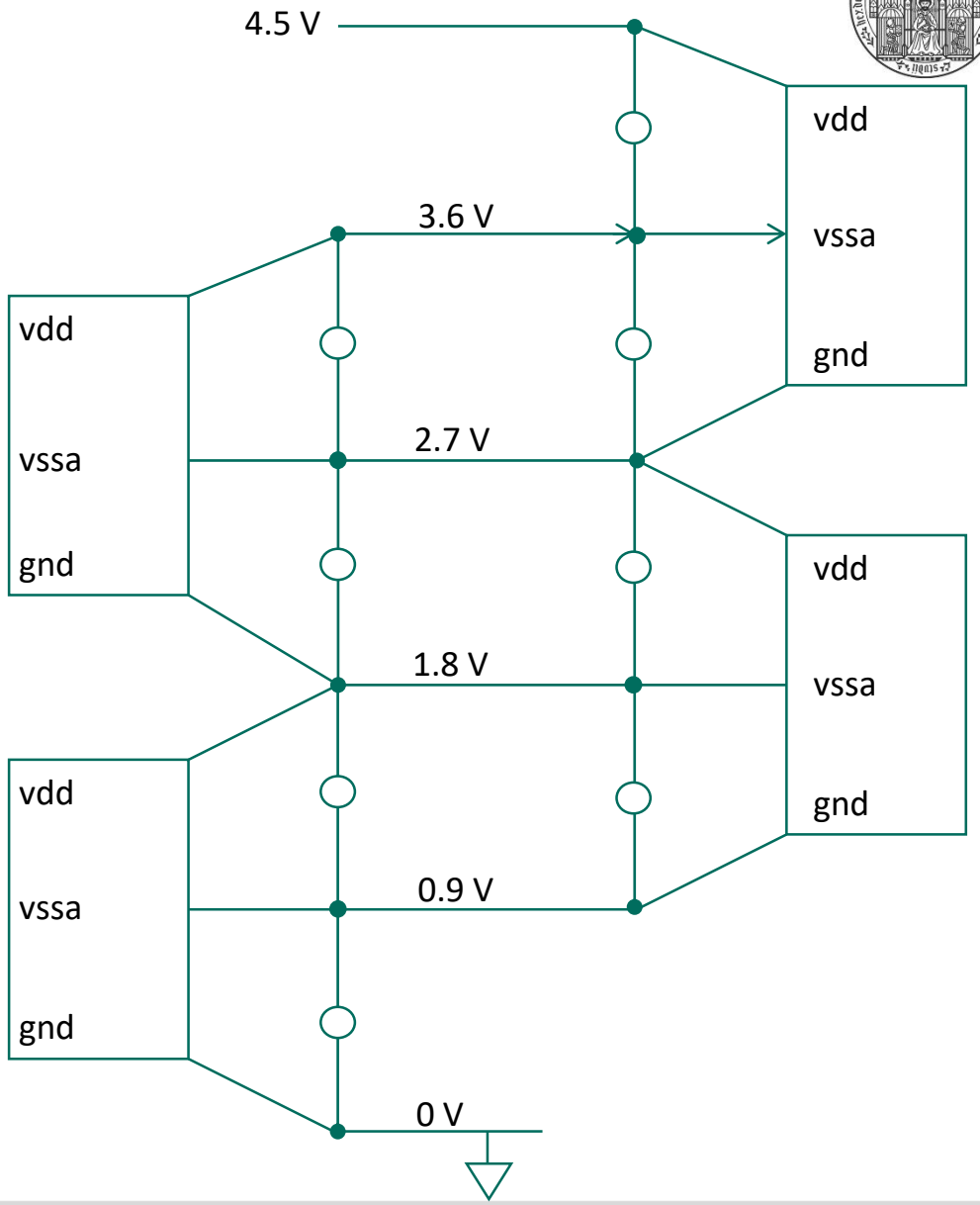
Chip interconnection concepts for serial powering
Concept 2: vdda = vssa

- Similar to concept 2, but:
- vssa = vdda = 1.8 V
- Redesign of pixel amplifier necessary



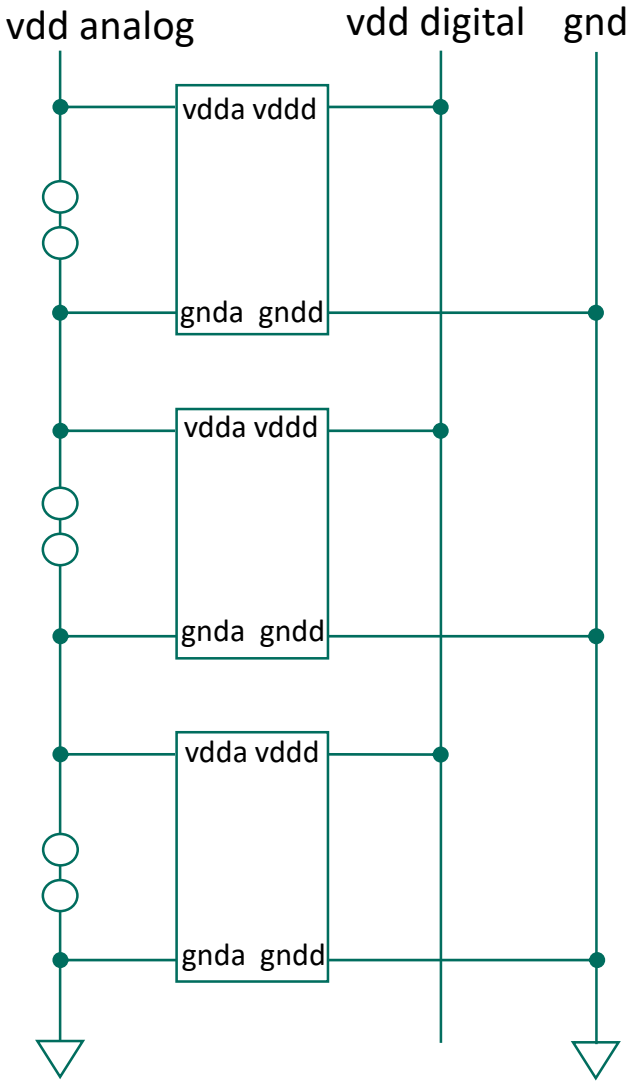
Chip interconnection concepts for serial powering
Concept 3: shared voltage

- Lower input current
- Less power consumption
- “Shared voltage”



Chip interconnection concepts for serial powering
Concept 4: analog part serial, digital part parallel

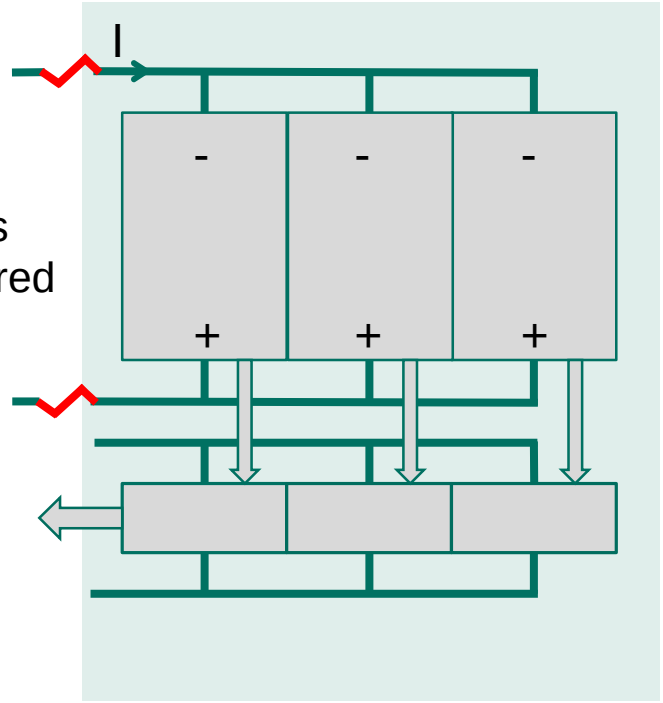
- Analog and digital voltage separated
- Analog part serial, digital part parallel
- For analog part all concepts that were presented can be used

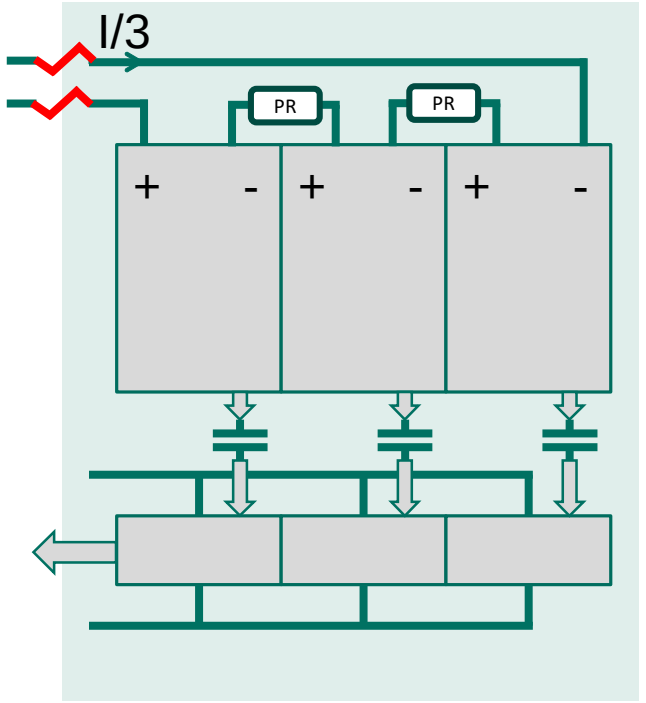


Vision for next generation MuPix

- On a full-size MuPix: three submatrices similar to MuPix8, but every submatrix identical
  - submatrices powered in serial
  - digital and analog power disconnected and captive coupled
  - chips powered in parallel
  - leads to a current reduction of 2/3

3 submatrices
parallel powered





3 submatrices
serial powered