The Pattern Recognition Mezzanine

for the ATLAS Hardware Tracking for the Trigger system

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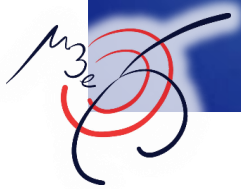
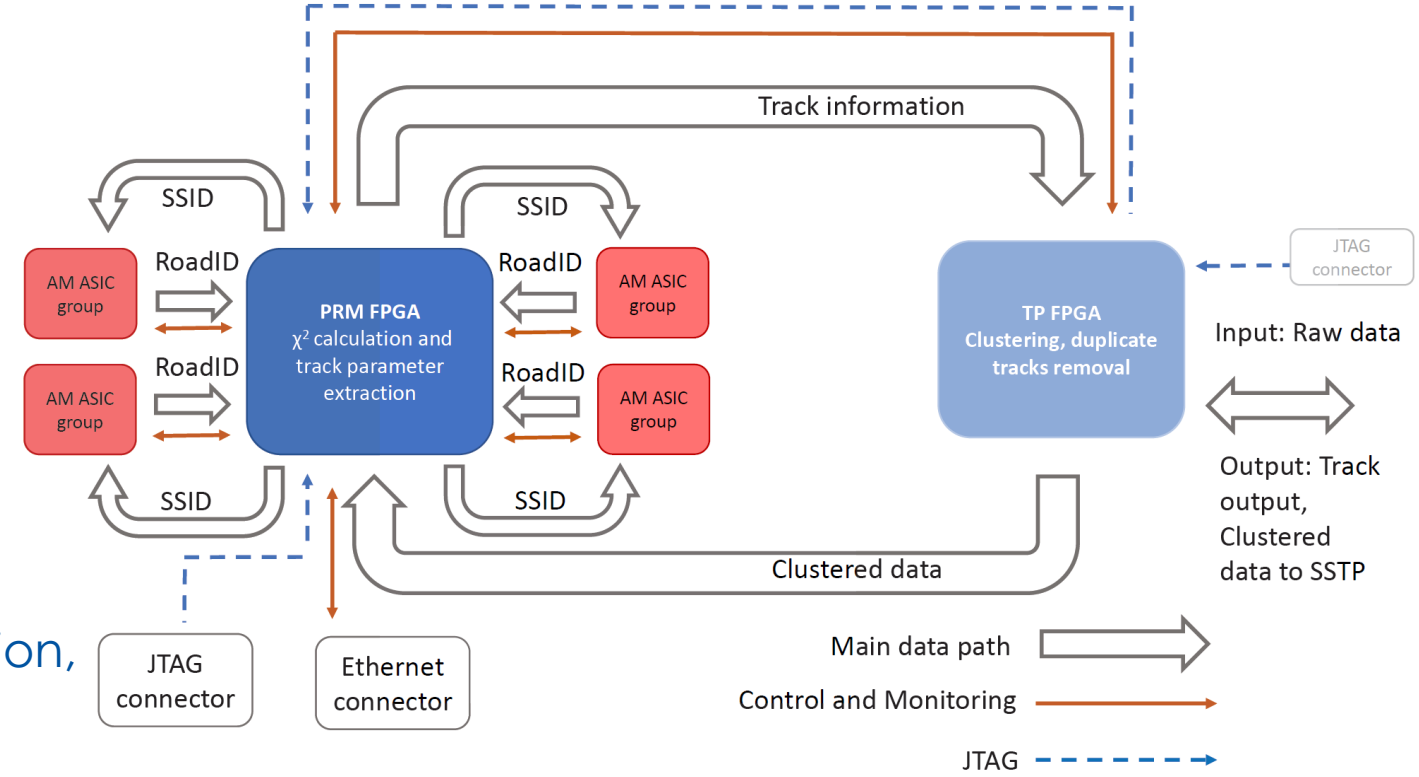


Pattern Recognition Mezzanine (PRM)

- Major components
  1. 20 × Associative Memory (AM) ASICs
  2. 1 × Intel Stratix 10 MX 1SM21BHN3F53E3VG
- Functionality
  1. Pattern recognition
  2. Data organization, preparation, track fitting and parameter calculation



The PRM is a mezzanine board.
The Tracking Processor (TP) is it's mother board in the HTT system

The AM ASIC

About the ASIC

- 32 Gb/s of input hit data
  - 250 MHz clock speed
  - 128 bit data interface
    8 × 16 bit hit information
- 3 × 128k patterns can be stored in production version AM 09
- Currently under development: small-scale version AM 08 with 16k patterns
- Technology TSMC 28 nm HPC+

The ASICs on the PRM

- Arranged in 4 groups of 5 ASICs
- ASICs within a group process hits in daisy-chain
- Two-event processing
  - Write hits to be matched
  - Read matched „roads“
- Road output interfaces from three ASICs in parallel

The Stratix 10 MX 2100

About the FPGA

- ~ 2.1 Mio Logic Elements
- ~ 700 k ALMs
- ~ 134 Mb of M20k Memory
- ~ 4k DSPs
- 8 GB of HBM2 high-bandwidth DRAM
- 94.5 Mb of eSRAM
- Speed grade #3 device

The FPGA on the PRM

- Performs track fit
  - Linearized χ^2 fit
  - Up to 4 × 1 Gfit/s
- Calculates track parameters

The Stratix 10 MX 2100

Linearized χ^2 fit

Constants S_{ij}, h_i

Cluster coordinates x_j

$$\chi^2 = \sum_{i=1}^{N_{dof}} \left[\left(\sum_{j=1}^{N_{coo}} S_{ij} x_j \right) + h_i \right]^2$$

Track parameter calculation

Constants C_{ij}, q_i

$$p_i = \sum_{j=1}^{N_{coo}} \left(C_{ij} x_j + q_i \right)$$

N_{dof}: # degrees of freedom

N_{coo}: # coordinates

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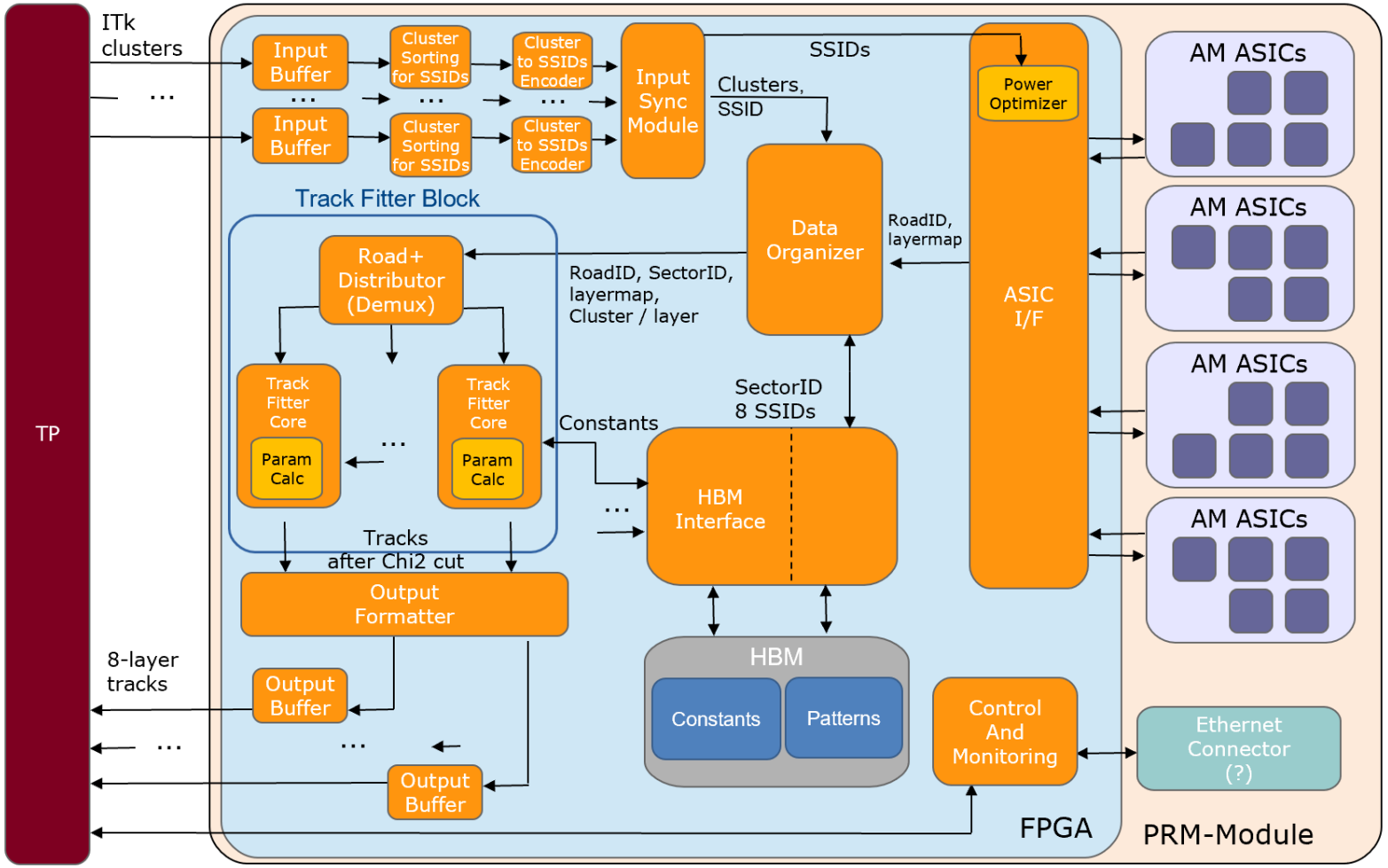
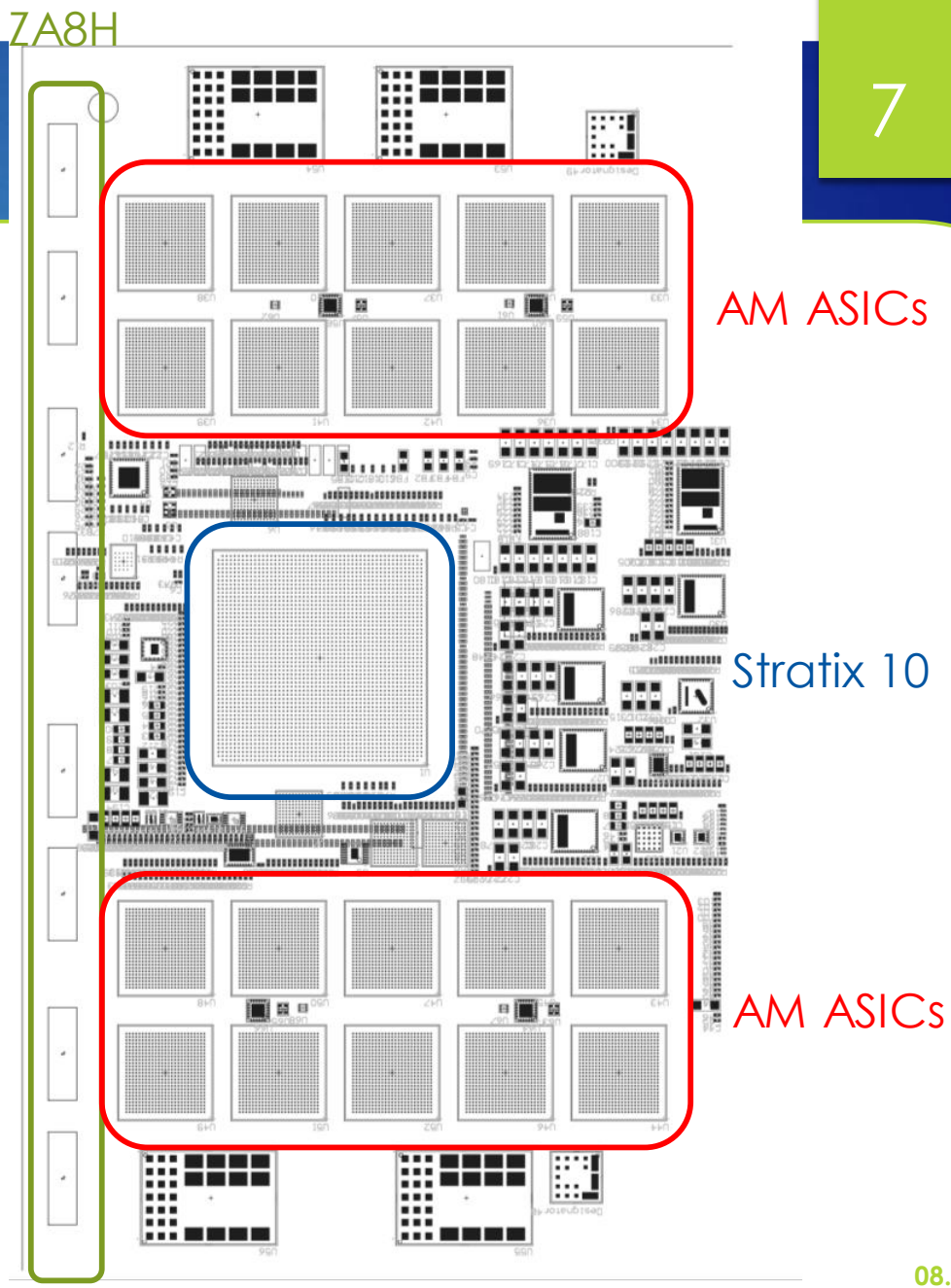
PRM Firmware



The PRM board

- A very early image of the layout (> 4 months old)
- Shows the main components
- Interfaces via
  8 Samtec ZA8H (0.33 mm) connectors with 7 × 12 contacts
  - 36 Multi-gigabit transceivers
  - 2 Gigabit Ethernet LVDS Tx+Rx
  - JTAG
  - I2C, power enables, clock input, …
  - +12 V as power input
- Max 10 FPGA for power up sequence and slow control



Estimated power consumption

- Driven by the PRM physics goals
- CBE: Current best estimate
- MEV: Maximum estimated value adds contingency
- MPV: Maximum possible value adds margin

Component	Parameters	CBE	MEV	MPV
PRM Power Estimate (W)		**166**	**188**	**215**
	FPGA Power (W)	**72**	**77**	**84**
Power Breakdown (W)	MGT+IO			
	DSP			
	Logic+RAM			
	HBM			
Assumptions	Links (count @MPV)	32+16	32+16	32+16
	Clock - Data Organiser + others (MHz)	250	300	350
	Clock - Track Fitter (MHz)	200	240	280
	LUT	34%	41%	48%
	FF	34%	41%	48%
	BRAM	29%	35%	41%
	DSP	60%	72%	84%
	HBM (Rd/Wr)	90/10%	90/10%	90/10%
	I/O (LVDS+SE)	92%	92%	92%
	Low-V DC-to-DC	**25**	**28**	**32**
	AM ASICs	**69**	**83**	**99**